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7 Key Drivers of Change in Product Design Today

How are companies are addressing digital transformation, ever-increasing design complexity, and the effects of a postpandemic world on tech companies amid the so-called "Great Resignation?" A study of nearly 300 companies gauges the shifting approaches to hardware and software. by JOHN MCMILLAN



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Microvia Reliability Testing Utilizing D-Coupons to Understand Best Design Practice

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Cold Underfill Component Removal

PCB component milling removal processes have become more automated, and many previous shortcomings in milling of electronic components have been overcome. These process developments, due to the built-in vacuum chuck and real-time, high precision laser-guided depth measuring, make the latest commercial version of milling of components more attractive. by BOB WETTERMANN



ON PCB CHAT (pcbchat.com)

BEST PRACTICES FOR AUTOMATION with STEPHEN CHAVEZ

NO- AND LOW-HEAT SOLDER

with DR. ANDY MACKIE, PH.D. and DR. IAN TEVIS, PH.D.

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MIKE BUETOW PRESIDENT

A Different Kind of Additive Manufacturing

WAS ALL set this month to write about plating using additive manufacturing, but when someone pointed out just how subtractive the industry really is, it compelled a change in plans.

It came in the way of an email from Dr. Hayao Nakahara, the preeminent market researcher in the printed circuit industry. Naka, as he is known to friends, shared results of a months-long study of the North American PCB supply base.

This was no easy task. Naka started with the Fabfile database, long the favorite child of Harvey Miller. Harvey, who is about to hit 100 years old (!), gave Naka the keys to the car. In turn, Naka reached out to every company on that list, diligently revising and updating. The effort took more than three months.

When he was finished, he had a list of 177 merchant corporations in the US, Canada and Mexico (yes, there are a few south of the US border) that build bare printed circuit boards. Those 177 corporations represent 220 sites. The net revenue, based on his best estimates, is roughly \$2.87 billion. Those companies broker another \$400 million or so worth of PCBs to North American buyers. That puts the domestic fab market from the suppliers' perspective at roughly \$3.27 billion.

That's on par with what North America produced and sold in 2018, and a few hundred million behind where it was in 2015 and 2016.

There have been some true success stories over the past decade. TTM has become one of the largest fabricators in the world, and that's even after selling off most of its China operations – and the \$530 million in revenue they reaped. Summit Interconnect has found a niche in the prototype and high-reliability sectors and grown both organically and through targeted acquisitions to become the second-largest US fabricator. No. 3 APCT has done likewise.

But large-scale, industrywide organic growth has been hard to come by. Correcting for inflation, the domestic industry is trending sideways, not up.

That's why I'm so bullish on the Printed Circuit Board Association of America. It has a vision for growing the industry, not just the member companies. It gets that the goal needs to be broad-based growth, not individual company preservation.

This picture isn't complete, of course, without the buy side. The general thinking a few years ago was domestic bare board purchases by OEMs and EMS companies amounted to about \$4 billion per annum (of which about \$2 billion is for military and related buys). If correct, at \$3.2 billion, the domestic supply base has an 80% market share. There's not a lot of headroom to grow.

OEMs and EMS companies must grow their capacity in order to create a larger market for domestic suppliers.

As we've mentioned in these pages, new US legislation,

introduced in May, proposes to incentivize buyers of boards manufactured in the US.

As of this writing, H.R.7677 – Supporting American Printed Circuit Boards Act of 2022, the so-called Boards Act, has just five cosponsors. Even with the whole of Congress's backing, however, it probably won't move the needle on its own. The domestic *buy* side capacity just isn't large enough.

So while the Chips Act has helped unleash billions of dollars in new semiconductor capacity investment in the US – I'm not giving it full credit, as I believe crackdowns on exports of technology needed to design and build semiconductors are having their intended effect, too – it's reasonable to think similar incentives for the Flexes, Jabils, Sanminas and so on down the line, not to mention the thousands of OEMs with internal purchasing or assembly operations, would help create the bigger market needed for those domestically produced boards.

And that market needs to be made onshore. After all, no one is talking about future export markets for North American-made bare boards. It is sell here, or sell nothing.

That's the kind of switch from subtractive manufacturing – a shrinking domestic market – to additive manufacturing – a growing one – I can really get behind.



mike@pcea.net @mikebuetow

P.S. Those looking at expanding or changing their PCB or EMS supply base would do well to attend the PCB West exhibition (pcbwest.com) on Oct. 5 at the Santa Clara Convention Center. Some three dozen manufacturers of all sizes and specialties will be on hand. Check it out!



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PCDF People

Incap named **Hanno Septer** to its strategic sourcing and purchasing team.

Nano Dimension named **Quintin Armstrong** North America service manager. He has experience in sales and engineering with leading contract assemblers and SMT process equipment OEMs over 30 years in the electronics industry.



Rivian named Juan Frias staff PC board designer. He has more than 20 years' experience in electronics design with Flex, Continental, MJS, Crane and most recently Glenair.



Summit Interconnect named Sean Patterson chief operating officer. He was most recently chief revenue officer at Nano Dimension, and held multiple leadership roles in Amazon's

transportation and healthcare groups. He also led numerous aerospace and defense manufacturing plants during his tenure at TTM Technologies.

PCDF Briefs

Altix received additional orders from Elcoflex for its AcuReel system.

ArtnetPro has acquired CAD/Art Services, expanding its engineering, photoplotting, photomask and editing capabilities. Financial terms were not disclosed.

Flexium Interconnect announced its official entry into R100, a global renewable energy initiative led by Climate Group and the Carbon Disclosure Project (CDP), pledging to use 100% renewable energy by 2040 to help drive the development of Taiwan's renewable power industry and reduce the impact of climate change to achieve a sustainable future.

Guangzhou Taihua Multilayer Circuit has suspended production amid ongoing financial losses.

Icape Group has acquired **Møn Print**, a Danish PCB, for about \$700,000, subject to additional payments depending on the company's 2022 and 2023 results.

Jabil is investing \$3 million in a new design center Wrocław, Poland, scheduled to open this month. The new site will focus on automotive and healthcare products and will be staffed by more than 30 engineers when fully operational.

Luminovo, the Al-powered software suite for electronics makers, has raised €11 million in a seed round.

A team led by the Massachusetts Institute of Technology (MIT) has devised an elec-

Berkeley Scientists Develop Biodegradable Printed Circuit

BERKELEY, CA – A team of researchers from the Department of Energy's Lawrence Berkeley National Laboratory (Berkeley Lab) and UC Berkeley have developed what they say is a fully recyclable and biodegradable printed circuit.

The researchers, who reported the new device in the journal *Advanced Materials*, say that the advance could divert wearable devices and other flexible electronics from landfill, and mitigate the health and environmental hazards posed by heavy metal waste.

For the study, Ting Xu, faculty senior scientist, Berkeley Lab Materials Sciences Division, and professor of chemistry and materials science and engineering at UC Berkeley, and her team eschewed expensive purified enzymes in favor of shelf-ready enzymes known as Burkholderia cepacian lipase (BC-lipase) "cocktails." This significantly reduces costs, facilitating the printed circuit's entry into mass manufacturing, Xu said.

Doing so enabled the researchers to develop a printable conductive ink composed of biodegradable polyester binders, conductive fillers such as silver flakes or carbon black, and commercially available enzyme cocktails.

Using a commercial 3-D printer, the team printed the conductive ink in patterns onto various surfaces such as hard biodegradable plastic, flexible biodegradable plastic, and cloth.

To test its shelf life and durability, the researchers stored a printed circuit in a laboratory drawer without controlled humidity or temperature for seven months. After pulling the circuit from storage, the researchers applied continuous electrical voltage

to the device for a month and found that the circuit conducted electricity just as well as it did before storage.

Next, the researchers put the device's recyclability to test by immersing it in warm water. Within 72 hours, the circuit materials degraded into its constituent parts. The silver particles completely separated from the polymer binders, and



The recyclable, biodegradable printed circuit. (Marilyn Sargent/Berkeley Lab)

the polymers broke down into reusable monomers, allowing the researchers to easily recover the metals without additional processing. By the end of this experiment, they determined that approximately 94% of the silver particles can be recycled and reused with similar device performance.

That the circuit's degradability continued after 30 days of operation surprised the researchers, suggesting that the enzymes were still active. Xu attributes the working enzymes' longevity to the biodegradable plastic's molecular structure.

The circuit also shows promise as a sustainable alternative to single-use plastics used in transient electronics – devices such as biomedical implants or environmental sensors that disintegrate over time.





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tronic skin that communicates wirelessly without requiring chips or batteries.

Meizhou Kejie Electronic Technology has begun construction on a multilayer HDI PCB plant expected to achieve annual revenue of more than \$350 million.

Modelithics named EMA Design Automation as a reseller.

The **TPCA** postponed the International Circuit Board Exhibition – Shenzhen, better known as TPCA Show-Shenzhen, citing Covid concerns. The venue will not change and the new date will be announced, TPCA said.

CA People

Benchmark named **Tiffany Elle** director of internal communication.

Flex announced **Christopher Butler** as president, Industrial Business.

ShinePure Hi-Tech (Ningbo) named Ning Cheng-Lee account executive.

CA Briefs

The Anti-Malware Testing Standards Organization (AMTSO) in September released its first guidelines for testing IoT security products (www.amtso.org/news/ amtso-publishes-guidelines-for-testing-ofiot-security-products).

Bentec appointed **Sincotron** as **Insituware** distributor in Scandinavia and the Baltics.

Dixon Technologies has entered into an agreement with **Google** to make LED TV sets on the Android and Google TV platforms.

Electronic Design and Manufacturing held a groundbreaking ceremony on Aug. 22 to mark commencement of construction on an 11,400 sq. ft. expansion of its manufacturing facility.

Foxconn has signed a \$300 million memorandum of understanding with a Vietnamese developer to expand its facility there. Foxconn is also in talks with Saudi Arabia about jointly building a \$9 billion facility that could make chips, EV components and other electronics, the *Wall Street Journal* reported.

Google plans to move the assembly of the latest Pixel devices from its **Foxconn** factory in southern China to Vietnam, where it will begin production of the Pixel 7. More than half of high-end Pixel devices will be mass-produced in Vietnam next year.

Henkel Korea announced the completion of its state-of-the-art Songdo Plant within

Nortech Gains Patent for High Frequency Flex Circuit

MINNEAPOLIS – The US Patent Office has issued a patent to Nortech Systems for its Flex Faraday Xtreme, a flexible printed circuit for transmitting high frequency signals while precisely controlling both crosstalk and impedance, minimizing electromagnetic interference, improving parallel transmission alignment, and increasing data density.

Patent No. 11,412,608 is based on the work of Michael Faraday in the 1830s that contributed to current understanding of shielding effects of what is now call a Faraday Cage. It was invented by Scott Blanc, principal engineer, and is the company's first patent in its technology portfolio. FFX adoption will ramp up through 2023 and will not have a material impact on Nortech's 2022 or 2023 financial results.

"Nortech's commitment to innovative technologies is key to supporting our strategic medical, industrial, and defense customers," said Jay D. Miller, chief executive and president, Nortech. "In highly complex and compact devices, the FFX is designed to provide the signal integrity necessary to support sensitive, mission-critical applications."



Nortech's patented HF flex circuit.

"With our patent of the Flex Faraday Xtreme (FFX), Nortech provides intelligent transmission lines that provide benefits over traditional micro coax cables in challenging applications," said Steve Czeck, senior director of engineering, Nortech. "FFX technology will be applied to meet customer requirements for size or weight constraints, or where harsh conditions exist."

Both FFX and the recent Active Optical Xtreme product launch are early steps in the company's long-term pivot toward serving strategic customers by building higher level assemblies that contain advanced technologies and solve difficult connectivity challenges. □

the Songdo High-tech Industrial Cluster in Incheon, which will become the Asia-Pacific production hub for high-impact electronics solutions of the Adhesive Technologies business unit.

India will try a strategy of parallel testing to speed up safety approvals for new electronic devices, a move that could boost device launch plans by the likes of **Samsung** and **Apple**.

Indium Corp. has opened a 24,000 sq. ft. expansion of its operations in Rome, NY.

LG Electronics is working to set up a manufacturing plant in Bangladesh.

Micron will invest about \$15 billion over the next 10 years in a new memory-chip manufacturing facility in Boise, ID.

Nordson Electronics announced **SmartTec Nordic** as distributor of **Asymtek** conformal coating and fluid dispensing products in Denmark and Norway.

Part Analytics announced an expansion of its relationship with Plexus.







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Chapter News

National: The PCEA Annual Meeting will take place Oct. 4 at the Santa Clara Convention Center, in conjunction with PCB West. All PCEA members in good standing are invited to attend. The 2023-24 board will be formally introduced at the meeting.



Scott McCurdy in August stepped down as Membership committee chairman. Mike Creeden takes over as Membership chair and will continue as vice chairman until board elections are finalized.

Scott McCurdy

"Please join me in thank-

ing Scott for all his past and current actions and dedication to service in getting PCEA chapters kickstarted over these past two years," said board chairman Stephen Chavez. "Scott will continue his involvement with chapter activities as chairman of the PCEA Orange County chapter, and on the executive board."



A new chapter leader orientation meeting was held Aug. 31, with members from Albuquerque, the Ozarks, Greater Boston and Denver among those attending. Mike Creeden and Scott McCurdy shared details

Mike Creeden

of PCEA, how to launch a chapter and the importance of culture in developing a sustainable chapter.

Orange County: A live Lunch 'n Learn is scheduled for Oct. 19. Stephen Chavez and Gerry Partida are putting together a presentation on "Best Practices" focusing on do's and don'ts, and the dialogue between a designer and fabricator.

Rio Grande Valley: The startup chapter had its second leadership meeting in September, and is hoping to have its first public event in the next few months.

Silicon Valley: Held in-person meeting on Aug. 4 at Siemens EDA in Fremont, CA, featuring a good presentation by Carl Schattke. (Schattke will also be presenting at PCB West next month.)

PCEA Issues Call for Abstracts for PCB East 2023

PEACHTREE CITY, GA – PCEA seeks abstracts for the upcoming PCB East technical conference, coming to the Boston suburbs next spring. The conference will focus on training and best practices for printed circuit board design engineers, electronics design engineers, fabricators and assemblers.

The three-day technical conference will take place May 9-11, 2023, in Boxborough, MA. The event includes a one-day exhibition on May 10.

Papers and presentations of the following durations are sought for the technical conference: one-hour lectures and presentations; two-hour workshops; and half-day (3.5 hours) and full-day seminars.



Preference is given to presentations of two hours in length or more, and no presentations of less than one hour will be considered.

Abstracts of 100 to 500 words and speaker biographies should be submitted to PCEA. Papers and presentations must be noncommercial in nature and should focus on technology, techniques or methodologies.

Submit abstracts to https://pcbeast.com/abstract-submission-guidelines by Oct. 28, 2022. No emailed abstracts will be accepted.

Presenters of accepted abstract(s) for the 2023 program will receive complimentary access to the online proceedings and a complimentary pass to the technical conference.

PCB West Announces Free Technical Sessions

PEACHTREE CITY, GA – Registrants for the PCB West exhibition this fall will gain access to nine free technical sessions, PCEA announced. The sessions take place on October 5 at the Santa Clara (CA) Convention Center, and run the gamut from advanced packaging to design, fabrication and assembly.

"Free Wednesday" leads off with a panel on "How Heterogenous Integration

Affects the PCB Industry," moderated by Phil Marcoux, a legend in SMT and advanced packaging. Heterogeneous is the latest branding effort to promote the assembly of dissimilar electronic components. In the past these could be called multichip modules, 2.5-D, 3-D and even "hybrid" assemblies. Heterogeneous inte-



gration makes the design function much more complex than is typical for electronic products, however, because many parameters can impact performance. This panel will address those complexities and how to solve them for printed circuit board designs.

The panel is followed by a pair of sessions that look at design and fabrication considerations of semi-additive processes and high-frequency materials, followed by the keynote address, "Augmented and Virtual Reality, the Next Computer Revolution," by Brian Toleno, Ph.D., Meta. Following a lunch on the show floor, which is free to all show attendees, the free sessions resume with a pair of sessions looking at emerging PCB technologies and common design errors caught at fabrication, plus a review of the PCB outline drawing.

Two talks on how to leverage bidirectional data transfer using the IPC-CFX and IPC-2581 formats to create a digitized "smart" factory fill out the afternoon schedule. Following the free sessions is a reception on the exhibition show floor.

Anyone who registers at pcbwest.com for the exhibition and free sessions by October 4 will receive free admission. Day of show registration for the exhibition and free sessions is $$25. \square$

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Hot Takes

- Global shipments of traditional PCs are forecast to decline 12.8% in 2022 to 305.3 million units while tablet shipments will fall 6.8% to 156.8 million. (IDC)
- North American EMS shipments in July were up 22.7% versus a year ago but fell 3.2% sequentially. (IPC)
- Passive component makers have seen their commodity MLCC and chip resistor inventory swell in the second half, the result of sluggish demand for consumer electronics products, and are eyeing automotive applications as a growth driver. (DigiTimes)
- Worldwide hardcopy peripherals shipments declined 3.9% yearover-year to 22 million units in the second quarter. (IDC)
- Smartphone shipments will decline 6.5% to 1.27 billion units in 2022, then rebound 5.2% in 2023. (IDC)
- Third quarter NAND flash wafer contract prices are falling and the pricing decline is estimated to balloon to 30 to 35% from the original estimate of 15 to 20%. (TrendForce)
- DDR5 contract prices, which fell as much as 20% in July alone, are expected to continue trending downward through the end of this year, according to sources at memory module houses. (DigiTimes)
- The worldwide semiconductor capital spending growth forecast is now 21%, down from the 24% growth forecast at the beginning of this year. (IC Insights)
- Total North American PCB shipments in July were up 4.5% compared to last year and dropped 24.9% sequentially. (IPC)
- Additive manufacturing sales are set to surpass \$41 billion by 2033. (IDTechEx)
- Electronic component market sentiment slumped to 86.0 in August, down 870 basis points sèquentially. The one relative bright spot is the expected stabilization of market sentiment in September as the outlook calls for a level of 88.4. Measurements below the benchmark level of 100 indicate negative sales growth. (ECIA)



Source: Institute for Supply Management, Sept. 1, 2022 . Figures above 50% indicate expansion.

US Reshoring Pace Sets Record

CHICAGO – US companies are bringing jobs back to America at a record pace, according to estimates from the Reshoring Initiative, a nonprofit that tracks reshoring trends.

American companies are on pace to reshore nearly 350,000 jobs this year alone, the highest mark since the trade group began tracking in 2010.

The firm cited changes in supply chains due to the Covid-19 pandemic, coupled with geopolitical issues between China and the US, and federal government incentives.

China, Mexico and Canada accounted for three-quarters of reshored jobs between 2010 and 2021, according to the Reshoring Initiative, with 44% coming from China. The trendline is up sharply: by contrast, US companies reshored 265,000 jobs in 2021, versus 6,000 in 2010.

According to the National Institute of Standards and Technology, transportation equipment, computer and electronic products, electrical equipment, appliances and components, and medical equipment are among the top industries reshoring to the US.

The firm notes that passage of the so-called Chips Act and the Inflation Reduction Act could spur additional reshoring due to new tax breaks and related incentives for companies to invest in domestic manufacturing.

| US ELECTRONICS EQUIPMENT SHIPMENTS (% CHANGE) | | | | |
|---|-----------|-------------------|-------|------|
| | MAY | JUN. ^r | JUL.* | YTD% |
| Computers and electronics products | 0.6 | 1.6 | 0.2 | 5.8 |
| Computers | -0.4 | 1.4 | 2.8 | -0.4 |
| Storage devices | 2.0 | 1.1 | -0.3 | 13.9 |
| Other peripheral equipment | 1.1 | 26.0 | 10.7 | 16.5 |
| Nondefense communications equipment | 1.3 | 1.4 | 2.3 | 10.7 |
| Defense communications equipment | -3.7 | 1.5 | 2.9 | 7.3 |
| A/V equipment | -11.9 | -15.0 | 10.9 | 32.4 |
| Components ¹ | 1.9 | -0.7 | 1.0 | 14.8 |
| Nondefense search and navigation equipment | -2.2 | 1.4 | 0.3 | 1.7 |
| Defense search and navigation equipment | 0.7 | -1.1 | -1.1 | 0.2 |
| Medical, measurement and control | 0.6 | 3.8 | -1.0 | 3.3 |
| 'Revised. *Preliminary. ¹ Includes semiconductors. Seasonally a Source: U.S. Dept. of Commerce Census Bureau, Sept. 2, 2022 | ıdjusted. | | | |

| KEY COMPONENTS | | | | | | |
|--|------|-------|------|--------------------|-------------------|--|
| | MAR. | APR. | MAY | JUN. | JUL. | |
| EMS (North America) ^{1,3} | 1.40 | 1.36 | 1.35 | 1.59 | 1.39 | |
| Semiconductors ^{2,3} | 23% | 21.1% | 18% | 11.9% ^r | 7.3% ^p | |
| PCBs ^{1,3} (North America) | 1.04 | 1.04 | 1.05 | 1.03 | 0.98 | |
| Sources: ¹ IPC, ² SIA, ³ 3-month moving average, ^p preliminary, ^r revised | | | | | | |

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Fit to Print

Additive manufacturing might not be ready for prime time, but it's making inroads.

SOMETIMES I FIND myself walking around the shop floor asking, "Why do we have all this very expensive equipment? There must be a simpler, cheaper way to make a printed circuit board!" And yet, despite phenomenal technological strides, our industry still uses the same basic manufacturing processes since the earliest days of circuit board production: drill – image – plate – press – repeat – then route.

Observing so many different processes, simple logic might make you think printing conductive ink would have replaced plating processes long ago. Yet while printed electronics has advanced considerably, it is not ready for prime time for all applications. (Full disclosure: I spent a half-dozen years earlier in my career in the paperboard and flexible packaging industry, experimenting with various types of inks printing on materials that included cardboard, kraft boxboard, film, foil, and coated and uncoated paper.) Web-toweb printing of conductive inks can accomplish much, but the circuit board industry still primarily requires producing in sheet (panel) form to deliver the parts customers require. Moreover, conductive inks provide rather limited current capacity.

The world of 3-D "printing" may offer an opportunity to shift from so many manufacturing processes to fewer – and possibly simpler – approaches. Several years ago, I witnessed college students building a toy car via 3-D, using conductive ink to create a basic circuit board on the car interior, which was powered by a battery-driven electric motor. Deploying 3-D printing to create the car body and then printing conductive ink to create the circuitry on the car body, they built the car and circuitry far more simply than traditional processes would have required. That was a very primitive example, however, compared with applications that require dense circuitry, or complex builds including sequential lamination for a complex multilayer, tight impedance control, etc. Advances in 3-D printing have been more than impressive, but while the ability to have vias formed on, say a 45° "horizontal" angle, rather than on the current direct 90° "vertical" angle, opens the mind to interesting design opportunities (and challenges), the constraints of consistency, current capacity and component placement remain.

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While these two very different technologies cannot fully replace the printed circuit board today, they are nibbling away at the fringes. When any technology in any industry begins to make inroads, show promise and generate revenue at the expense of existing mainstream technologies, it must be considered either a passing phase, or a disruptive, paradigm-changing opportunity that should be closely followed.

Both printed electronics and 3-D printing have one major thing in common: They require a complete reset – a total mindset shift – regarding how a "circuit board" is envisioned.

In the case of printed electronics, engineers design, application and manufacturing - must rethink both shape and process. Web-to-web printing fits best in high-volume applications requiring flexibility. (Think ribbon cables, flex circuitry and volume.) The challenge for many engineers is considering which applications are indeed high-volume and require flexibility. For other engineers, it's thinking about the packaging that might go on a printed circuit and how to build up "layers," as it were, to replicate a traditional circuit board. Remaining focused on the existing paradigm of traditional circuit board design and assembly techniques, however, may well be the reason printed electronics is not yet a larger segment of the industry. The mental leap to reengineer based on different attributes, materials and processes most certainly is needed to truly take advantage of a very different, new technology.

If engineering minds have not been able to wrap themselves around how to integrate printed electronics into mainstream electronic circuitry applications, or design to take advantage of the unique characteristics of printed electronics, imagine how long it will take for others to fully embrace and harness 3-D printing in the electronics industry.

If conceptualizing printed electronics is difficult, doing the same with 3-D printing will be exponentially more so. Printed electronics requires rethinking twodimensional design concepts. 3-D printing, however, demands thinking and designing in three dimensions. That means breaking away from physical limitations ingrained with two-dimensional product design and instead imagining the "what if?" the lack of physical constraints enables. For instance: a structure where each layer can be designed and built with variable thicknesses; designing a product where the product itself is the circuitry; or, in the same process, assembling and fabricating a product in which components are truly embedded.

To truly replace the status quo, a disruptive technology requires users to break from current thought paradigms and embrace the scary edges of design,

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REQUIRES COMPARISONS

THAT CONSIDER

ALL FACTORS THAT INFLUENCE

VENDOR PERFORMANCE."

Relying on a single source is a recipe for failure.

"GOOD, FAST AND cheap ... pick two" is an old maxim that applies - to a degree, anyway - to the printed circuit board industry.

The implications, of course, are that if it's fast and good, it's going to be expensive; if it's good and cheap, it will require lots of time; and if it's cheap and fast, the quality will be poor.

PCB buyers should keep this in mind when choosing vendors and avoid relying too much on one supplier if they want good quality boards delivered on time and at a reasonable price.

While PCB manu-

facturers use basically the same equipment, raw materials and processes to build boards, it is ultimately their business philosophy that differentiates one from another.

There are ven-

dors that specialize in prototype or quickturn orders of several pieces in as many days. There are others that want only high-volume orders with a definitive schedule. Many PCB manufacturers focus

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quantities required, also known as high-mix, low-tomedium-volume production. Even if your firm has very specific needs within that range of production strategies, you should have

on producing multiple part numbers with a variety of

at least two suppliers with varying approaches and strengths to ensure you can consistently meet customer expectations.

Some PCB vendors have plenty of well-trained staff to support their customer base, whether it's in front-end and process engineering support, production, quality assurance or shipping. Many are struggling, though, to hire and retain the staff required to successfully run a board house.

In today's challenging workforce environment, even facilities with the newest equipment and largest production capacity are still only as good as the people behind the machines or on the other end of the phone. Personnel problems affect not only the quality (good)

but timely delivery (fast) of your circuit board orders.

And that brings us to the "cheap" segment of the old saying. While PCBs are custom-made items, manufacturers pay similar costs overall to build them. But supplier pricing will vary, depending on their overhead expenses.

Just because a vendor has the latest equipment or more personnel (and therefore more overhead) does not necessarily mean its prices will be higher in the long run. A supplier with cost-effective and efficient processes in place to ensure timely delivery of quality

> product will be able to offer PCB buyers a lower total cost of ownership.

> Higher yields mean a competitively priced PCB, ontime deliveries and a reduced chance of short shipments or quality problems.

> A short shipment from the board shop means a possible delay in boards hitting the production floor, or a chance for double assembly setups because of a customer's need to have some product

on hand now rather than later.

Receipt of poor-quality PCBs could result in poorly assembled boards, costing your company the components, the labor to make those assemblies, and revenue from not making those deliveries in the first place.

And let's not even mention the possibility of field failures, as well as the analysis time required for those failures and the hit to your company's reputation.

My intent is not to belittle any company's current vendor base. Instead, I'm encouraging you to fully evaluate price versus cost - again, that total cost of ownership. Navigating today's PCB supply challenges requires an apples-to-apples comparison that considers all factors that influence vendor performance.

And regardless of how good a particular vendor may be, board buyers should not put all their eggs in one basket. It is best to have more than one supplier.

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Stopping the Spread of Customer Service Mediocrity

Teams are overworked and on the edge. How to combat the slide.

"DO YOU HAVE A

TOP-DOWN VISION

OF WHAT

CUSTOMER SERVICE

SHOULD LOOK LIKE?"

ONE OF MY favorite bosses pointed out that a contract is only as good as the intent of the parties who sign it. Yes, you can haul a party in breach of contract into court or arbitration, but the resolution rarely completely fixes the issue, and in many cases parties breach agreements with no consequences. Nowhere is that more evident than in today's semiconductor industry. You'll

get parts when they arrive even when there was a commitment for an earlier date; they may cost more than the agreed-upon price; and the order is noncancellable regardless of how many previously agreed-upon terms change. In short, one party has no intent to adhere to the terms of its agreements, and market conditions will likely enable that behavior to continue indefinitely with no consequences.

This type of environment

can be as contagious as the most recent Covid variant. Customer service and honoring commitments are sliding across the board. Last month, I listened to a gate agent lecture a 6 a.m. flyer who foolishly thought she could get to her destination in a single day, saying the airline wasn't obligated to put her on a different airline until she had been stuck in transit for 48 hours. Separately, three contractors I called for glass cutting informed me that they couldn't commit to a time for quoting or delivery but would a call an hour before they arrived. One finally did call back a week later and got the job. The other two still haven't called back. When all competitors in a market are getting away with behaving badly, mediocrity thrives.

The converse is also true. When all competitors in a given market behave badly, average customer service stands out. Companies can distinguish themselves simply by returning phone calls, working through issues as rapidly as possible and doing their best to honor commitments even when market pressures make follow-through more difficult. In short, noticeable customer service in this environment really means meeting normal expectations.

Like Covid, however, mediocrity spreads easily through overworked teams who see examples of poor customer service everywhere. The airline gate agent I saw last month was taking joy in schooling this unhappy traveler in the new rules, most likely because she had been yelled at by passengers so often she now saw reschedules as an adversarial relationship rather than a customer service opportunity.

How do you stop the spread of mediocrity in your organization? To start, acknowledge the drivers of mediocrity. In the EMS industry, market factors are creating an environment where customers are regularly disappointed. Those factors are outside the control of the EMS staff members interacting with customers. That

said, those representatives can control some issues, including:

• Speed of returned phone calls or emails (even when the reply is "I'm still working on getting an answer.")

 Mistake-free execution of internal processes

• A commitment to transparency and fast delivery of bad news

 Attention to detail in communications among team members and customers

- Creativity in development of options in situations where customer requirements can't be met
- Empathy in situations where customer requirements can't be met
- Best efforts to honor commitments where possible.

It's also important to establish a top-down vision of what customer service should look like within the organization, with metrics for problem resolution cycle time, definitions of what extraordinary measures staff can take to resolve a bad situation, and clear expectations on appropriate behavior in dealing with customers.

Training is helpful as well. The issue I observed at the airport escalated because of the gate agent's attitude. While transactional analysis is no longer in vogue as a management training technique, its simple lessons are very relevant today. The attitude we exhibit when we address people drives the quality of the transaction, and most people interact in parent, child or peer (adult) states. When someone exhibits the attitude of a parent talking to a child, it will drive a rebellious child response. When the attitude conveys a peer-to-peer discussion of a business case, the response will convey a similar peer-to-peer calm approach. And when the response is a frustrated child ranting about out-of-control situations, it will drive a parent response. Helping employees understand their individual role in delivering good customer service, even when suppliers are not, helps inoculate against the spread of mediocrity and pays dividends in customer tenure when markets return to normal operations.

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Electrostatic Discharge: As Old as the Hills and Still Something to Consider

Grounding and routing tips for sensitive parts.

YEARS AGO, I set out to become a world-famous PCB designer. The journey, however, took much longer than that. Starting near the beginning, the second lesson I learned about electronics came on the first day on the job in electronics. I bet you're wondering what I did in electronics on my first day.

My contribution was to put completed printed circuit board assemblies into pink bubble wrap bags. The bags were sealed with resealable ESD warning stickers and placed in individual boxes. Labels on the boxes had blanks for the

information, which was copied from the board to the label. Completed sets of eight boxed boards were again boxed in a larger box, which was labeled with the content part numbers, revisions and so on.

As an aside, the next stop for the boxes was the shipping department and, finally, phone company offices around the country. Called offices, they were more of a precursor

to today's data centers. The build-out was a result of the US government forcing the phone company to break itself into regional businesses.

What our equipment did was allow 384 voice calls on T1 cable originally built out to carry 24 such lines. The T1 interface was one of the more interesting looking cards, with a lot of passive parts. Whether it was a modulator/demodulator board, or the more expensive A to D converter and so on, they all had pink bags and orange stickers as part of their final prep.

By now, you've guessed that the second lesson I learned was about electrostatic discharge (ESD). We had to watch a film and tolerate constant reminders to plug our wrist straps into the bench before we began work. Larger areas where the equipment racks went together had special floor mats and shoe straps. Earth ground was achieved with an actual stake in the concrete floor to create a common point ground. It was a normal function to prepare the workspace before working on static-sensitive products.

One of the tenets of the system was regular verification of compliance with the established ESD processes. Auditors could show up at any time with their clipboards and checklists as part of ISO certification. Having a certified factory is one thing. The driving cause was to reduce scrap and its erosive effect on business results. Profit matters. No matter who you were, you needed a smock and proper awareness to go into the ESD-safe zones.

It was the time of very large-scale integration.

VLSI was the buzz phrase that implied hundreds of thousands of transistors on a single die. The six-digit number of gates is now a nineor ten-digit number that takes about the same amount of space. Integrated circuit geometry has been reduced by orders of magnitude, to the point of vanishing entirely.

Seriously, our eyes can only work with visible light that comes in wavelengths between 380 and

700nm. The geometry of early microcontrollers and microprocessors wasn't even measured in nanometers, as we see on today's devices. "Deep sub-micron" only hinted at what was to come. Generation after generation, the tiny features have always required protection. Electrostatic discharge is the same threat today.

Cause and effect: magnetism from an arc. Random high-voltage spikes generate rapid change in the electromagnetic fields. The system sees that as a huge noise spike, in addition to the potential damage done by the voltage. Reactance is the natural byproduct, and it has a wider reach than the tiny arc of electricity that sets it in motion. The good news is we have a few tools to keep our electronics safe.

Ground the connector's body to a perimeter seal

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FIGURE 1. Two different symbols indicate ESD zones, with the hand being the more common. (Source: Compliance Signs)

ATTENTION

STATIC CONTROL AREA

ESD PROTECTION

REQUIRED





JOHN BURKHERT

JR. is a career PCB

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in military, telecom,

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|-----------------------|-------------|
| Via in Pad Expedited: | 3 Days |
| HDI Standard: | 25 Days |
| HDI Expedited: | 5 - 12 Days |
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People are Staying Away from Work after Covid. The Next Industrial Revolution Wants Them Back.

Industry 5.0 promises a more humanistic approach to production.

IT HAS BEEN over a year since governments began lifting restrictions on citizens' movements to resuscitate their economies, and some 18 months since the Ever Given blocked the Suez Canal in March 2021, sending global shipping activities into spasm.

But supply chains today are in critical condition. Assets and materials are in the wrong places around the world, factories are struggling to resume normal activities, and large numbers of people are simply not working, having either not returned to work after the pandemic or become part of what is now termed the Great Resignation, or the Big Quit. Some 20 million workers around the world, in the largest and most advanced economies, have left their posts, citing factors such as burnout, pressures at home and isolation, and feeling unvalued by their companies.

This is not the "new normal" we all expected. A major shift is taking place as peoples' attitudes, desires and priorities have fundamentally changed.

Industry 4.0 and the previous automation-centric revolution have each sought to remove humans from production activities, to raise productivity by moving beyond our own limitations: our tendency to make errors, relatively short attention span, our vulnerability to illness.

In factories, humans certainly cannot compete with machines, and a strong case can be made for a similar transformation in the logistics sector. Here, digitalization including technologies like smart pallets and smart containers can deliver similar efficiency gains by improving visibility, which helps supply-chain partners understand each other's needs and plan accordingly. As the consequences of Covid continue to play out in supply chains, it's time for Logistics 4.0.

Despite the chaos and difficulties, however, markets such as IT and infrastructure have no shortage of inventory. Factories have been busy responding to short-term demand spikes during the Covid crisis as companies and employees have adapted to changing working patterns and the work-from-home phenomenon, in particular. We are now seeing stocks of these products have become so high it will take some time for the excess inventory to dissipate. It's reminiscent of the communications industry crash of the early 2000s, when companies produced uncontrolled quantities of infrastructure equipment to fuel the internet revolution. They based their activities on wildly inaccurate forecasts, and when this was realized, the party suddenly stopped.

Well, now again, we are seeing excess inventory exposing manufacturers to unwanted costs in terms of materials, energy and manufacturing capacity they have expended. The waste is compounded because while our factories are building unwanted products through bad forecasting, they cannot build those that are needed to tackle the challenges of the future.

Could digitalization help with this problem?

Logistics 4.0 proposes to replace the current spreadsheet-based and siloed supply chain and logistics arrangements with a more informed and properly directed approach directed by AI and not subject to human errors and inattention.

Meanwhile, Industry 4.0 is moving over for Industry 5.0, which could be a complete paradigm shift: a rethinking of the entire purpose and priorities of our corporations. While the industrialists' view of Industry 5.0 is about bringing AI and machine learning into manufacturing processes, the EU has stepped into the debate by defining Industry 5.0 in terms of humancentric, resilient and sustainable qualities as three guiding principles. It's a vision that seeks to define success less in terms of corporate growth and customer satisfaction, and instead prioritizes worker fulfillment and protecting the world's resources. It reflects a desire to move away from minimizing the negative impact of business on people and the planet - working toward net zero - and instead ensure businesses of the future have a positive impact.

Putting people back in the picture is good for all of us – and necessary, because machines cannot solve all our problems on their own. Certainly, in factories, their productivity provides the means for economic success.

On the other hand, when used to support planning, their help in directing our activities to make only the things we need, when we need them, provides the key to future sustainability. Perhaps most importantly, they bring the possibility to predict the unpredictable: black swan events that are, by definition, rare and beyond human anticipation. (It's worth noting that Nassim Nicholas Taleb, who articulated the black swan theory in 2007, has said that the Covid crisis was no black swan; that such a pandemic had, indeed, already been predicted and governments advised to plan for its inevitability.)

While some may believe we can rely on human intelligence to protect ourselves against the apparently obvious, AI gives the ability to foresee unthinkable

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What's Wrong with My Stack?

The IPC slash sheets simplify communicating design intent.

IT IS COMMON to see a drawing with a stackup that identifies all the materials used to build a board. The designer selects foil and dielectric types and thicknesses, and in many cases may even call out glass weaves and specific brands. And why not? It is their design, and it is natural to want to control it. As a designer, it makes sense to be as clear and as complete as possible, right?

Specifying a particular material is required in some instances to get a particular performance attribute. In many cases, however, performance levels can be achieved with a variety of material selections.

It is common to want to call out a specific prepreg because it has been modeled to achieve certain signal integrity performance. Often several materials, however, can accomplish the same result. Sometimes the manufacturer can offer a solution that helps manage cost. In other cases, the manufacturer may need to use a different glass weave/resin combination to achieve a good, void-free lamination. This can impact dielectric thickness between layers and the resultant impedance lines.

IPC has a series of material specifications that categorizes materials into specific buckets using slash sheets to differentiate among materials and their performance characteristics. Notably, the rigid laminate and prepreg specification, IPC-4101, has many slash sheets covering polyimide and epoxy resins, and more. In many cases, the designer will be best served by defining materials based on slash sheets and not specific brands. The reasons for this are numerous.

Most manufacturers have qualified a series of materials. The manufacturing partner might not have qualified a certain specified brand. The designer will then be facing a drawing change, or require the fabricator to use a new material set and validate its process for the first time on the designer's part.

If the part requires UL certification, the manufacturer may not have submitted that specific material or combination of materials to UL as part of its UL listing. Again, this might mean a drawing change, or charges to have the particular construction tested and approved by UL.

Rigid-flex throws another wrench in the works. Rigid-flex uses no-flow prepreg in order to control resin flow and keep it from the flexible regions of the part. As a result, options are limited, as not all types and brands of prepreg are offered as no-flow. Calling out one of those materials will drive an exception request and drawing change. Also, with no-flow prepreg, many are limited to just a few weaves, most commonly 106 or 1080 types. The manufacturer will have a series of no-flow prepreg materials it has qualified and characterized. Take advantage of its experience here.

For example, even polyimide prepreg is not that simple. IPC-4101 slash sheets for polyimide laminate and prepreg really number just three: /40, /41 and /42. It may be quite common that a manufacturer's preferred rigid laminate is qualified to one slash sheet and its no-flow prepreg certified to another.

As the name implies, no-flow prepreg does not flow as standard-flow prepreg does. As a result, the manufacturer has different rules for the amount of prepreg needed between layers, depending on foil thickness and copper coverage on each layer. This can drive use of prepreg sheets that might be a bit thicker than what the designer might expect, or maybe multiple thinner sheets.

Some rigid-flex boards have more than one type of prepreg in the same stackup. This is especially true when using HDI fanout layers in combination with microvias. These designs are typically sequentially laminated, using no-flow prepreg in the first lamination but possibly standard-flow for subsequent laminations. This can open the design to more possibilities for the outer laminations.

Additionally for rigid-flex, some prepreg materials laminate at higher temperatures than others. This can have a damaging effect on some lower-temperaturerated materials in the stackup, such as the coverlay and flexible bondply. Sequential laminations can magnify this effect with multiple high-temperature excursions.

Where possible, then, use of IPC slash sheets is recommended to signal design intent and leave some room for the manufacturer to navigate the design and fabrication. If it helps to soothe concerns, ask the manufacturer to share its final stackup to confirm the board will be built to match the drawing.

Once the circuit is qualified, it becomes a fabrication of record. There should be no issues with lack of design control moving forward. Good manufacturers will not change material selection without the designer's prior knowledge and approval.

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NICK KOOP





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7 Key Drivers of Change in PRODUCT DESIGN Today

A study of nearly 300 companies reveals shifting approaches to hardware and software. **by JOHN MCMILLAN**

How are companies addressing digital transformation, everincreasing design complexity and the effects of a post-pandemic world on tech companies amid the so-called "Great Resignation?" This year, our technology-led analyst firm, Lifecycle Insights, conducted an in-depth independent study to learn more about and better understand what the coming years hold for engineering. The survey collected responses from 274 companies that design products across all major industries, with revenues ranging from \$1 million to over \$5 billion.

To say the Covid-19 pandemic is having lingering effects on how companies are operating in the "new normal" of a postpandemic world is a tremendous understatement. Technology continues to advance rapidly in a time of historic levels of digital transformation. Evolving markets for electric vehicles, IoT devices, 6G, miniaturization, and more are increasing the need for systems and product design flows and tool capabilities without pause. Digital twins, artificial intelligence (AI) and augmented reality (AR) are terms we use daily, and product and systems

design flows developed to accelerate firstpass design success are continually evolving.

Lifecycle Insights' 2022 "Digital Transformation on the Engineering Executive's Strategic Agenda" consisted of more than 60 questions focused on several key themes. They included:

- Product development improvement efforts,
- Developments that address design complexity,
- Attitudes toward cloud-based applications and investments, and
- Improvement efforts planned to achieve product development goals.

Follows are seven key drivers of change that the survey revealed.

Driver 1: Companies are hiring – and buying software. Despite the shift to remote work over the past two years, our survey revealed 52% of companies are purchasing new software solutions to address design complexity. And, amid the Great Resignation, 57% are hiring new personnel.

To support digital transformation, companies are acquiring new computer hardware and changing their processes. Tools for both product and application management – along with personnel to develop and manage those tools – are in demand. In fact, 41% of companies reported that changes to organizational structures and roles were part of their effort to improve product development.

Driver 2: Simulation and MBSE. It came as no surprise that 56% of companies surveyed are using simulation earlier in development (**FIGURE 1**). Downstream simulation and verification, which have begun to "shift left" over the past decade, are now becoming integrated capabilities of a full-flow concurrent design platform. Improvement efforts also include a 53% movement



FIGURE 1. Technology process trends. (Source: Lifecycle Insights)

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toward a model-based systems engineering (MBSE) approach and the addition of more automation to design processes, all driven by time-to-market and pressures to lower product costs. Growth in multi board product design platforms, for example, has emerged as a clear trend. These platforms improve the entire design process by considering and automating simulation and analysis from product inception to manufacturing.

Driver 3: Cloud-based engineering applications. When asked what best describes their company's official attitude toward cloudbased engineering applications, 63% of respondents are either already in the process of transitioning to cloud-based applications, exploring their options or planning to move to cloud-based applications. In fact, 24% stated that a vast majority of their engineering solutions already run on private or public cloud services. These companies are moving fast, with 49% targeted to be supporting cloud solutions within the next 24 months. These decisions are aimed to help their companies lower upfront costs, support remote accessibility for employees and collaborators, reduce overhead, and ease integrations with other cloud solutions.

Driver 4: Increasing number of electrical endpoints. Make no mistake, the average number of electrical endpoints – that is, circuit boards, sensors, antennas, etc. – in products is increasing. In fact, 35% of our survey respondents reported seeing between 10 and 25 electrical endpoints in their products, while 45% reported that their products are seeing from 26 to more than 200 endpoints. This increase in endpoints over the past two years has impacted signal and power distribution systems, increased the number of network signals, and raised the bandwidth demand required to support communications. As a result, 80% of companies surveyed reported they have formally invested in efforts to improve the development of their electrical power and signal distribution systems.

Driver 5: Security concerns. Whether it be from apps on connected devices, desktops, or software running on cloud applications either on-premises or off, security concerns are

distribution systems? using new software solutions 63% 50% 31% onihip by an executive (VP or higher) Assignment of a dedicated leader 8 31% 19% Explicit, public, and measurable objectives 38% their chargers to processes and activities Hiring new personnel to support the change 50% Changes to organizational structures and roles 31% Tested with a priot program 19% LIFECYCLE INSIGHTS

In the past two years, which of the following has your company formally invested in to improve the development of electrical power and signal



driving companies to improve engineering processes for most companies. Software on a public cloud was of greatest concern.

That said, cloud and high-performance computing ranked as most important to companies' future improvement efforts. Where does security stand when it comes to making purchase decisions for engineering solutions? Well, 48% reported it was a moderate or top influencer and are exploring ways to improve security based on cloud company competencies.

Driver 6: On-premises or outsource? Although circuit boards are generally designed internally, it was interesting to learn that 20% of companies surveyed have been designing circuits on-premises for five or fewer years. In addition, we found that 33% of companies are outsourcing the systems engineering for their products.

Complexity – in terms of innovation, technology and new product introduction (NPI) – is driving companies to improve their engineering efforts. To address supply chain resilience, companies that historically outsource component selection are looking at ways to bring those services in-house so supply issues are addressed the moment they are encountered, to accelerate decision-making. Although the top barriers to achieving improvement benefits were lack of budget support and unclear objectives or metrics, 52% of companies surveyed stated they have achieved benefits from their improvement efforts.

Driver 7: Design improvement efforts. In addition to simulation, more than half the companies surveyed revealed they are also investing in processes that improve and accelerate design. Those efforts include increasing design reuse circuitry, developing better architectures for multi board systems, implementing earlier design for manufacturability (DfM) checks and adding more automation to their design processes. In addition, companies are focusing more intensely on product lifecycle management (PLM) and application lifecycle management (ALM) to ensure products are being developed and designed with regulatory and compliance requirements in mind. From adopting agile principles to best practices, companies are investing in platforms that help their teams manage requirements through systems development processes to reduce design cycle time and improve quality.

> These seven drivers provide key insights into the ways that company executives have pursued efforts to address growing design complexity and the impacts of remote work. The study showed a strong correlation between timely investments in digital transformation and measurable improvements in performance. That said, from year to year, the initiatives that delivered benefits over the past two years are not guaranteed to deliver again over the next two.

> JOHN MCMILLAN is a senior industry analyst for Lifecycle Insights (lifecycleinsights.com), with more than 30 years of expertise in electronics, ECAD design and the EDA industry, where he is dedicated to research that helps executives realize value from tech-led initiatives without disruption; john.mcmillan@lifecycleinsights.com.

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MICROVIA RELIABILITY TESTING Utilizing D-Coupons to Understand Best Design Practice

A study of the influence of design parameters that impact success. by KEVIN KUSIAK and SCOTT BOWLES

A microvia is defined in IPC-T-50M as "a blind structure (as plated) with a maximum aspect ratio of 1:1 when measured in accordance with **FIGURE 1**, terminating on or penetrating a target land, with a total depth (X) of no more than 0.25mm [0.00984 in] measured from the structure's capture land foil to the target land."



FIGURE 1. Microvia definition per IPC-T-50M. (Note: X/Y = microvia plating aspect ratio, with X < 0.25mm (0.00984") and aspect ratio < 1:1.)

Advantages to using microvias in PCB design include but are not limited to signal integrity, routing real estate, and pin escape. The most common reason that drives designs to use microvias is the need to escape the pins of a fine-pitch part. As pin pitch on an integrated circuit (IC) is reduced, the design starts to approach a threshold where mechanically drilled vias are not possible. When this happens, other routing solutions such as microvias are required. Use of area array components with a pitch of less than 0.8mm will very likely require the use of microvias to escape the pins of the component, and these components are becoming common in high-reliability electronics such as space hardware and military/defense products. Another advantage is microvias can be used to make connections between two adjacent layers, thus saving a significant amount of routing real estate by not requiring a via that spans multiple layers as a mechanically drilled via typically would. And microvias help with signal integrity of high-speed digital

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or radio frequency (RF) circuits. At higher frequencies designs can be very sensitive to signal reflection caused by via stubs, and microvias may be required to mitigate signal integrity issues.

Once it is determined microvias are necessary, many design decisions remain to be made. On the lower complexity end of the spectrum the design may require only one layer of microvias spanning from the outer layer to the next layer in. On the other end of the spectrum the design may require microvia structures spanning every layer, also known as Every Layer Interconnect (ELIC) or All Layer Via (ALV). While it would be very difficult to capture the entire design spectrum, the more common design parameters for current aerospace designs were tested and the next section covers those design details.

Coupon/Panel Design

A 12" x 18" panel of test coupons was designed to test and examine various microvia structures. Conductor Analysis Technologies (CAT) has a web-based interface for coupon generation¹ to simplify the creation process; however, this panel was designed by hand, leveraging a previous design created by a coworker. The design calls out polyimide per IPC-4101/40, /41 or /42, currently the most common requirement for our designs. In the future other material may be explored, but for now all panels were built using polyimide. The panel contains 54 D-coupons, 37 coupons with isolated via structures for cross-sectional evaluation (similar to IPC A/B coupons and, for simplicity's sake, they will be referred to here as A/B coupons) and two peel strength coupons, with embedded microvias, to be used as test strips. **FIGURE 2** shows the test panel design.

Each D-coupon contains two daisy chains of vias with plated through-hole (PTH) connections on each end of the chain. A press-fit header is assembled onto the coupon, which enables a Kelvin (or 4-wire) resistance measurement to be taken, for precise resistance measurement of the chain. Each coupon in the design represents different variations of microvia size and pitch. Most daisy chains consist of the transition between two different via spans (e.g., 1-2 and 2-3); however, a



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few daisy chains utilize almost all via spans and the daisy chain traverses the top to the bottom of the board (the 3-4 microvia is the only via span left out of these daisy chains). The size and pitch remain constant within each daisy chain, and through the numerous D coupons on the panel, many variations may be examined.

The goal was to straddle microvia diameters and aspect ratios representative of current design practices, but to also use design parameters that start to push the limits of what is considered good design practice. Microvias of 5, 6 and 7 mil diameter were used (to be clear, this is the diameter of the laser-formed microvia at the capture pad), and all microvias were copper-filled. The design supports a constant dielectric thickness (approximately 3.8 mils), which means multiple aspect ratios can be examined by altering the microvia diameter alone. A 3.8-mil dielectric plus 0.5oz. foil is about 4.5 mils thick, and for a 5, 6 and 7 mil microvia this yields aspect ratios of 0.90:1, 0.75:1 and 0.64:1, respectively.

Microvia structure pitch was varied between 0 and 20 mils, in increments of 5 mils. Note the pitch between vias is measured center to center, so a via that has a 0-mil pitch to another in the vertical plane can also be referred to as a stacked via structure. The microvia pad size used was 14 mils, so microvia transitions on a 5- or 10-mil pitch will have overlapping pads; at a 15-mil pitch the pads are no longer overlapping.

FIGURE 3 illustrates the transition between the 1-2 and



FIGURE 2. Panel design.



FIGURE 3. Layer 2 of a representative D coupon.

2-3 vias in the bottom chain (15 mils in this case), and the top chain shows the transition between one staggered structure pair to the next. Each of the two chains are on the same grid (50 mils), with just over 100 via transitions per chain. Several coupons have a larger grid pitch (150 mils), however, meaning the number of via structures and transitions in the chain is reduced. The purpose of this was to determine if the number of structures in the chain had a major impact on resistance variation of the chain during testing. If each structure contributes a resistance delta to the overall measurement, the theory is that more vias in the chain would increase the probability of failure. The more transitions, the greater the resistance delta between each thermal cycle, thus making it more difficult to meet the 5% resistance change threshold required by IPC-TM-650 method 2.6.27B.² The theory and the data did not correlate: all the coupons on a 150-mil grid passed thermal stress testing as did all their counterparts on a 50-mil grid.

When using D-coupons for acceptance testing, it is important the coupon be designed properly by ensuring the via structures are the same as in the board design. If designed properly and tested to IPC-TM-650 method 2.6.27B, the D-coupon is an excellent tool for testing the robustness of the via structures to withstand the thermodynamic effects caused by convection reflow assembly. The D-coupons are ideal for via reliability testing because they can represent a variety of propagated via structures and transitions, the same as the board design. The

> electrical resistance of the via structures is monitored while undergoing a representative reflow profile, which is the harshest environment the PCB will see in its lifetime and when plating separation is most likely to originate.

Panel Fabrication

Two PCB fabricators were selected as partners on this effort, henceforth referred to as Fabricator A and Fabricator B. Early in the project, each fabricator supplied input on the design to ensure all interested design parameters were captured. A statement of work was created for each fabricator to flow requirements that deviated from standard build requirements such as:

 Pulling coupons from the panel after certain steps in the fabrication process

Recording chemical bath analysis results

 Supplying monthly results for tensile strength, elongation and purity testing

Adding a TMA coupon for T_g testing of the base material.

These data were collected to aid in failure analysis or process investigation, if needed.

Two panels of coupons were procured from each fabricator. Fabricator A had several D-coupons fail during electrical testing per IPC-9252B, which is part of the standard performance specification testing PCBs are subject to for lot acceptance. Due to these failures they had to fabricate third and fourth panels. Between the four panels



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FIGURE 4. Example of IPC-defined limits for a reflow profile (IPC-TM-650, method 2.6.27B).



FIGURE 5. IPC-TM-650, method 2.6.27B results after 12x cycles.



FIGURE 6. IPC-TM-650, method 2.6.7.2C results after 100x cycles.

fabricated, they shipped us all D-coupons that passed electrical test. Some coupon positions yielded 0%, and some yielded 100% from all four panels. The total number of D-coupons delivered was 152 of 216 (54 D-coupons per panel x four panels). Fabricator B had to scrap panels 1 and 2 in their entirety, due to a material stackup issue, but were able to ship 108 of 108 D-coupons from panels 3 and 4.

Coupon Testing

D-coupons were sent to Conductor Analysis Technologies for thermal stress and thermal shock testing as outlined below. CAT tested 108 coupons from each fabricator. Since Fabricator A delivered more than 108, the coupons were sorted and prioritized, starting with coupons containing the smaller diameter and tighter pitch between the transition.

Convection reflow assembly simulation. Thermal stress testing simulates thermodynamic effects caused by the assembly process, specifically the reflow process, which is the harshest environment the PCB will experience and when microvia cracking is most likely to originate. Test method 2.6.27B is referenced in the special requirements section (3.10) of IPC-6012E³, and is a required conformance test for any PCB containing microvias built to the Space and Military Avionics Applications Addendum (IPC-6012ES).⁴ Testing was performed on a D-coupon, as previously described. Both tests described in this section require D-coupons to be baked for moisture removal for a minimum of 6 hr. at 105° to 125°C. The D-coupon is then thermally stressed through a representative reflow profile simulation, with upper and lower limits defined in the test method. FIGURE 4 shows the upper (red) and lower (blue) limits for the 260°C reflow profile. The test method also defines 230° and 245°C reflow profiles. The intent of the multiple reflow profiles is to give the end-user options to test with a reflow profile that is representative of what the deliverable boards will be subjected to during assembly. Most products built at the authors' company will experience a tin-lead reflow profile with a peak temperature near 230°C. Hand assembly and rework are very common processes, however, and these temperatures are very difficult to account for when trying to simulate the entire assembly process of a PCB. While we may not be able to encompass all assembly processes the PCB may be subjected to, testing to the higher 260°C reflow temperature profile provides additional margin to give confidence the PCBs will also survive a reasonable level of hand assembly or rework processes.

The IPC test method requires the resistance of the daisy chain be continuously monitored during the entire reflow cycle and consists of at least one reading per sample net every second while the coupons are thermal-cycled. The minimum number of required

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FIGURE 8. Fabricator A test data organized by via pitch.

TABLE 1. Testing Results Sorted By Via Diameter

| Vie | Electrical Continuity Test | | | Thermal Stress | | | Thermal Shock | | |
|----------|-----------------------------------|-------------------|--------------|----------------|----------------|--------------|----------------|----------------|--------------|
| Diameter | Coupons Tested | Coupons Passed | Passing % | Nets Tested | Nets Passed | Passing % | Nets Tested | Nets Passed | Passing % |
| 5 mils | 68 | 19 | 27.9 | 36 | 31 | 86.11 | 16 | 9 | 56.25 |
| 6 mils | 80 | 65 | 81.3 | 108 | 99 | 91.67 | 16 | 9 | 56.25 |
| 7 mils | 68 | 68 | 100 | 78 | 75 | 96.15 | 16 | 9 | 56.25 |

TABLE 2. Testing Results Sorted By Via Pitch

| | Electrical Continuity Test | | | Thermal Stress | | | Thermal Shock | | |
|-----------|-----------------------------------|-------------------|--------------|----------------|----------------|--------------|----------------|----------------|--------------|
| Via Pitch | Coupons Tested | Coupons Passed | Passing % | Nets Tested | Nets Passed | Passing % | Nets Tested | Nets Passed | Passing % |
| 0 mils | 36 | 29 | 80.6 | 46 | 34 | 73.91 | 10 | 4 | 40 |
| 5 mils | 40 | 27 | 67.5 | 38 | 31 | 81.58 | 10 | 4 | 40 |
| 10 mils | 52 | 34 | 65.4 | 50 | 48 | 96 | 10 | 6 | 60 |
| 15 mils | 52 | 36 | 69.2 | 54 | 53 | 98.15 | 8 | 4 | 50 |
| 20 mils | 36 | 26 | 72.2 | 34 | 33 | 97.06 | 10 | 5 | 50 |

thermal cycles is six, but for this effort the coupons were subjected to 12 cycles to gather additional data beyond the minimum requirement. Pass/fail criteria are based on a resistance change in the daisy chain. The maximum resistance during the first cycle is used as the reference (baseline) resistance for the test. During thermal cycling the resistance shall not exceed a 5% change from the baseline measurement. FIGURE 5 shows results from 24 D-coupons tested for 12 cycles at the 260°C reflow profile. One chain stands out because the resistance increases each cycle and never returns to the original resistance value even at ambient temperature; this is an obvious failure. A few chains get progressively worse each thermal cycle, with some exceeding the 5% pass/fail criteria indicated by the red line. Many maintain near a 0% change in resistance from the first thermal cycle. The lack of resistance changes between each thermal cycle is a good indicator that the harsh environment of the reflow profile has not adversely affected the connectivity of the microvias.

Thermal shock, thermal cycle and continuity. In addition to thermal stress testing, thermal shock testing per IPC-TM-650 method 2.6.7.2C⁵ was performed on several D-coupons. This testing requires thermal stress testing be performed first, so this test must be performed in tandem with IPC-TM-650 method 2.6.27B. Several coupons that passed thermal stress testing were then subjected to thermal shock testing, which is a more rapid temperature cycle change, for 100 cycles. The test method defines the max. temperature of the thermal cycle to be the least of:

- Material T_g 10°C (lowest T_g of the materials used in the specimen, but not lower than 125°C)
- Reflow process peak temperature 25°C
- 210°C.

With peak reflow temperature around 230°C and mate-

rial with a minimum Tg of 250°C (per the datasheet), the max thermal cycle temperature is derived from the second bullet above and is 205°C. The default of -55°C was used for the low end of the temperature cycle. Resistance readings are recorded once per cycle, with cycle durations of approximately 8 min. and a maximum allowable resistance change of 5% after 100 cycles. FIGURE 6 shows the results of 24 nets from Supplier A: Some nets maintain a relatively constant resistance throughout the test, and some have a steady increase in resistance throughout the cycling.

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Printed Circuit Engineering Professional

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- 6.11 Final Deliverables Formats and creation process
- 6.12 Transfer to Manufacturer Manufacturing interface

Chapter 7: Advanced Electronics, EM Applications

- (During the review class only cursory coverage of Chapter 7 will be provided due to the advanced nature of this content.)
- 7.1 Energy Movement in Circuits –EM Theory
- 7.2 Critical Frequencies in Circuits on PC Boards Frequency and Rise Time (Tr)
- 7.3 Transmission Lines in PC Boards Relational nature in electronics
- 7.4 Understanding Impedance of Transmission Lines Modification from layout
- 7.5 Impedance Control of Transmission Lines Controlling impedance in layout
- 7.6 Controlling Impedance of Digital ICs Controlled and set to specific values
- 7.7 Controlling Noise Margin Critical lengths understanding
- 7.8 Crosstalk and Cross-coupling Capacitive and inductive coupling
- 7.9 Controlling Timing of High-speed Lines Timing matched, not length

Discussion

Fabricator B testing yielded almost 100%, and because of that, this discussion will focus on the data from the testing of coupons from Fabricator A. **FIGURES 7** and **8** show the yield comparison of three types of electrical testing that took place; the two methods mentioned above and electrical testing per IPC-9252B. **TABLES 1** and **2** contain the details behind the yield percentages, such as the number of coupons or nets tested.

Electrical testing per IPC-9252B is accomplished by flying probe or bed-of-nails testing and is performed at ambient temperature.⁶ No temperature cycling is associated with this testing. All coupons that failed electrical testing did so due to opens in the daisy chain. The resistive continuity testing (Figure 7) produced some interesting results: yield increased over 50% when the microvia diameters increased from 5 mils to 6 mils, and at 7 mils yield jumps to 100%. This was the first indicator of the importance of microvia diameter and/or aspect ratio.

Thermal stress testing results also improved as via diameter increased. As mentioned, 5-mil diameter vias had the most failures in electrical testing at ambient. Likewise, coupons with

FIGURE 9. Passing stacked microvia structure.

5-mil diameter microvias had the most failures when subjected to thermal stress testing. Yield increased approximately 5% when diameter was increased to 6 mils, and increased another 5% for the 7-mil microvias, which had a yield of just over 96%.

The final type of testing performed on the coupons was thermal shock testing. The sample size of coupons put through thermal shock testing was limited – only 24 of the 108 coupons from each fabricator were tested – as this testing wasn't as high priority as thermal stress testing and funding was limited. The environments were much less harsh on the coupons, with the maximum testing temperature 205°C. For that reason, more focus was placed on thermal stress testing, although more data could shed light on the importance of thermal shock testing.

Looking back to Figure 6 (thermal shock testing), a pack of nets show a steady increase in resistance for each subsequent cycle, and several of those nets do not exceed the 5% threshold, meaning those nets passed acceptance testing. The rate of change is alarming but does seem to be leveling. It would be interesting to see if the resistance change does level past 100 cycles, or if these vias could potentially be a reliability risk to



FIGURE 10. Poorly formed microvia.



FIGURE 11. Cross-section of a failing microvia from Fabricator A.



FIGURE 12. Higher magnification of the previous figure.









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FIGURE 13. FIB cut across the plating boundaries, 1,000x.



FIGURE 14. Previous figure at 6,000x.



FIGURE 15. Voiding between the electrolytic copper fill and target pad, 25,000x.

hardware, by continuing to increase in resistance each thermal cycle and eventually become an open circuit.

Thermal shock test results sorted by via diameters showed flat results, at 56% across all via diameters. Unfortunately, this doesn't leave anything conclusive when trying to identify correlating trends with via diameter and thermal shock testing.

Figure 8 sliced the same data by via pitch; the centerto-center distance between staggered vias. The results from electrical testing at ambient were relatively flat, with limited correlation to pitch. The 10-mil pitch yielded the lowest at 65%, whereas the 10-mil pitch had some of the best results through thermal stress and thermal shock testing. Interestingly, the 0-mil (stacked microvias) pitch vias had the highest electrical test yield: 80%. This is a testament that electrical testing cannot be relied on for screening microvia construction integrity.

Thermal stress testing did show an increase in yield with greater via separation. Yields were just under 75% on the stacked vias (0-mil pitch). As pitch increased to 5 mils the yield jumped to just over 80%, and at 10 mils the yield was 96%. The jump in yield between vias on 5-mil pitch and 10-mil pitch is relatively large, a 16% increase. At 5-mil pitch, the holes are tangent, but due to drill misregistration there is a chance the 5-mil holes could have some overlap. At 6 and 7 mils the holes will have some overlap in their nominal locations, but when the pitch is increased to 10 mils there is no overlap of the holes. All microvias have a 14-mil pad, which means when there is a 10-mil pitch between vias there is some overlap of the pads, but when the pitch is increased to 15 mils there is no overlap of the pads. With this limited amount of data, it is difficult to determine if the separation of the microvia holes or pads is more critical. But with a larger jump in yield when the microvia holes are separated versus the separation of pads, the data suggest it is more important to separate the microvia holes, but higher yield can still be achieved by ensuring the microvias are far enough apart that the pads do not overlap.

When the thermal shock data were sorted by via pitch, the results were also inconclusive. It will take more data to understand if there is a trend when it comes to thermal shock testing.

In summary, the component packaging may dictate the diameter and pitch of the via separation required to ensure large enough routing channels to escape from fine-pitch parts with producible line widths and spacing. The thermal stress reflow simulation testing results show higher yields with larger microvia diameters/lower aspect ratios and greater via separation, so it is important to maximize these for higher yields.

Failure Analysis

Several coupons were selected to undergo failure analysis to obtain a better understanding of what causes a microvia to fail or what certain indicators may be for poorly formed microvias. Several of the A/B and D-coupons





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FIGURE 16. Cross-section of a stacked structure from a failing coupon of Fabricator B.



FIGURE 17. Base of the microvia from the previous figure at 1600x.



FIGURE 18. The previous figure rotated 90° CW at 5,000x.

were cross-sectioned and examined from both fabricators. FIGURES 9 and 10 show a stark comparison between the two. Figure 9 is a cross-section from a microvia structure stacked on a buried via in a D-coupon from Fabricator B that passed both thermal stress and thermal shock testing. The microvia is fully filled with copper without any voiding. The cap plating on the buried via is also very uniform and relatively thick. It meets the minimum cap plating thickness requirement of 0.0005" per the IPC-601x series. These two items seemed to be good indicators of properly formed microvias that will pass both thermal stress and thermal shock testing, as described earlier. On the contrary, Figure 10 contains a microvia with a lot of voiding, close to 50% of the microvia. The cap plating for the filled buried via structure is very thin, so thin that it looks like the laser process forming the microvia penetrated the cap plating and into the via fill material of the buried via. Vias from both fabricators were formed with UV-CO₂ combo lasers. With this combo process, the UV penetrates the copper and the CO₂ penetrates dielectric, so the equipment alternates to first penetrate the surface copper layer with the UV laser, followed by a CO₂ laser to penetrate the dielectric. When forming the microvia on top of the buried via shown in Figure 10, the cap plating could have been so thin or porous that the laser was able to penetrate it, leaving behind even less copper surface area for the base of the microvia to adhere to.

FIGURE 11 is a microvia on top of a buried via with a 5-mil offset from fabricator A that we will take a closer look using focused ion beam (FIB) milling and a scanning electron microscope (SEM) for high magnification images. Both Figures 11 and 12 are from an optical microscope.

FIGURE 12 shows dark boundaries above and below the cap plating layer. This indicates there may be separation, but it is very difficult to tell at these magnifications.

In FIGURE 13 the sample is rotated so the FIB cut can mill across the plating boundaries at the base of the microvia. After the milling is performed, SEM imagery can be used to get a very good look at the plating boundaries. In FIGURE 14 the separation occurring at the electroless copper layer between the target pad and the electrolytic copper is becoming more obvious.

FIGURE 15 focuses on the voiding occurring in the electroless copper layer. The copper grain structures do not bridge the plating boundaries. This is not a good sign the copper formed properly. Ideally, these crystal structures form across the boundary, but due to the separation they were not able to.

The results from Fabricator B have not been discussed because almost all coupons passed testing. One coupon, however, failed thermal stress testing. This coupon was cross-sectioned, and the results (FIGURES 16 and 17) using an optical microscope look very similar to Figure 9 at lower magnification. This shows it may be difficult to determine pass/fail criteria for microvias using only crosssectional analysis.

When looking at the optical microscope and SEM

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images of this microvia, the separation occurred between the thin electroless copper plating layer and the electrolytic copper fill, which can start to be seen in Figure 17 and becomes much more apparent in **FIGURE 18**. The separation can be seen in more detail after the FIB cut in **FIGURES 19** and **20**. There is suspicion that oxidation occurred between this boundary, but energy dispersive x-ray spectroscopy (EDS) was not able to verify this. One last item to point out is the thin layer of material in the separation: this is redeposited material from the FIB milling process and is not a part of the fabrication process.

In the future, transmission electron microscopy (TEM) may be used to help pinpoint the exact location of the electroless and confirm where the separation is occurring. In Figure 19 the separation occurs between the electroless copper and electrolytic copper fill, yet in Figure 14 it is not as clear.

Conclusions

Through extensive testing of hundreds of D-coupons repre-



FIGURE 19. Plating boundaries after the FIB cut, 10,000x.



senting various microvia diameters and pitches, some correlation came to light. Electrical continuity testing showed much better yield for larger diameter vias, yet it should not be relied on for screening microvia reliability because it does not expose the microvias to the environments they are most vulnerable to. Thermal stress testing yielded better results with larger diameter microvias and greater pitch microvias. These yields were greater than 90% for staggered microvias separated by at least 10 mils center-to-center, and the 6- and 7-mil diameter microvias with aspect ratios of approximately 0.75:1 and 0.64:1, respectively. The data show designing with an aspect ratio less than 0.75:1 combined with a diameter of 6 mils or greater and separation of 10 mils or more provides a more robust yield, even from a less-capable fabricator. The second fabricator with a more robust process yielded good results on almost all via constructions, including 5-mil stacked microvias. The next phase in this project will be to fabricate panels from more fabricators and run the same or similar testing to get a better idea

on what the limits are within our domestic supply base.

Acknowledgments

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FIGURE 20. Separation in the plating, 60,000x.

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Cold Underfill COMPONENT REMOVAL

Newly developed, dedicated purpose precision milling machinery simplifies rework. **BY BOB WETTERMANN**

BGAs, CSPs, flip chips and other component packages on handheld devices are commonplace today in consumer, military, and industrial products such as tablets, smartwatches, and handheld computers. These handheld products, along with transmission control modules, cameras and image sensors in the automotive sector, use underfill to withstand mechanical shock or impact that takes place when devices are dropped or struck. Underfilling these component packages creates a compliant layer between the package and printed circuit board that increases the reliability of the interconnections even when subjected to outside forces.

Underfill is a polymeric material used to fill the gap between the PCB and underside of the electronic component package, thereby surrounding and protecting the solder joints. This material boosts the reliability of the component, which is subject to mechanical impacts and shocks by distributing the forces. Thermal stresses caused by the coefficient of thermal expansion (CTE) mismatch between the component and PCB are lessened using underfill. Typically, underfills have a high modulus (E) matched CTE with respect to the solder, as well as a high glass transition temperature (Tg). Underfill

dampens and distributes the stress more uniformly on the solder joints, thereby increasing interconnection reliability. As pitch of components such as CSPs becomes tighter, the standoff height between the bottom of the device and PCB lessens, thereby reducing the PCB level reliability.¹

Challenges with reworking of underfilled components on PCBs include but are not limited to the following:

- Many underfills, when softened at elevated temperature, displace solder joints and components, resulting in defects.
- 2. The economics of underfill removal are not worthwhile. Low yields and

the prohibitive cost of long processing times for experienced "high touch" rework are the norm.

- Potential physical damage to the PCB is a risk as the underfill rework process may cause laminate damage, mask destruction and lifted pads, reducing assembly reliability (FIGURE 2).
- 4. Non-reworkable underfills, which exhibit excellent stability at temperatures much higher than the liquidus temperature of lead-free solders, are difficult to rework using standard PCB rework processes and tools. This eliminates the possibility of using a thermal- or thermal/mechanical-based rework process.
- OEMs object to use of chemical "softening agents," which can aggressively attack the PCB and may damage components, boards and other materials.

These challenges were confirmed in the iNEMI 2019 *Roadmap*², in which the Rework section outlined that one of the most significant rework challenges is reworking where there is minimal or zero clearance between adjacent parts near an underfilled area array device.



FIGURE 1. Underfill is dispensed under advanced packages such as BGAs and CSPs to increase reliability.

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Current Underfill Rework Process Methods

Hot air or IR heat source. The first step in preparing a board for rework is to bake it per J-STD-033 to prevent moisture-induced failures. Underfill provides a strong adhesive force on the underside of the component that needs to be "broken" to lift the component on the rework station. This means the board needs to be properly fixtured and secured. Bars, pillars or custom pallets are used to hold boards in place during the removal cycle.

Like all rework processes, a proper temperature profile is needed, with thermocouples embedded at key locations such as the corners of the device, the die, and the corner and middle solder balls. The proper removal profile should minimize the force necessary to break the bond between the underfill and board. If temperatures are too low, excessive force will be required, and BGA pads will have a propensity to lift during the removal process. A profile that is too hot or long may cause other issues, such as component or board warpage, and underfill pushing solder joints off the pad.

Several methods exist for breaking the force between the underfill and board or the underfill and component. In some cases, the rework technician manually cuts through the underfill with a (heated) knife. Once completed, the tech will pry the BGA loose from the board. Various rework nozzle designs can aid in the removal. In some cases, the nozzle can be twisted during the removal process. Alternatively, a special gripper nozzle can simultaneously grab and lift the component. Once the component is removed, underfill residue is left behind. Tacky flux is applied with the heat from a soldering iron or hot air tool to soften the remaining residue. This mixture is best removed with solder braid. This process is not only timeconsuming, but may lead to damaged mask or lifted pads. In addition, the potential damage to neighboring components can result.

After being dressed, the site is cleaned using IPA and a wipe. The site is now ready for placement and reflow of the replacement component.

Chemicals. Commercially available organic solvents can dissolve and remove a cured underfill from underneath an area array package. In this rework scenario, the board is placed into the softening agent, which may or may not have to be at an elevated temperature. The overriding concern with this technique is the unknown impact of the chemical on components and the PCB. After exposure to the softening agent, the component is subjected to hot air or IR rework sources to remove the component.

Laser ablation. Another technique for removing the component utilizes selective laser ablation of the component, underfill material and solder. This process involves careful laser processing and source selection, as the wavelength of the laser must be tuned to multiple material absorption spectra to ablate the material. In addition, the depth of the laser needs to be carefully controlled to avoid damage to neighboring components or the PCB.



FIGURE 2. Underfilled BGA pulls up pads upon removal of component in a non-reworkable underfill.

Refined Cold Milling Process

One of the other techniques to remove underfilled components is through a "cold" process. The component is milled from the PCB, leaving a solder remnant of a few thousandths of an inch. The remnant solder becomes the pre-tinned pads for the replacement component.

Alternatively, the milled location can be site-prepped using a soldering iron and braid to remove remnant solder. This process ensures components near the rework location do not experience solder reflow temperatures. This eliminates solder from being "squirted" out by the softened underfill, which can cause solder shorts or opens.

Previous milling methods have used retrofitted commercially available mills with some modifications to accomplish this mechanical "cold" removal. While the milling machines could be grounded, static charges generated during the milling operation could cause ESD damage. Solder, component and other debris could cause potential reliability risks if permitted to spread to other areas of the PCB. Couple this with the vibration of the milling operation and the subsequent risk to cracking of solder joints made this technique a last-ditch approach for underfilled component removal. The machine operator and rework technician masking the board of any potential foreign object damage (FOD) and site preparation must be highly skilled to work on such projects.

Newly developed, dedicated-purpose precision milling machinery simplifies the process of component removal via a "cold" removal milling process. The commercially available machinery today consists of the following:

- Rework software, including structured machined programming, eliminates the need for a highly skilled CNC programmer/operator to run the machines. The x and y dimensions generate the milling pattern. Fiducials on the PCB read by the machine sensors and all precision alignment are locked onto these coordinates. Irregularly shaped features like those of an RF shield are easily programmed into the machine.
- A vacuum chuck that does not permit metal shavings to be dispersed from the rework area eradicates shielding of each rework location.
- An integrated active ionization source, which reduces the

Fully Automated Milling of Electronic Components on Printed Circuit Boards <u>without Heat</u>



Main Applications

- Underfilled & Conformally Coated Components that can't be removed with heat.
- Non-Underfilled Components: Eliminates removal and site cleaning heating cycles.
- RF Shields: Removal without heat, protects underfilled components inside the shield.

Key Features

- Flexible Software: Easy-to-use including virtual milling.
- Automatic Laser Height Measurement of board and component.
- Particle Removal System: Proprietary vacuum-based with self-contained Hepa filter.
 - Automatic Tool Changer with Tool Length Measurement System.

Static Elimination System

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FIGURE 3. Initial x-ray of BGA rework location of under-the-hood module.



FIGURE 4. Neighboring passive components shifted and solder balls formed during reflow of underfilled components.



FIGURE 5. BGA of under-the-hood PCB milled to 2.2-mil height.



FIGURE 6. Underfilled BGA rework location for retail communication system.



FIGURE 7. Lifted pads after removal of underfilled BGA.

potential incidence of charging due to the milling operation.Vacuum-based board holding and support are used to

- ensure coplanarity of the milling surface relative to the PCB.
- Laser-based automatic multipoint measuring scheme to determine the true accuracy of the component, board and tooling offsets. In some cases, this permits cuts to within 0.001" from the board surface.

Case Studies

Under-the-hood automobile module. In an application requiring removal of a BGA (FIGURE 3) directly on the other side of an underfilled component, heat-based component removal techniques did not work. As soon as either hot air or IR energy was directed onto the component to be reworked, the temperature on the other side of the PCB rose to a point where the underfill material softened. Once this occurred, the underfill expanded, pushing neighboring reflowed solder around the PCB. This action led to solder balls formation, disturbing components (FIGURE 4).

Using the cold removal process on the BGA, the neighboring underfilled components do not experience the underfill shift or push around components or solder, resulting in a much higher yield (over 90%). At the same time, this obviated the need for highly skilled and experienced BGA rework and repair technicians to fix the problem. The component was milled off using a 30-mil diameter mill at 15,000rpm spindle



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speed and a horizontal travel of 2mm/sec. The milling routine was optimized using a variety of cut depths. This included taking larger depths of cut initially as the cutter moved through the component body, and then smaller depths of cut with a 20-mil diameter bit using a slower cut speed. After several cuts, the distance from the final milled surface to the PCB surface was, on average, 2.2 mils (FIGURE 5). Once the BGA location was milled, the component was placed using a paste flux stencil printed on the replacement BGA. It was reflowed using a split vision hot air rework station with a 60 sec. time above liquidus (TAL) profile. X-ray imaging along with dye-and-pry analysis confirmed the previously disturbed components were free of soldering anomalies.

Communication system for retail. A handheld retail communications PCB (**FIGURE 6**) had underfill applied at a variety of component locations. The BGA rework location was also underfilled. The adhesive properties of the non-reworkable underfill caused the underlying BGA pads to lift off the board during hot air removal (**FIGURES 7** and **8**). Removing the remnant solder and underfill from the BGA location resulted in numerous lifted pads. While some pads were "no connects," others that were lifted most often were connected to either vias or lands, making the repair time-consuming and therefore "beyond economic repair."

After consultation with the OEM, more samples and further process development yielded a cold removal process using a commercially available precision milling system. After two gross depth cuts and two refined milling profiles, the component was removed with 2.5 mils of solder remaining on the pads. The milling process resulted in no pads being lifted. In addition, this semiautomated process took some of the "art" out of the rework process, thereby improving yield and throughput. The component removal time of 14 min. added 7% to the cost of the rework service. The replacement component was placed directly onto the milled surfaces (FIGURE 9) without further site preparation using a paste flux dipping process. After component placement, replacement underfill was applied to the BGA.

The PCB component milling removal process has become more automated, and many previous shortcomings in milling of electronic components have been overcome. These process developments, due to the built-in vacuum chuck and real-time, high precision laser-guided depth measuring, make the latest commercial version of milling of components more attractive. The vibration as well as temperature effects of milling and resulting impact on solder joint reliability need further investigation to use this process on other assemblies.

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FIGURE 8. Lifted pads after removal of underfilled BGA.



FIGURE 9. BGA removed using cold removal process.

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continued from pg. 22

ring that creates a Faraday cage around the PCB edge. This might be a partially isolated ground, depending on the circuit.

- The transient suppression circuit is helped by localized mounting holes where the PCB ground is tied to the enclosure. Anchoring the connector is good for mechanical reasons, too.
- Place ESD diodes near the connector (ESD source) and route with short, unbending traces, including a lowimpedance ground termination. Multiple ground stitching vias are good, if there is room for such things.
- You don't necessarily want sensitive components to be placed near the connector/ESD diode region. A little routing will do some good, up to a point.
- These additional ESD suppression components will eat into your loss budget, so try to maintain low capacitance on the signal going down the line.

Going beyond the layout considerations, the particular assembly process

documentation and general workmanship manual should stress the importance of proper PCB handling with respect to ESD. Those documents would be called out by reference on the assembly drawing.

Some manufacturing engineers will request we add notes to the assembly drawing that detail some or all the processes of the assembly. Lab coats and straps have nothing to do with the state of the product when it is all done. They are a means to an end. The assembly drawing is not a how-to but rather a what-is type of document.

ROI, continued from pg. 16

process and most of all, thinking. So far, such a shift to enable mainstream acceptance and application of printed electronics does not appear to have occurred. In the case of 3-D printing, mechanical engineers have embraced and successfully implemented it into many facets of the manufacturing shop floor. Now, hopefully, it's the electronic engineers' turn to harness that radical new technology.

With two potentially disruptive technologies nibbling away at the applications of traditional electronic circuits, maybe there will be enough free-thinking engineers and design visionaries who together will reimagine what is possible when these disruptive technologies finally emerge.



FIGURE 2. Swaged turret terminals such as these provide a high-reliability method of connecting wires to a PCB. We can't rely on the strength of the copper barrel of the plated hole. (Source: Greenhouse Lighting)

The wisest course to bring ESD awareness to the assembly and test benches is to label the board accordingly. The marking on the board itself should indicate it has sensitive components as the largest single piece of information. The purchase order should include packing instructions for safe transportation.

Taking an interest in electrostatic discharge shows that you care about the bottom line. Being mindful in the lab or wherever electronic components are exposed will help those parts reach their full potential as part of a working unit. Make it happen.

Material Gains, continued from pg. 26

events as the data suggest them. Through not knowing any better, machines can hypothesize situations the human mind would discard immediately as unconscionable. In this way, they can force us to contemplate scenarios we could not, or would not, imagine. At this point, the role of the human becomes essential, bringing the critical thinking needed to distinguish the real black swans from the shadows and reflections that will inevitably be present.

As the coming industrial revolution seeks to leverage human qualities to ensure human fulfillment, support of our most advanced machines can enable the resilience that is an essential part of the mix. \Box

Stencil Nanocoatings, Only Better

A "rougher" foil may improve stencil performance.

A HIGH-PERFORMING stencil printing process deposits the right amount of material volume in the right place, at the right time, and at the lowest cost per print achievable. Every assembly professional strives for this utopia, leaving no solder paste stuck in the apertures or smeared on the underside of the stencil. Naturally, with all the variables, this state is difficult to achieve 100% of the time. A perfect gasket (board to stencil) does not exist in the electronics manufacturing real world. Transfer efficiency is managed through aperture designs to provide the desired material volume on the pad, and solder paste smear (or its potential) is allevi-

ated by cleaning the underside of the stencil between prints to avoid bridging. Cleaning, of course, comes at a cost - both in consumables use and in production time. If more high-quality prints can be achieved between necessary cleans, consumables overhead will be lower and throughput will be higher. Stencil nanocoatings have helped to meet these objectives. The coatings are fluxophobic materials proven to prevent paste and flux from adhering to the stencil surface or

"A MICRO-ROUGHENING TECHNIQUE APPLIED TO STENCIL FOILS INCREASES SURFACE AREA FOR BETTER NANOCOATING ADHESION."

inside apertures, keeping the underside of the stencil relatively free from unwanted material and, in some cases, encouraging better material release.

Stencil nanocoatings arrived on the electronics assembly scene over a decade ago, first as self-applied wipe-on materials and then as professionally applied (at the stencil manufacturer) spray coatings. Regardless of the application mechanism, the end goal was the same: to improve material transfer efficiency, reduce solder paste smear and build-up on the stencil underside and, through these capabilities, increase print cycles between understencil cleans while also raising print reliability. And they've worked as intended. As miniaturization has accelerated over the past decade, thin, polymer stencil coatings have become standard protocol for many operations, particularly for applications with very small dimensions and tight interspaces. While coatings are likely here to stay, their durability could stand some improvement.

With dimensions and board densities becoming more challenging, it's not surprising that understencil

post-laser cut – are texturized to increase the surface area, permitting better mechanical bonding of the coating and long-term adhesion durability. These added micro features are relatively shallow – less than 5μ m deep – to avoid impact on stencil integrity. Additionally, the nanocoating materials are self-leveling and, once cured, result in a smooth, even layer. Some analysis suggests that coating longevity can be extended by a factor of 10 and makes the stencil extremely resistant to high sear force. In some instances, manufacturers have reported the coatings may also aid in creating a better board to stencil gasket, furthering their effectiveness for defect avoidance (bridging) and cleaning optimization.

Producing advanced electronics assemblies to power the digital world is becoming more challenging. Assembly professionals must use every tool in the box to raise yields and reduce costs. Stencil nanocoatings are one of many ways to do that and, with this new technique, they are better, longer lasting and more durable than ever.

cleaning technologies have become more thorough and frequent, ranging from 10 plus to every print, even on coated stencils. This more rugged cleaning regimen has also introduced the potential for the stencil nanocoating to delaminate if subjected to numerous aggressive cleaning cycles. The nano materials are made in various formulations and, as stated, are applied to the foil at the time of stencil manufacture. Typically, the coatings are sprayed on in an ultra thin, 4µm layer, thoroughly coating the bottom of the stencil and aperture walls. They are then cured to form a mechanical bond. Because stainless steel is a smooth

> surface, maintaining that bond over time and after hundreds - if not thousands - of cleaning cycles is difficult. Therefore, a more durable stencil coating process has been developed to address the propensity for delamination, which could introduce the opportunity for defects. As the coating formulations are very effective, the aim was to find a mechanism to increase the coating's bonding robustness. Using a novel microroughening technique, stencil foils - either pre- or

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polarinstruments.com/2022/speedstack_sep_2022.pdf

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In Case You Missed It

Electronics Recycling

"Conductive Ink with Circular Life Cycle for Printed Electronics"

Authors: Junpyo Kwon, Christopher DelRe, et al. Abstract: Electronic waste carries energy costs and an environmental burden rivaling that of plastic waste due to the rarity and toxicity of the heavy-metal components. Recyclable conductive composites are introduced for printed circuits formulated with polycaprolactone (PCL), conductive fillers and enzyme/ protectant nanoclusters. Circuits can be printed with flexibility (breaking strain $\approx 80\%$) and conductivity $(\approx 2.1 \times 10^4 \text{ S m}^{-1})$. These composites are degraded at the end of life by immersion in warm water with programmable latency. Approximately 94% of the functional fillers can be recycled and reused with similar device performance. The printed circuits remain functional and degradable after shelf storage for at least seven months at room temperature and one month of continuous operation under electrical voltage. The present studies provide composite design toward recyclable and easily disposable printed electronics for applications such as wearable electronics, biosensors and soft robotics. (Advanced Materials, May 2022, https://onlinelibrary.wiley.com/doi/abs/10.1002/ adma.202202177)

Solder Joint Reliability

"Accelerated Solder Interconnect Testing Under Electromigratory and Mechanical Strain Conditions"

Authors: Mahsa Montazeri, Whit M. Vinson and David R. Huitink

Abstract: Continuous power density increases and interconnect scaling in electronic packages raise risk of electromigration-induced failures in high current interconnects. Concurrently, thermal cycling fatigue also places interconnects at risk of failure during electronics' operating lifetime. These two differing failure mechanisms are historically treated separately, but in operation, the combination of EM effects and thermal cycling can act synchronously in accelerating failure. Presently, no model predicts the complexity of reliability estimation arising from these interacting failure modes but is certainly important for high-current-density applications. In this work, a novel testing system has been employed to help estimate the reliability of solder interconnects under the combined influence of EM and mechanical strain. The system subjects solder interconnects to high current density, elevated ambient temperature and a constant tensile stress while recording the change in electrical resistance and change in length of the solder over time. The solder samples were created using two copper wires connected by a eutectic PbSn solder ball to imitate flip-chip or BGA packaging interconnects, permitting controlled testing conditions to demonstrate the combined effects of a mechanical load and EM on the lifetime of a solder joint. A significant reduction in lifetime was observed for samples that endured the coupled accelerating factors. Comparing the experimental results of different current densities at different stress levels provided a new outlook on the nature of coupled failure acceleration in solders. This novel test methodology can inform model generation for better anticipating the failure rate of solder interconnects that naturally experience multiple stress inputs during their lifetime. (Journal of Electronic Packaging, Aug. 8, 2022; https://asmedigital collection.asme.org/electronicpackaging/articleabstract/145/2/021002/1143211/accelerated-solderinterconnect-testing-under)

"Investigation of Solder Beading Phenomenon Under Surface-Mounted Electrolytic Capacitors"

Authors: Daniel Straubinger, et al.

Abstract: A study of the solder beading phenomenon (referring to larger-sized solder balls) of surfacemounted electrolytic capacitors. Solder beading could induce failures by violating the minimal electrical clearance on the PCB. In modern lead-free reflow soldering, especially in high-reliability industries, detecting and preventing such defects is essential in reliable and cost-effective manufacturing. The large size of the involved components may block the view of automatic optical inspection; therefore, x-ray inspection is necessary. To detect the failure mode, x-ray imaging, cross-section grinding, optical microscopy and Fourier transform infrared spectroscopy (FTIR) were used. High-resolution noncontact profilometry and optical microscopy were used to analyze component designs. The surface mounting process steps were also analyzed to reveal their dependence on the issue. Test methods were designed and performed to reveal the behavior of the solder paste during reflow soldering and to emphasize the component design relevance.

It was found that the reduction of solder paste volume reduces the failure rate but does not solve the problem. Results show that excessive component placement pressure could induce solder beading. Statistical analysis revealed that differences between distinct components had the highest effect on solder beading rate. Design aspects of solder beading-prone components were identified and discussed as the primary source of the problem. The findings can be applied in SMT production, where the total failure count and resulting failure costs could be reduced according to the findings. (*Soldering & Surface Mount Technology*, June 2022, https://emerald.com/insight/content/doi/10.1108/SSMT-06-2021-0039/full/html)

This column provides abstracts from recent industry conferences, technical journals and company white papers. Our goal is to provide an added opportunity for readers to keep abreast of technology and business trends.



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