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PRINTED CIRCUIT DESIGN & FAB CIRCUITS ASSEMBLY

BREAKING NEWS

CURRENT EVENTS –

Design Charts for Sizing Electrical Traces

- ✓ *OSPs ARE NOT ALL THE SAME*
- ✓ *PACKING YOUR PCBs*
- ✓ *CONTROLLING IMPEDANCE*

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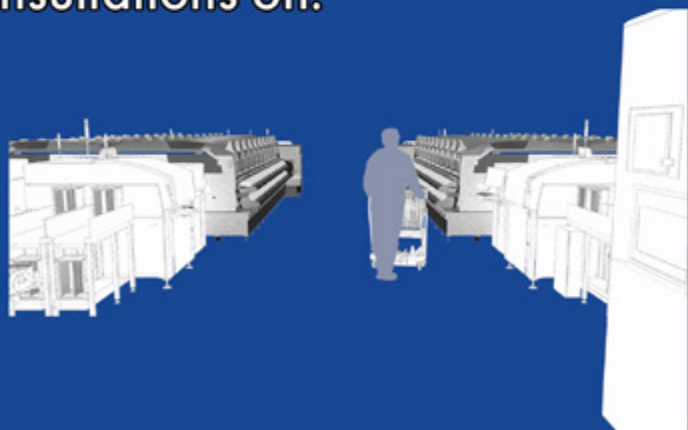
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by MIKE JOUPPI

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by MICHAEL CARANO

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A Royal Summit
In May, Summit Interconnect announced its acquisition of Royal Circuit Solutions, expanding the fabricator's capacity of rigid and flex PCBs. But it was the behind-the-scenes technologies and assembly capacity that convinced Summit president and CEO Shane Whiteside to make the deal.
by MIKE BUETOW



PCB Chat

ON PCB CHAT (pcbchat.com)

RIT PCB DESIGN COURSE RECAP
with DR. KIRSCH MACKEY and DR. JAMES LEE

BEST PRACTICES FOR PURCHASING X-RAY EQUIPMENT
with KEITH BRYANT, DR. DAVID BERNARD,
DAVID KRUIDHOF and ROBERT BOGUSKI

PEOPLE MANAGEMENT SKILLS
with JOHN BURKHERT JR.

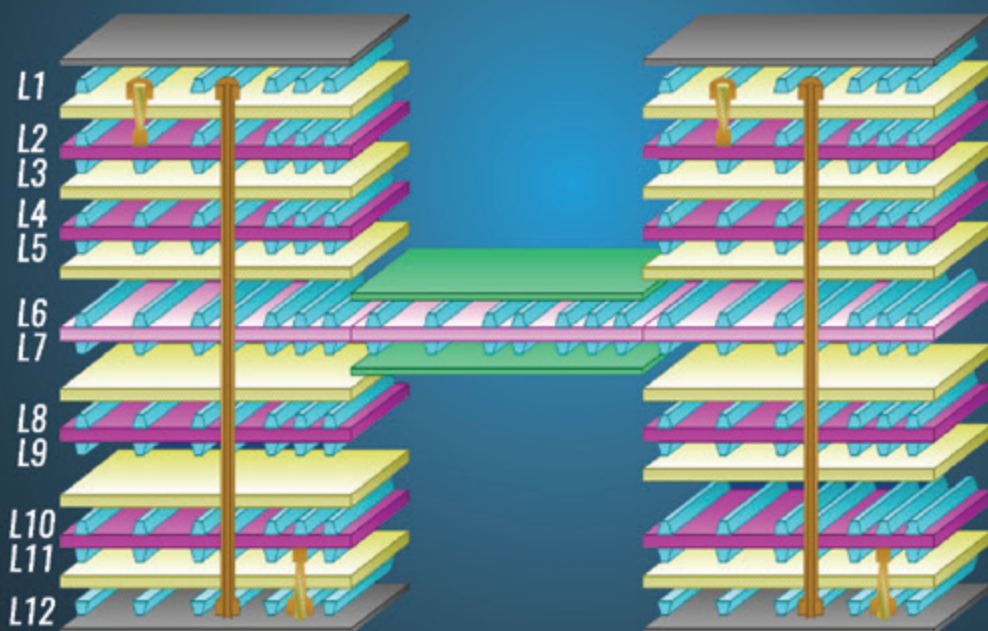


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PCB Update

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AWARDS

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The CIRCUITS ASSEMBLY
DIRECTORY OF EMS COMPANIES

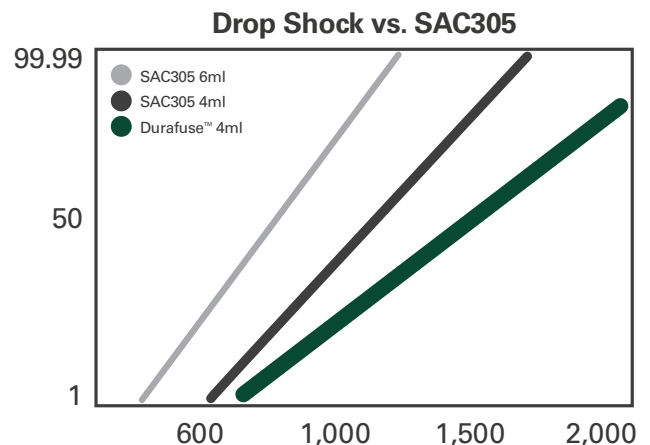
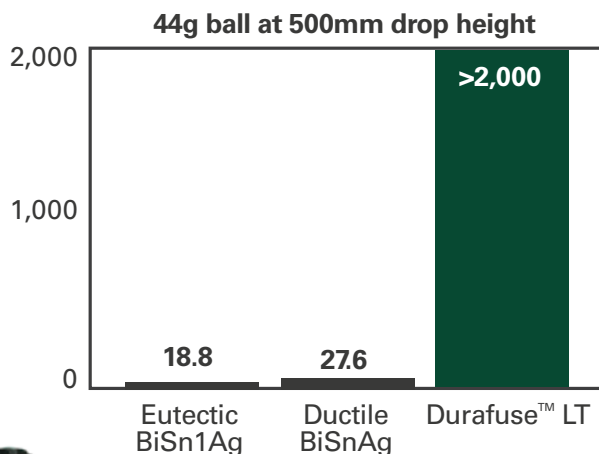
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Training Begets Retaining

FOXCONN WAS IN the news (again) last month, this time for alleging competitors are poaching its employees.

The complaints were levied specifically at rivals in Vietnam, where the world's largest ODM/EMS is expanding its factories as major customers like Apple shift production away from China, in part to avoid being a pawn in the geopolitical tug-of-war between the US and China.

Foxconn, which currently employs about 60,000 workers in Vietnam, asserts its EMS competitors are establishing their own operations near Foxconn's to make it easier to entice workers to jump ship.

Poaching complaints are hardly new, of course. Mexico is notorious for workers relocating *en masse* from company to company in pursuit of everything from higher pay to better food in the plant cafeteria.

Audrey McGuckin, who spent 10 years as chief talent officer for Jabil and now consults to Kimball Electronics, among others, points out the top stress point for CEOs is talent. And a McKinsey study found only 5% of CEOs feel their organizations' talent management has been very effective at improving company performance.

Covid-related issues have raised the profile of workers and increased their bargaining power, at least in the current term. And for their part, staffers at all levels are taking advantage of the situation.

The issue isn't whether employees can or should switch jobs. It's what steps companies can and should take to ensure valued workers *want* to stay put. In short, what can companies do to keep workers?

Having a culture that respects and promotes employees is often cited, of course. But how do you get there?

Don Charron, CEO of Kimball Electronics, says developing the EMS company's bench was a point of emphasis upon its spinoff from its parent company in 2014. In an interview on McGuckin's podcast, he said, "We literally were one deep in several really important positions, not just in the leadership level but in middle management as well. And I thought about our practices around talent, and it was a concern to other leaders on the team, but we really didn't know how to approach it."

Kimball, which has more than 6,400 employees today, realized it needed a combination of formality, rigor and science for its talent acquisition.

Charron says Kimball put a framework in place in order "to have a tougher conversation, a better conversation with people about their personal development, and it ended up with insights that were more

actionable." It all started, he acknowledged, with him and his leadership team getting priorities in place, then getting the priorities down to the workforce.

This tracks with studies performed by Harvard Business School professor Robert Kaplan, who has shown that among publicly traded companies, those that best communicated their goals and objectives throughout the entire organization were more profitable over time than those that fell short. Kaplan arrived at his conclusions through interviews of upper and middle management and hourly personnel, where he studied whether the message as conceived and intended by the ranking officers was understood and internalized at the lower levels.

Oscar Gonzalez, vice president of operations, Mexico at Mack Technologies agrees. In an interview on the PCB Chat podcast this spring, Gonzalez said, "I think the best companies [in Mexico] are retaining talent. ... There's been studies on the key elements people look for. Competitive salary. Tasty food in the cafeteria. Being treated with dignity and respect. And training, the amount of hours you provide employees training."

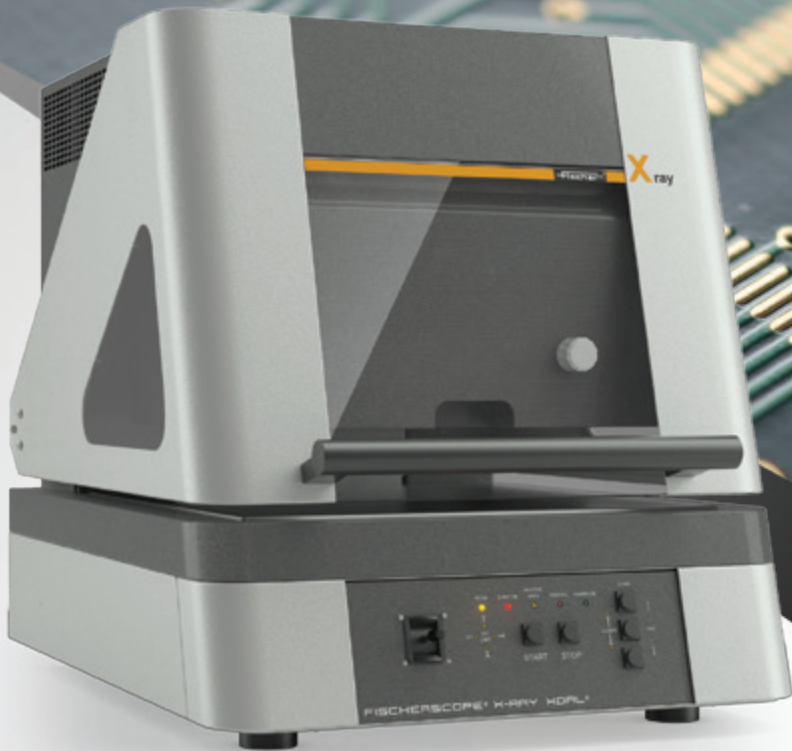
In my experience, middle management is where communications break down. Often those promoted to lower-level management positions are thrust into the role due to an unanticipated need and based on their skills and performance in operations or sales. They are not trained for their new responsibilities, nor are they given time to acclimate to the role under the watch of a skilled mentor. They are handed a budget, a handful of direct reports, and basically told to make it work. Those who lack flexibility and acuity quickly find themselves in tricky situations, without the tools to resolve them appropriately.

Workers, for their part, have a once-in-a-generation opportunity where they don't need to hang around waiting and hoping for an internal change.

As Gonzalez says, training helps retain valued employees. The best printed circuit engineering training program of the year is PCB West, which takes place Oct. 4-7 at the Santa Clara (CA) Convention Center. Registration is open at pcbwest.com.

The greater economy is outside our control, but every company can study their internal goals and objectives, and put into place bidirectional communications systems that ensure those priorities are heard and met throughout the organization. □

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PCDF People



Averatek appointed **Michael V. Carano** vice president of quality. Carano brings 40 years of electronics industry experience to Averatek, with expertise in manufacturing, chemicals, met-

als, semiconductors, medical devices and printing.

Fresh Consulting named **Rob Blomstrom** PCB design engineer.

SEMI named **Joe Stockunas** Americas president. Before joining SEMI, he served as executive vice president and corporate officer of Nordson, overseeing the company's worldwide electronics systems business.

PCDF Briefs

Altair in June acquired **Concept Engineering** for an undisclosed sum. Concept Engineering provides automatic schematic generation tools, electronic circuit and wire harness visualization platforms, and electronic design debug tools.

Atotech sold its 1,000th horizontal electrolytic copper plating line.

Eltek in June reported a fire in one of the production rooms in its plant in Petach-Tikva, Israel. The fire damaged part of the production line in that room and was extinguished without harming staff.

The European Union and Taiwan have set up a platform to work together on semiconductor supply chains.

Prototron Circuits added two **PHI** lamination presses.

The **SEMI Foundation** has been awarded \$1.5 million to design and develop the SEMI Career and Apprenticeship Network (SCAN) in Michigan.

TPCA is publishing a roadmap for PCB smart manufacturing in Taiwan. Chairman Maurice Lee, a senior consultant at **Unimicron**, says "member cohesion, industry competitiveness enhancement, and sustainable new value" and a high-value, low-carbon Taiwanese PCB industry are the main goals for his term.

Westak Circuits installed four **Tagarno** digital microscopes.

WUS Printed Circuit plans to spend \$280 million on a new production facility in Thailand.

Technical Conference Program Set for PCB West 2022

PEACHTREE CITY, GA – The PCEA Conferences Task Group announced the technical program for PCB West 2022, featuring nearly 50 presentations and more than 110 hours of in-depth electronics engineering training.

Among the industry experts on tap for this year's show are Rick Hartley, Susy Webb, Thomas Chester and Dan Beeker. The conference will be held October 4 to 7 at the Santa Clara Convention Center and features classes for every level of experience, from novice to expert.

The scope of classes ranges from basics on design engineering and DfM, to designing and building advanced HDI and routing high I/O count chip packages, board stackup, circuit grounding, low layer-count (IoT) board design, high-frequency design, thermal management, and a complete virtual plant tour of a flexible circuit manufacturing facility. New courses this year include RF and microwave design, PCB layout of DDR memory, mechanical design, and raw material selection.

To drive engagement between experts and attendees, three panel discussions have been arranged on topics ranging from leading-edge component packaging drivers, emerging technologies, and discussions on careers in electronics engineering. These open forums are designed to spur lively interactive discussions on what electronics engineers can expect over the next 12 to 24 months.

"Printed circuit engineers are ready to get back to face-to-face events, and the PCB West technical conference has all the reasons they need to make their return to live interaction more than worth their time," said Mike Buetow, conference director, PCB West.

Registrants who sign up by Sept. 6 can take advantage of the Early Bird Special discounts for the conference, which features 49 presentations and panel discussions spanning 114 hours of classroom time.

For the first time, the program was developed by committee, as more than 70 abstracts were reviewed by the PCEA Conferences Task Group. The task group is made up of nine industry veterans with more than 270 years of cumulative experience in the printed circuit industry.

An exhibition featuring more than 100 leading suppliers to the electronics design and manufacturing industry will be held October 5. For more information, visit pcbwest.com.



PCB West Keynoter Dr. Brian Toleno to Focus on Where Electronics Meets Virtual Reality

PEACHTREE CITY, GA – The metaverses offer myriad opportunities not just for users but for developers of computing devices. As that market takes off, what novel innovations in materials and production will be needed for printed circuit designs to meet the requirements for weight, size, and functionality?

Those are the questions Dr. Brian Toleno, manager, Applied Materials at Meta's Reality Labs, will tackle when he keynotes this year's PCB West conference. His talk, Augmented and Virtual Reality, the Next Computer Revolution, will describe the current market, use cases, and the technology all around AR/VR, with a focus on the printed circuit board aspects.

At Meta, Dr. Toleno leads a multi-disciplinary team that works on the material challenges in Meta's consumer electronics hardware. These devices include VR headsets (Quest 2), smart glasses (Ray-Ban Stories), Portal smart screens and other exciting devices that help bring people together.

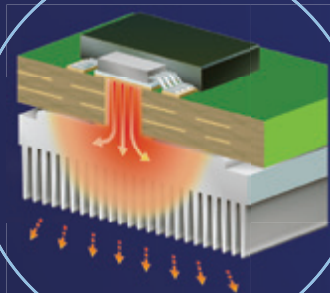
Dr. Toleno is a leading expert in materials science for electronics applications. Prior to Meta, Dr. Toleno was director of new technology at Microsoft, working on the

Via Filling Solutions



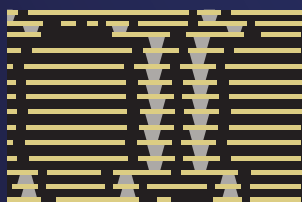
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This image shows circuitry formed with SW series on glass substrate.

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CA People



Arch Systems appointed **Benjamin Freeman** vice president of engineering. Freeman specializes in analytics and technology-assisted optimization of physical processes.

Restronics Mid Atlantic named **Matthew Osborne** managing partner.

Sanmina promoted **Rodrigo Sierra Avila** to acting plant manager, Guadalajara.

Yamaha Motor Europe SMT Section appointed **Kamil Stasiak** product marketing manager.



Yamaha named **Andy Wittbrodt** key account manager. He joins Yamaha with 27 years of technical sales and service operations experience in electronics.



Zestron Americas appointed **John Neiderman** US and Canada sales manager. Neiderman has over 20 years of sales and technical experience in electronics manufacturing.

CA Briefs

Absolute EMS installed a **VJ Electronix** XQuik II Plus.

AIM Solder signed **Cabiotec** as distributor for its full line of products in Italy.

Alpha Circuit purchased and installed two Galaxy 30µ AOI machines.

Cobham Mission Systems purchased a photon steam aging system from **Hentec Industries/RPS Automation**.

Cogent Technology installed a **YJ Link** YLM laser marker.

Compal and **Pegatron** are reportedly expanding production in Vietnam, while Vietnam is poised to increase minimum wage amid rising inflation.

DICA Electronics deployed a **Pleora Technologies** visual inspection system.

Flex is building a new 145,000 sq. ft. facility in Jalisco, Mexico. The site will serve as an in-region automotive manufacturing hub.

GJD Manufacturing invested in a **Hanwha Techwin** SM482Plus SMT line.

Incap Slovakia added a selective soldering machine and a new SMT line to its Námestovo factory.

Hololens and director of global product management for underfills and encapsulants at Henkel. He was also a director of SMTA. He has a doctorate in chemistry from Penn State University and a bachelor's of science in chemistry from Ursinus College.

His talk takes place Oct. 5 from 11 a.m. to 12 p.m. at the Santa Clara (CA) Convention Center. There is no fee to attend Dr. Toleno's presentation, but advanced registration at pcbwest.com is required.

"Virtual reality is much further along than many people realize," said Mike Buetow, conference director, PCB West. "It has more daily transactions than the two largest digital currencies combined. Dr. Toleno has a deep knowledge of electronics manufacturing, and I can't think of a better person to explain the computing requirements from the cloud, the edge and localized devices this future will require."

PCD&F's Annual Designers' Salary Survey Open

PEACHTREE CITY, GA – PRINTED CIRCUIT DESIGN & FAB is undertaking its annual salary survey of printed circuit board designers, design engineers and other layout specialists.

Results will be published in an upcoming issue of PCD&F. The data collected are revealed only in the aggregate, and no individual data will be revealed.

Designers for years have taken advantage of the results to benchmark their salaries, benefits and credentials against peers. The survey link is here: <https://www.surveymonkey.com/r/N989JS3>.

Because this is a survey, not a poll, the audience being surveyed is not selected or controlled.

Vector Fabrication to Invest \$60M in Vietnam PCB Plant

DA NANG, VIETNAM – Vector Fabrication has received an investment license for a PCB and MEMS factory, with plans to invest \$60 million, according to reports.

The factory is expected to be 40,000 sq. m., and the first phase is expected to begin in the first quarter of 2025. The plant plans to begin manufacturing MEMS as of the first quarter of 2027.

The fabricator will build two-, four-layer and multilayer PCBs, probe cards and IC burn-in boards.

Vector reportedly develops substrates for Intel.

Ampel Acquires US Circuit, RMC

ELK GROVE VILLAGE, IL – Ampel has acquired fellow fabricators Rocky Mountain Circuits and US Circuit for an undisclosed sum.

Production at Boulder, CO-based Rocky Mountain Circuits is shutting down, and existing orders will be moved to Ampel and US Circuit.

RMC will maintain a sales and engineering support office, however.

Ampel was founded in 1983 and also owns Lazer-Tech, Image Circuits, Tritech PCB, PC Specialties, Crimp Circuits and Texas Circuitry.

Nitto Acquires Bend Labs

FARMINGTON, UT – Nitto Denko acquired Bend Labs for an undisclosed sum.

The sensor device technology company merged into Nitto, starting business as Nitto Bend Technologies.

Bend's flexible sensor measures bend, stretch and force. The flexible sensor is expected to meet automation demands in the automotive field and remote monitoring

Support For Flex, Rigid Flex and Embedded Component Designs Now Available.



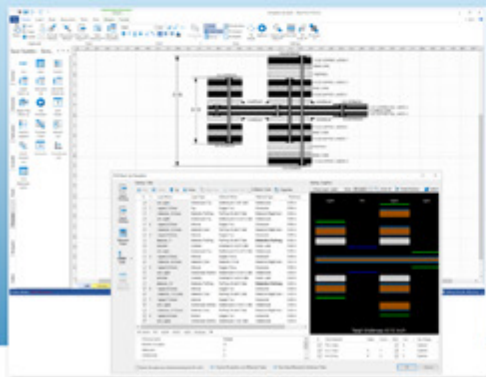
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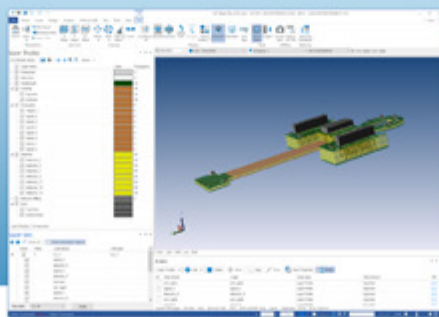
CAM350

DownStream's CAM350 and BluePrint-PCB support importation and visualization of PCB designs containing Flex, Rigid Flex or Embedded components. Visualize designs in both 2D and 3D, and easily document complex Flex or Rigid-Flex Stack-Ups for submission to PCB Fabricators.

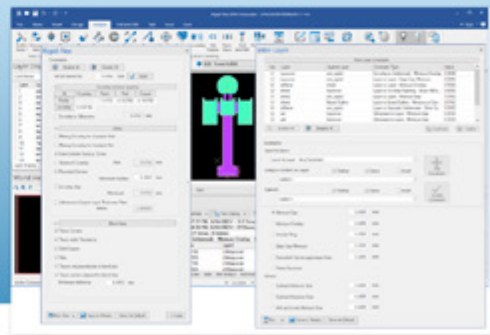
- Import and Visualize Flex, Rigid-Flex and Embedded Component Designs
- 3D Visualization to Validate PCB Construction and Component Assembly
- Manage Variable Stackup Zones for Rigid-Flex Designs
- Easily Create Custom Flex or Rigid-Flex Fabrication and Assembly Documentation
- Use DFM analysis to analyze a flex or rigid-flex design for potential fabrication or bend related defects



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A rigid-flex design in 3D. Shown with layers spread to improve visualization of the layer stackup.



Use Rigid-Flex and Inter-layer DFM analysis to analyze flex and rigid-flex designs.



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Infestos Sustainable Solutions said it would initiate buyout proceedings for all outstanding ordinary shares of **Newways Electronics**. Infestos currently owns more than 95% of the company's shares.

iNEMI was awarded \$290,865 from the **National Institute of Standards and Technology's** Advanced Manufacturing Technology Roadmap Program to develop a 5G/6G roadmap.

IPC established a subsidiary in Munich.

Jabil announced a manufacturing collaboration with **Cardo Systems**, a maker of wireless group communications and entertainment systems for motorcycle riders.

Jaltek opened a new EMS facility near Luton, UK, that increases its manufacturing space by 50%.

Omega EMS is producing **Eguana Technologies** products in San Jose.

PDR Rework Systems hired **Restronics** as manufacturers' representative in Southern California.

Pektron purchased 15 **Yamaha** YRM20 placement machines.

Pro-Active Engineering integrated an **ASM** DEK NeoHorizon screen printer and three SiplaceTX placement platforms at its EMS plant.

PVA received a patent in Japan for an optical bonding machine with cure in place and visual feedback.

A **Sky One France** subsidiary has acquired EMS provider **Malaga Aerospace Defense & Electronics Systems SAU (MADES)** from **American Industrial Acquisition Corp. (AIAC)**. Terms were not disclosed.

SMarTsol Technologies added **Austin American Technology** to its line card in Mexico.

Stewart Technology added two **Nordson** Cerno 300.1S selective soldering systems to its production facility in Tweedbank, Scotland.

Spain's government has approved a plan to spend €12.25 billion on the semiconductor and microchip industry by 2027, Economy Minister Nadia Calvino said, including €9.3 billion to fund the building of plants.

ViTrox Technologies named **Ostec-SMT** sales channel partner in the Russia region.

VJ Electronix appointed **Southwest Systems Technology** to represent its component counting systems in Texas, Oklahoma, Arkansas and Louisiana.

Yekani closed its manufacturing facility in South Africa and auctioned off the assets.

in the digital healthcare field. Nitto anticipates this technology to be used in sports and robotics as well.

The impact of this acquisition on Nitto's consolidated earnings forecast for 2022 is insignificant.

Nitto develops new products and services in three domains: information interface, next-generation mobility and human life.

PCB Technologies Launches SiP Subsidiary iNPACK

OCEAN TOWNSHIP, NJ – PCB Technologies is launching a subsidiary to provide system-in-package solutions. Beginning this month, iNPACK will focus on high-end technology that contributes to improved signal integrity and reduces unwanted inductance effects.

iNPACK will provide SiP, semiconductor packaging, organic substrates (25µm lines and 25µm spacing), and 3-D, 2.5-D and 2-D packaging solutions for aerospace, defense, medical, consumer electronics, automotive, energy and communications industries.

"The new company incorporates innovative interconnects as part of its substrates and micro-assembly process capabilities," said Jeff De Serrano, PCB Technologies' president for North America. "Our technological solutions can more than double the electronic functionality in the same form factor and create substrate-like PCBs. To top it off, our lead times are only six months long. The goal is to support our customers from design concept to production, all under the same roof, while utilizing unified design rules."

GPV, Enics to Merge, Creating Europe's 2d Largest EMS

VEJLE, DENMARK – Europe's EMS industry was shaken up in June as GPV and Enics announced a pending merger to form the continent's second-largest EMS company with more than 7,500 employees and annual revenue of more than DKK 7 billion (\$990 million).

The transaction values the combined business at more than DKK 4 billion (\$566 million). Closing is subject to customary approvals, including from antitrust officials.

Danish industrial conglomerate Schouw & Co., listed on Nasdaq Copenhagen, will hold 80% of the merged entity, while the current owner of Enics, Ahlström Capital will hold 20%. Additionally, as a result of the transaction, Ahlström Capital will receive approximately EUR 60 million (\$63.1 million) in cash. The merger will create an international electronics group with more than 7,500 employees.

"This is a combination of two equally strong and very competent companies," said Bo Lybæk, CEO, GPV. "With the merger, we take yet another significant step on our growth journey. In 2018, we successfully acquired the Swiss electronics manufacturer CCS, which had revenue of DKK 1.6 billion. That lifted GPV into the top 10 of EMS companies in Europe, and we have since delivered solid results. Based on our track-record from the integration of CCS, we're now looking to repeat the success. Together with Enics, we're creating the second-largest EMS group headquartered in Europe."

Lybæk will lead the integration of the two businesses into the new combined company.

"Schouw & Co. and Ahlstrom Capital share similar values and both companies' legacy and long-term strategic outlook provided an excellent climate for negotiation," said Jens Bjerg Sørensen, chairman, GPV. Sørensen will become chairman of the merged company.

"At Schouw & Co., we have a clear strategy of making long-term investments in market-leading companies. With the merger between GPV and Enics, we will now create a leading player that can measure up to even the largest EMS companies, and which within a foreseeable number of years can reach DKK 10 billion in revenue," Sørensen added.

Following the deal, the merged entity will be Europe's second largest EMS com-

pany, behind Zollner.

Enics is among the industrial leaders in design, lean manufacturing, and development of test systems for some of the world's largest customers, while GPV is a full-service EMS provider specializing in managing high-mix product portfolios, application design and engineering for a strong range of market-leading customers.

"Enics and GPV are a perfect match. I look forward to laying the foundation for this strong European industrial platform. Together, both companies have even stronger capabilities to provide turnkey offerings that will make the combined company a success in the fast-changing EMS market. I'm confident that together we will be driving the sustainable success of our customers and leading the way to change how EMS companies operate in complex ecosystems," said Elke Eckstein, CEO, Enics.

Enics has seven factories in Europe and Asia across Finland, Sweden, Estonia, Slovakia, China, and Malaysia, while GPV has 12 factories located in Denmark, Switzerland, Germany, Austria, Slovakia, Mexico, Sri Lanka, and Thailand. Enics is focused on electronics manufacturing and test, while GPV also specializes in product application design, in-house mechanics, and cable-harness assemblies. GPV has been particularly successful with its box-build mechatronics products, an area where both Eckstein and Lybæk see great potential going forward, including for Enics' current customers.

Most of Enics' and GPV's customers are in the industrial segment.

Align Capital Partners Acquires StenTech

MARKHAM, CANADA – Align Capital Partners has acquired StenTech for an undisclosed sum.

StenTech provides surface mount technology stencils, pallets, tooling and related components.

The company boasts more than 2,000 customers across North America.

Proposed IPC Standard for Green Cleaners Open for Public Review

BANNOCKBURN, IL – A draft version of IPC-1402, Standard for Green Cleaners Used in Electronics Manufacturing, is now open for public review. The draft standard has been progressing through the standards process since fall of 2021 and, despite some minor delays in the draft development timelines – as is common during consensus-based standards development processes – the draft is now ready for public review through Jul. 15.

The draft IPC-1402 standard has been developed by volunteers and key governmental agencies from Asia, Europe and North America. This first-of-its-kind standard for the electronics manufacturing industry defines and sets minimum criteria for green cleaners – chemical cleaners meeting a defensible set of green chemistry requirements – used in electronics manufacturing processes. Also, this standard provides a core set of foundational environmental, health and safety requirements that aim

to reduce impacts and improve the safety of cleaning products.

IPC encourages personnel whose company uses chemical cleaners on electronic products or components, or on machines and tooling used during operations and maintenance, to review the draft standard and provide comments to the authoring task group.

The draft document is freely available, and reviewers can participate in the process by submitting comments about this draft industry standard by mid-July. Reviewers can request a copy of the draft document and instructions on how to submit comments by emailing answers@ipc.org.

At the end of the public review period, comments will be consolidated, and the standards development team will work toward resolution of comments. Then, the final document will move to the ballot group for consensus vote. IPC-1402 is expected to be released in mid-December.

PG Technoplast to Invest \$41M in Maharashtra, India

UTTAR PRADESH, INDIA – PG Technoplast signed a memorandum of understanding with the government of Maharashtra to invest Rs 3.15 billion (US\$41 million) in the state, according to reports.

The electronics manufacturing services provider has eight production sites in India. The company will work with Maharashtra Industrial Development Corp. to create the region's largest room AC manufacturing capacity.

"We are grateful to the government of Maharashtra for facilitating PG's push to provide its customers turnkey solutions for all home appliances," said Vikas Gupta, MD-Operations, PG Group. "The move will help bring room AC manufacturing to the Western region of the country, which historically has been concentrated in the Northern, and now Southern, parts of the country."

In the fiscal third quarter, the firm's net profit declined 2.6% to Rs 63.3 million, and sales increased 45% to Rs 2.7 billion compared to the same period last year.

GPV to Construct Mechanics Factory in Thailand

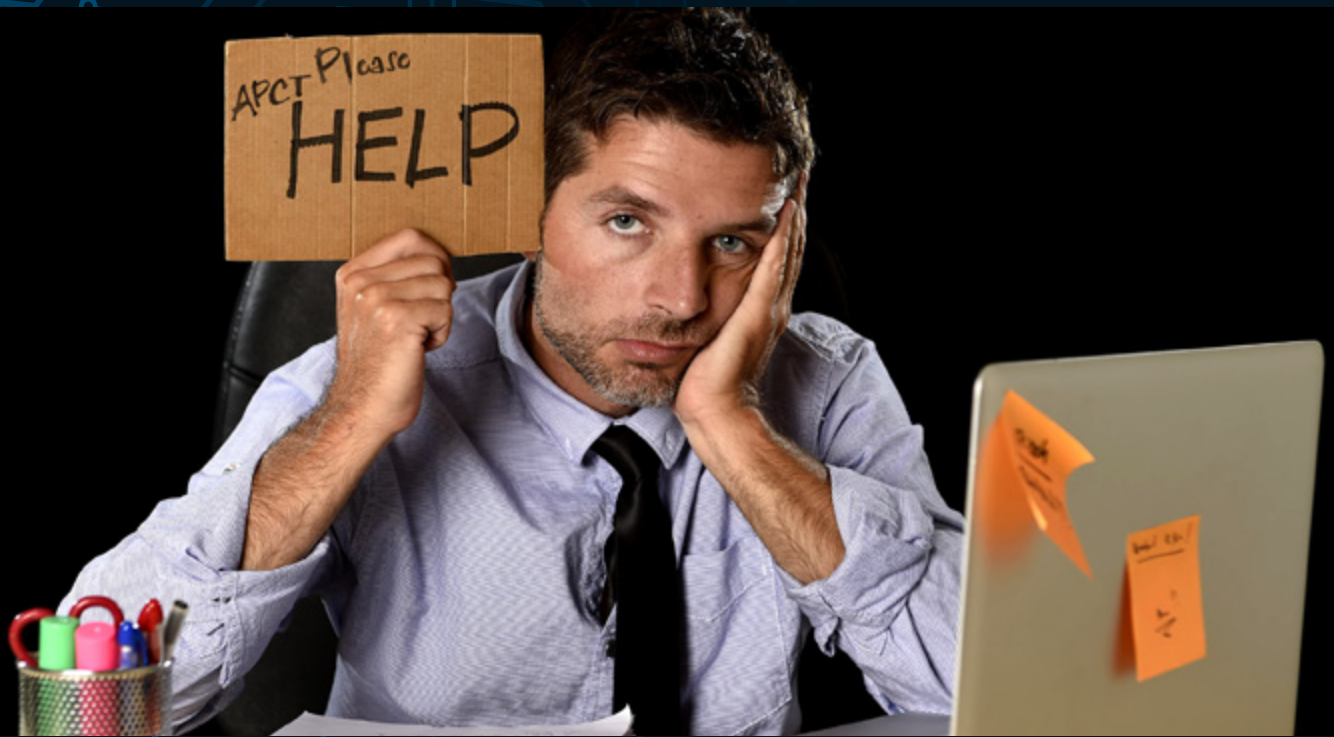
PHRAEKSA, THAILAND – GPV Mechanics is constructing a 12,000m² mechanics manufacturing factory in Thailand. The facility will be built with room to grow, say reports.

"We are very much looking forward to serving our customers from the new factory in 2023. The main piling ceremony is an important first step in going forward with the construction work. Safety of our employees is key, and so is the safety of all involved in the construction of our new production facility. Our ambition is to execute the building construction with zero LTIs," said Bjørn Fiskers, managing director.

GPV currently has 7,100m² mechanics production and 15,000m² electronics production in Bangkok.

The company is also building a new 11,300m² electronics manufacturing facility in Sri Lanka. □

Is Your Current PCB Supplier Pushing Out Lead Times That Are Unthinkable?



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TECHNOLOGIES

RIGID

Standard:

2 – 28 Layers

Advanced:

30 – 38 Layers

Development (NPI only):

40+ Layers

HDI; BLIND/BURIED/STACKED VIA

Lam Cycles:

Up to 8x

Micro BGA Pitch:

.2 Millimeters

FLEX / RIGID-FLEX

Standard Flex:

1 – 6 Layers

Rigid Flex:

4 – 22 Layers

Rigid Flex HDI Lam Cycles:

Up to 2x

LEAD TIMES

RIGID

Standard:

20 Days

2 – 10 Layers:

24 Hours

12 – 24 Layers:

48 Hours

HDI; BLIND/BURIED/STACKED VIA

Via in Pad:

72 Hours

HDI:

5 – 15 Days*

** Depending upon # of Lam Cycles*

FLEX / RIGID-FLEX

Flex 1 – 6 Layers:

5 – 15 Days

Rigid Flex 4 – 22 Layers:

7 – 15 Days

Rigid Flex HDI 2x Lam Cycles

20+ Days

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Printed Circuit Board Solutions

Report: 70%+ of Electronics Supply Chain Lead Times to Increase into 2023

PASADENA, CA – Through the first quarter of 2023, more than 70% of lead times are forecast to increase, according to Supplyframe. During that time frame, analog, complex semiconductor (ASICs, MCUs, MPUs, PLDs), flash memory, non-ceramic capacitor, resistor and standard logic devices are forecast to rise in price with very limited exceptions. Most of the same devices will also remain at or exceed already elevated lead times.

From analog power to standard logic to ASICs and sensors, the active components market will be swimming in a sea of red indicators for the next four quarters. This is happening as strong demand continues; production is at capacity; there are extended lead times; and rising prices plague most devices.

Passive components are not as constrained as active ones. However, like active components, passive commodities also suffer from raw material challenges and labor shortages. □

PERIPHERAL PLUMMET

Trends in the US electronics equipment market (shipments only)	% CHANGE			
	FEB.	MAR.	APR.	YTD%
Computers and electronics products	1.3	-0.3	0.5	4.6
Computers	4.2	-2.9	1.5	-2.0
Storage devices	1.8	-0.7	5.2	11.0
Other peripheral equipment	6.3	7.2	-10.8	3.0
Nondefense communications equipment	1.3	-3.1	1.1	9.2
Defense communications equipment	-1.9	-3.3	5.9	9.3
A/V equipment	0.0	5.0	0.9	46.5
Components ¹	2.2	-0.1	0.1	13.8
Nondefense search and navigation equipment	0.4	-1.8	2.5	1.2
Defense search and navigation equipment	1.5	-1.7	0.4	0.2
Medical, measurement and control	0.6	0.3	1.4	1.3

¹Revised. ²Preliminary. ³Includes semiconductors. Seasonally adjusted.

Source: U.S. Department of Commerce Census Bureau, June 2, 2022

US MANUFACTURING INDICES

	JAN.	FEB.	MAR.	APR.	MAY
PMI	57.6	58.6	57.1	55.4	56.1
New orders	57.9	61.7	53.8	53.5	55.1
Production	57.8	58.5	54.5	53.6	54.2
Inventories	53.2	53.6	55.5	51.6	55.9
Customer inventories	33.0	31.8	34.1	37.1	32.7
Backlogs	56.4	65.0	60.0	56.0	58.7

Source: Institute for Supply Management, June 1, 2022

Hot Takes

- **Global semiconductor equipment billings** grew 5% year-over-year to \$24.7 billion in the first quarter. Sequential billings in the seasonally soft first quarter declined 10%. (SEMI)
- **Total semiconductor sales in 2022** are forecast to increase 11%, the same growth rate that was forecast in January. (IC Insights)
- **Tech manufacturing plants** are operating at 87% capacity, and that's expected to increase 5.8% throughout 2022. Capital expenditures are forecast to grow 7.2% during the same period. (Institute for Supply Management)
- **The worldwide infrastructure as a service (IaaS) market** grew 41% in 2021 to total \$90.9 billion, up from \$64.3 billion in 2020. Amazon retained the No. 1 position in the IaaS market in 2021, followed by Microsoft, Alibaba, Google and Huawei. (Gartner)
- **Despite chip demand showing signs of a downturn** since the start of 2022, the capacity expansion spree at foundry houses seems unstoppable, sparking concerns that overcapacity may hit the global foundry market in 2024. (DigiTimes)
- **Samsung remained the world's largest DRAM supplier** in 2021, with sales of nearly \$41.9 billion and 44% market share. (IC Insights)
- **Seventy-eight percent of CFOs plan to maintain or increase enterprise-wide digital investments** in the next two years. (Gartner)
- **The augmented reality market** was worth \$9 billion in 2021 and is estimated to grow to \$150 billion by 2030. (Research and Markets)
- **Sixty-three percent of executives plan to make compensation adjustments** in response to high inflation. (Gartner)
- **Smartphone production** fell 13% sequentially in the March quarter to 310 million units. (TrendForce)
- **Smartphone shipments** will decline 3.5% to 1.31 billion units in 2022. (IDC)
- **The automotive testing inspection and certification market** was valued at \$22.9 billion in 2020 and is expected to grow at a CAGR of 4.7% over the forecast period to reach \$31.6 billion by 2027. (Research and Markets)

KEY COMPONENTS

	DEC.	JAN.	FEB.	MAR.	APR.
EMS (North America) ¹	1.55	1.58	1.52	1.44	1.36
Semiconductors ²	28.3%	26.8%	26.2%	23% ^r	21.1% ^p
PCBs ³ (North America)	1.17	1.18	1.16	1.05	1.03
Computers/electronic products ⁴	5.32	6.46	6.38	6.45 ^r	6.39 ^p

Sources: ¹IPC, ²SIA (3-month moving average growth), ³IPC, ⁴Census Bureau, ^ppreliminary, ^rrevised



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Innovative Technology: Enabling or Disruptive?

Fabricators and designers must communicate about new technology to verify its viability.

MORE OFTEN THAN not over the past couple of decades, new technologies, processes and options we fabricators have been asked, begged or threatened to add to our repertoire of offerings were ones that could be best considered disruptive. What's disruptive to a manufacturer may seem benign to the casual eye, as often the technology – or process – that is most disruptive is a simple one.

Indeed, sometimes that technology is nothing more than the rebirth of an older, tried-and-true, albeit significantly tweaked, process. REACH, and the prior RoHS, caused much disruption, and yet most of the plating chemistries and surface finishes in use today are essentially highly refined formulas of older plating technologies such as ENIG, silver and tin.

Old or new, disruptive technologies tend to be challenges for several reasons. First is understanding the technology and how to process it so it works as intended. Second is determining what equipment is needed to cost-effectively and robustly apply the new technology. Finally, finding enough customers to consistently order product that uses the technology, so everyone remembers what it is and how to process it!

Truly new paradigm-shifting technologies hit the scene as “must haves” so a product can function. While disruptive to manufacturers, in some ways the more off-the-wall a technology seems, the easier it is to decide whether to embrace it or wait to see if it sinks under the weight of its own hype. These disruptive technologies more typically challenge everyone to understand not only how to apply them, but how to measure success or failure so yields and costs can be determined.

In all cases, what makes disruptive technologies so unruly boils down to two issues: First is the learning curve and capital investment needed to provide the technology, and second is gaining consensus among customers that the technology is a better alternative to more traditional technologies, and they will purchase enough to warrant the human and capital investment. Probably most frustrating for fabricators is when a buyer provides no apparent reason other than “because” for specifying a new technology. The fabricator's goal is to supply quality product they understand and can safely and consistently produce, not (inadvertently) become a customer's R&D center, with the concurrent risks and costs.

Every new technology has at least two sides. At a recent industry gathering, a supplier mentioned a current disruptive technology we had difficulty working our way through was only one of a slew of new

“enabling” technologies available to the industry. Enabling? Not to me. That is when the communication gap between design application and manufacturing competence became evident. As this conversation continued, I heard a different spin as to why a particular new technology was being specified. Understanding the benefits from the end-product perspective began to make sense and explained why this customer would have specified it, as well as why its use may become widespread in the future. The tutorial was strictly from a value-add design perspective, and it was compelling. When asked if the design community knew of the fabrication challenges the new technology caused that impacted yield and lead times, in addition to cost, the answer was honest: “Probably not.”

What's enabling to one party can be disruptive to another. Fabricators often do not understand the nuances of pushing design to meet challenging performance objectives but do fully understand robust, time-proven manufacturing techniques. Equally, when a designer chooses to move toward a new technology, they may be excited by the functionality it offers but most likely is unaware manufacturing the board could lead to lower yield, longer lead times and ultimately higher costs.

The real issue is understanding the risks involved with embracing – or ignoring – new technology. The risks include, “Will it work, or will it only work if executed flawlessly? Will the new technology pass the test of time? Most important, will widespread use of the technology lead to cost-effective processes or equipment to ensure consistency from one application to another and from one supplier to another?”

As a fabricator, it is more important now than ever to be in touch with customers' designers to understand what they are attempting to accomplish. Equally for designers, it is essential they are in contact with all their PCB suppliers, especially the behind-the-scenes process gurus, so everyone understands the manufacturability of new technology in the real world of the shop floor.

This gets back to the need for suppliers knowing their customer and customers knowing their suppliers – and not just at the buyer/sales rep level but at the designer/manufacturing engineer level. Knowing the intended end-result a new technology enables, as well as how disruptive that technology may be when

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appears monthly.



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All Wet: PCB Packaging, Shipping and Storage

Limiting PCB moisture absorption is the full responsibility of the supplier.
How to pack boards right.

PCB SUPPLIERS WHO use good packaging methods are keeping their products safe from physical damage incurred during transit from the manufacturing facility to customers' warehouses. Equally important, these packaging practices help ensure shelf-life expectancy by preventing moisture absorption.

To protect their orders, PCB buyers should require suppliers strictly follow corporate shipping specifications. Nothing is more frustrating than waiting for quality product to be built, only to have it damaged because of poor packaging practices. It's just as frustrating when boards become useless while sitting on the shelf.

PCBs can be very heavy. Their sharp corners sometimes wreak havoc on the corrugated cardboard boxes in which they are shipped. A good freight spec should state boards are to be vacuum-packed with a bubble wrap base, with no more than 25 boards to a stack. When a board is oversized or heavier than normal, 10 to 15 pieces is the best option. Whatever number is used, the packaging should be consistent in count for a particular shipment.

Extra care should be taken for flexible or very thin, rigid PCBs less than 0.028" thick. They should be packaged with stiffening material on the top and bottom of the bundle to help prevent warping.

A humidity indication card (HIC) and desiccant are to be placed within the package as well. The HIC should be placed inside on top of the PCBs for easy review. The desiccant should be placed along the side or edge of the bundle, so it doesn't contribute to bending or warping caused by the stress of the vacuum packaging.

Each PCB bundle should have a sticker affixed detailing the part number, date code and number of pieces per bundle. More than one date code of the same product may be shipped together if they are segregated and marked as such.

X'd-out panels, if allowed by your PCB fabrication specifications, should be packaged separately and clearly marked.

The individual packages of PCBs should be placed tightly in a box, with Styrofoam or other shock-absorbing material placed between the packages and the wall of the shipping container. The PCB corners should be protected, as they can be easily dinged or dented while in transit.

The weight of each box should not exceed 30 lb. Boxes may have exterior strapping applied when the PCBs are oversized or heavier than normal.

Each box should have a sticker on either end identifying

its contents, including the part number, purchase order number, date code and number of pieces within the box.

Each part number shipped should come with a packing slip and "proof of quality" documentation, including (but not be limited to):

- The certificate of compliance
- A first article or dimensional report
- A microsection report to include a solderability test with a cross-section
- An electrical test report
- An ionic contamination report
- A TDR report (controlled impedance, when applicable)
- Any material certifications
- Any other documentation required by the purchase order.

When the product is shipped, the supplier should notify the customer's purchasing, receiving and accounting departments of shipment method and tracking number. The commercial invoice and electronic copies of the quality paperwork should be included in case such documentation for the shipment is lost in transit.

As crucial as proper PCB packaging is, the storage of the boards once they reach the customer is just as vital. Other than opening one of the packages to verify the PCBs meet the criteria of the print and the documentation received, the best bet is to leave the boards in their original packaging.

A bare board begins to absorb moisture immediately upon leaving the factory. The amount of moisture absorbed depends on a variety of factors, including:

- Base material used in manufacturing
- Manufacturing environment
- Packaging method
- Shipping temperatures (from the cold bellies of aircraft or the humid transit of a sea shipment to hot delivery trucks)
- Customer storage and inventory procedures.

Vacuum sealing and the use of desiccant only delay or lessen moisture absorption. They do not prevent it.

The longer a PCB is stored on a shelf, the greater the chance it will absorb moisture, which can manifest in the assembly operation as delamination. Delamination is caused either by moisture or manufacturing defects. If a problem PCB is determined to be structur-

GREG PAPANDREW

has more than 25 years' experience selling PCBs directly for various fabricators and as founder of a leading distributor. He is cofounder of Better Board Buying (boardbuying.com); greg@directpcb.com.



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PCE-EDU, Inc.
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The comprehensive curriculum specifically for
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The **Printed Circuit Engineering Professional** curriculum teaches a knowledge base and develops a competency for the profession of printed circuit engineering layout, based on current technology trends. It also provides ongoing reference material for continued development in the profession. The 40-hour course was developed by leading experts in printed circuit design with a combined 250 years of industry experience and covers approximately 67 major topics under the following headings: Basics of the profession, materials, manufacturing methods and processes; circuit definition and capture; board layout data and placement; circuit routing and interconnection; signal-integrity and EMI applications; flex PCBs; documentation and manufacturing preparation; and advanced electronics (energy movement in circuits, transmission lines, etc.). Class flow: Books sent to students prior to an instructor lead review. This is followed by an optional exam with a lifetime certification that is recognized by the PCEA Trade Association.

The course references general CAD tool practices and is vendor-agnostic. Instructors include Mike Creeden, CID+, who has over 44 years of industry experience as an educator, PCB designer, applications engineer and business owner; and Tomas Chester, P.Eng., CPCD, who has designed over 100 circuit boards through all phases of the product lifecycle, and managed a variety of multifaceted, interdisciplinary projects, from simple interconnect designs to complex microprocessors.

For Information or Registration:

<https://pcea.net/pce-edu-design-engineer-curriculum/>

Upcoming Class Openings: *More added each month!*
July 11-15



AUTHORS



Mike Creeden



Gary Ferrari



Susy Webb



Rick Hartley



Steph Chavez

Printed Circuit Engineering Professional

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ECTC Highlights Next-Generation Packaging Challenges

Large crowds mulled the latest substrate trends and new developments in 3-D IC hybrid bonding.

The IEEE Electronics Components and Technology Conference (ECTC) returned to an in-person conference at the end of May with more than 1,500 attendees, domestic and international. Attendance in San Diego matched pre-pandemic numbers. While some presentations remained virtual, using video recording, many were onsite. A variety of electronics packaging topics were discussed. Judging by the crowded rooms, this year's hot topic was 3-D IC hybrid bonding.

Advanced packaging. A pre-conference Heterogeneous Integration Roadmap workshop discussed trends in networking for the future and new developments in advanced packaging for high-performance computing and data centers. The workshop concluded with a panel of presenters discussing the latest trends in medical health and wearables.

Plenary sessions covered some of the latest topics. The MicroLED display session focused on high-volume manufacturing progress and challenges. In a session on the evolution of IC substrate technology, panelists from Intel, Amkor, Ajinomoto, AT&S and Atotech discussed the latest substrate trends.

The special session – Meeting Next Generation Packaging Challenges from Chiplets to Co-packaged Optics – included panelists from AMD, Cisco, Marvell and Synopsys (**FIGURE 1**). Panelists discussed the importance of co-design and changing the approach to design, including system-level design. The combination of digital and photonics is coming. Integrating this in 3-D will include the laser, modulator, filters and detectors. Interfaces and the design platform are important for robust manufacturing, including product quality, debug and traceability, and in-field optimization. The

panel concluded that, with increased use of chiplets, continued work is required in the areas of test and known good die (KGD), thermals, power deliver and system-level integrity. Adoption of standards such as the recently introduced UCIE is important to align the industry around an open platform to enable chiplet-based solutions. Thermal management remains one of the major bottlenecks with 3-D.

A special night session focused on the US Department of Defense (DoD) in the state-of-the-art heterogeneous integration (SHIP) program. The opening statement from the office of the Undersecretary of Defense for Research and Engineering explained the backdrop of the program. Speakers from Intel and Qorvo, recipients of US government funding, described their activities. Qorvo is focused on RF, and Intel is focused on high-performance computing with its embedded multi-die bridge (EMIB) technology. The panel admitted that, in the absence of a volume supplier of buildup substrates, the DoD depends on a global substrate procurement strategy.

A session on diversity and career growth provided advice from a panel of experts, including representatives from IBM, Lam Research, Edwards and Cadence. The plenary session covered digital transformation with participation from Intel, TSMC, Yole, Onto Innovation and Samsung. A late-night session focused on Interconnect Technologies for Chiplets with participants from Intel, IBM, Unimicron, TSMC, SPIL and Furukawa Electric. Participants from Taiwan and Japan dialed into the session to discuss topics including embedded bridge, the incorporation of memory in advanced package developments in optical packaging, 3-D packaging and substrates.

Adapting to substrate shortages.

With the continued substrate shortage, companies focused on the potential for a fan-out wafer level package (FO-WLP). Numerous presentations covered several options, with new applications for fan-out discussed. SK Hynix discussed the potential for memory applications. IME A*Star discussed FO-WLP antenna-in-package (AiP) for automotive radar applications. Researchers at UCLA described their work on FO for micro displays. RFcore discussed FO-AiP for 5G mmWave applications. Amkor, ASE and Samsung presented package options for FO-WLP.

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FIGURE 1. A special panel on packaging challenges. Panelists included (from left) Kevin O'Buckley (Marvell), Raja Swaminathan (AMD), Ming Zhang (Synopsys), Ravi Mahajan (Intel), Sandeep Razdan (Cisco Systems), and moderator Jan Vardaman (TechSearch).

Processing FO in a panel has been proposed as a way to lower the cost by increasing the number of parts with large-area processing. Fraunhofer and the Technical University of Berlin discussed the technology limits of panel processing, describing warpage and die shift as the major issues. Layout adaptation is promoted to overcome die-shift challenges on large panels. Samsung Electronics discussed the reliability of the via structure in its FOPLP line. Amkor introduced its 650mm x 650mm panel line. Nepes provided reliability data on FO packages fabricated on its new panel line based on Deca M-Series technology (FIGURE 2). Deca Technologies described 20µm device pad pitch with its M-Series process. The use of adaptive patterning provides a way to handle die shift. Dai Nippon Printing introduced its panel-based RDL interposer with a 2µm pitch semi-adaptive process for chiplet integration.

Several presentations focused on new substrate options, including glass as a substrate and RDL interposers. Developments in glass substrates were introduced with papers from Korea Electronics Technology Institute and Georgia Tech. TSMC introduced its organic interposer CoWoS-R+ technology that replaces the silicon interposer with an RDL structure. The plus indicates the integration of a large amount of high-density integrated passive devices (IPDs) that serve as decoupling capacitors. The integrated de-cap capacitors suppress the power domain noise and enhance HBM3 signal integrity at a high data rate. Optional silicon connection blocks (bridges) provide high-density die-to-die connections. IBM provided updated work on its direct bonded heterogeneous integration (DBHi) silicon-bridge package, in which the Si bridge is connected to the die and then mounted on the laminate substrate. SPIL provided recent reliability data for its embedded bridge package. Unimicron discussed its hybrid substrate with a buildup film.

3-D hybrid bonding. Three years ago, many ECTC papers focused on R&D activities in hybrid bonding. This year, more than 30 papers discussed hybrid bonding process improvements and new developments. While image sensors have been using hybrid bonding for many years, Sony described their recent work to develop 1µm face-to-face bonding and a new thinning process that minimizes Si thickness variation across

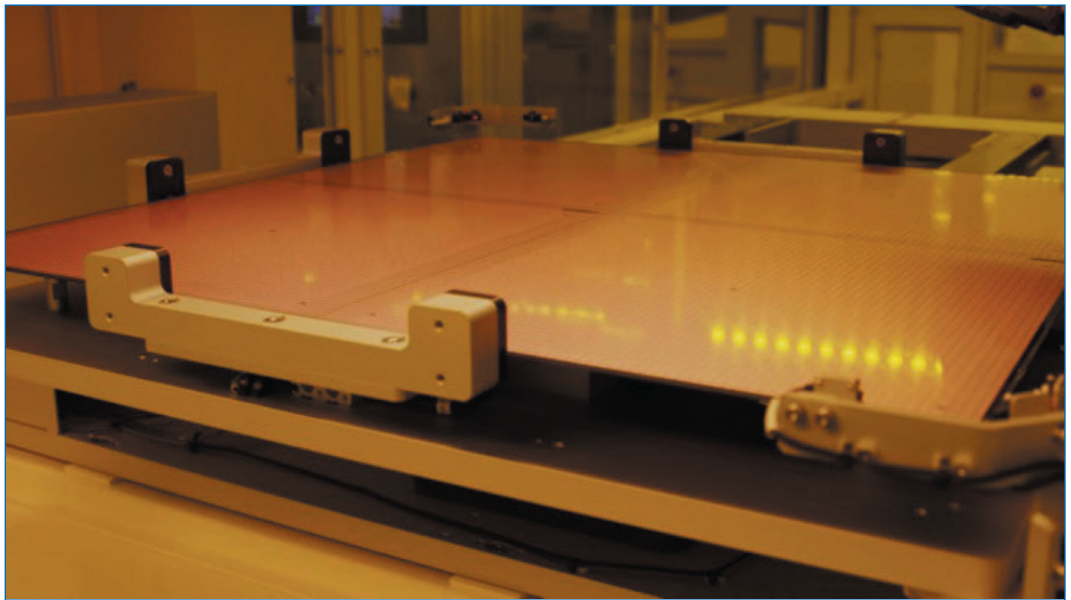


FIGURE 2. The Nepes nPLP 600mm x 600mm fanout panel line reportedly can produce five times as many chips as one 300mm round panel.

the wafer. Adeia's (formerly Xperi) study of the influence of Cu microstructure on the thermal budget shows the possibility of a 20° to 40° reduction in the final anneal temperature. CEA-Leti presented research conducted with Intel on a new die-to-wafer (D2W) collective bonding self-assembly process using water droplets with high alignment accuracy and high throughput. SK Hynix reported the work on wafer-to-wafer (W2S) DRAM stacking for DRAM. Samsung presented several papers on hybrid bonding, including research on controlling bonding voids. AMD described its V-Cache, now in commercial production for servers, desktops and gaming, using TSMC's SoIC process. TSMC described an extension of its SoIC process.

Co-packaged optics. Several presentations focused on co-packaged optics (CPO). Rockley Photonics introduced a fan-out silicon photonics module for next-generation CPO. Rain Tree and IME A*STAR described a heterogeneous integration package using FO-WLP for a hyperscale data center. IBM Canada, GlobalFoundries and others discussed optical fiber pigtail integration for CPO. Cisco described its vision for CPO and challenges in the use of through-silicon vias, including high warpage, optical fiber coupling, and chip-on-substrate assembly. Reliability requirements were also highlighted. A joint paper from EV Group, Tyndall National Institute, IMEC and Ghent University described a high-speed Si photonic switch with a micro-transfer-printed III-V amplifier. ASE described its CPO assembly.

Emerging areas. Presentations also covered additive manufacturing, 3-D printing, developments in packaging and assembly for wearables, and micro LEDs.

Next year's ECTC will be held in Orlando May 30 to Jun. 2. □



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SCHEDULE-AT-A-GLANCE

TUESDAY OCTOBER 4, 2022

Time	Title	Speaker
9:00 a.m. - 10:00 a.m.	Panel: Where is the Design Profession Going?	Mike Buetow, PCEA
10:00 a.m. - 12:00 p.m.	Making Intelligent Material Decisions	Michael R. Creeden CID+, Insulectro
	How to Fight Magnetic Noise Gremlins	Keven Coates, Fluidity Technologies
	Industry Best Practices for Hardware IP Reuse	Stephen Chavez, Siemens
	From DC to AC – Power Integrity and Decoupling Primer for PCB Designers, Situation Today and Outlook for the Future	Ralf Bruening, Zuken
	Back-to-Basics: Understand PCB Fabrication Processes for Traditional, HDI, and Ultra HDI	Mark Hughes, Summit Interconnect
10:00 a.m. - 6:00 p.m.	PCB Design for Engineers	Susy Webb, Design Science
12:00 p.m. - 1:00 p.m.	LUNCH-N-LEARN with Summit Interconnect	
1:00 p.m. - 4:30 p.m.	PCB Designers Guide for Implementing Advanced Semiconductor Package Technologies- Flip-Chip, WLP, FOWLP, 2D, 2.5D and 3D	Vern Solberg, Solberg Technical Consulting
	Circuit Grounding to Control Noise and EMI	Rick Hartley, RHartley Enterprises
	An Intuitive Approach to Understanding Basic High Speed PCB Layout	Keven Coates, Fluidity Technologies
	Effective PCB Design: Techniques to Improve Performance	Daniel Beeker, NXP Semiconductor
	Printed Circuit Fabrication Today: A More Complex Process	Gary Ferrari, Ferrari Technical Services
6:30 p.m. - 7:30 p.m.	Printed Circuit Engineering Association Annual Meeting	

WEDNESDAY OCTOBER 5, 2022

10:00 a.m. - 6:00 p.m. EXHIBITS OPEN

Time	Title	Speaker
10:00 a.m. - 11:00 a.m.	Optimizing the Tool Chain from Design Through Manufacturing for Printed Electronics	David Wiens, Siemens, and Jeff Bergman, NextFlex
10:00 a.m. - 12:00 p.m.	Cables and Connectors: Design for Signal Integrity (Will They Work?) and EMI	Keven Coates, Fluidity Technologies
	Back-to-Basics: Understand the Surface Charge Model of Electricity	Mark Hughes, Summit Interconnect
12:00 p.m. - 1:00 p.m.	FREE LUNCH on Show Floor, sponsored by Sierra Circuits	
1:30 p.m. - 3:30 p.m.	The Mystery of Bypass Capacitors	Keven Coates, Fluidity Technologies
1:30 p.m. - 5:00 p.m.	PCB Antennas for Everyone	Benjamin Jordan, JordanDSP
	Part Placement Choices and Consequences	Susy Webb, Design Science
3:30 p.m. - 4:30 p.m.	Surface Finish Selection Criteria for Next Generation PCB Technologies (5G-HDI-High Frequency-RFMW)- Focusing on Performance & Reliability	Kunal Shah, Ph.D., LiloTree
5:00 p.m. - 6:00 p.m.	FREE EVENING RECEPTION on Show Floor, sponsored by EMA and Ultra Librarian	

WEDNESDAY FREE SESSIONS

10:00 a.m. - 6:00 p.m. EXHIBITS OPEN

Time	Title	Speaker
9:00 a.m. - 10:00 a.m.	Panel: How Heterogenous Integration Affects the PCB Industry	Phil Marcoux
10:00 a.m. - 11:00 a.m.	Dynamic Guidelines for Design with SAP (Semi-Additive Processes)	Tomas Chester, CED, and Tara Dunn, Averatek
	Understanding High Frequency Materials Test Methods for Dk and Df	John Coonrod, Rogers Corp.
11:00 a.m. - 12:00 p.m.	Keynote: Augmented and Virtual Reality, the Next Computer Revolution	Brian Toleno, Ph.D., Meta
12:00 p.m. - 1:00 p.m.	FREE LUNCH on Show Floor, sponsored by Sierra Circuits	
1:30 p.m. - 2:30 p.m.	Evaluating Emerging PCB Technologies Through Industry Collaboration	Madan Jagernauth, HDP
	The 21 Most Common Design Errors Caught by Fabrication (and How to Prevent Them)	Ray Fugitt, DownStream Technologies, and David Hoover, TTM Technologies
2:30 p.m. - 3:30 p.m.	Leveraging CFX-QPL to Integrate Equipment and Create a Smart Factory	Ivan Aduna, Koh Young
3:30 p.m. - 4:30 p.m.	The A+ PCB Outline Drawing	Carl Schattke, PCB Product Development
	IPC-2581's Bi-directional Electronically Executable DFx Exchange Accelerates NPI	Hemant Shah, IPC-2581 Consortium, and Dana Korf, Nano Dimension
5:00 p.m. - 6:00 p.m.	FREE EVENING RECEPTION on Show Floor, sponsored by EMA and Ultra Librarian	

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SCHEDULE-AT-A-GLANCE

THURSDAY OCTOBER 6, 2022

Time	Title	Speaker
10:00 a.m. - 12:00 p.m.	uHDI Design Process Overview and PCB Fabrication	Herb Snogren, Summit Interconnect, and Chris Hunrath, Insulectro
	PCB Layout of Switch Mode Power Supplies	Rick Hartley, RHartley Enterprises
	Electromagnetic Fields for Normal Folks: Show Me the Pictures and Hold the Equations, Please!	Daniel Beeker, NXP Semiconductor
	Ask the Flexperts—Design-Test with Lessons Learned	Mark Finstad, Flexible Circuit Technologies, and Nick Koop, TTM Technologies
	Improving Circuit Design and Layout for Accessibility and Success	Tomas Chester, Chester Electronic Design
10:00 a.m. - 7:00 p.m.	A Guide to RF and Microwave PCB Design	Benjamin Jordan, JordanDSP
12:00 p.m. - 1:00 p.m.	LUNCH-N-LEARN with Polar Instruments	
1:00 p.m. - 2:00 p.m.	Panel: Emerging Technologies and Their Impact on Manufacturing	Tara Dunn, Averatek
2:00 p.m. - 3:00 p.m.	HDI Via Design: Planning the Energy Pipelines	Daniel Beeker, NXP Semiconductor
2:00 p.m. - 5:30 p.m.	Where Does Today's Designer/Engineer Start? Has The Industry Really Changed That Much?	Gary Ferrari, Ferrari Technical Services
	IoT and Low Layer Count PC Board Design	Rick Hartley, RHartley Enterprises
	Heat Management for SMD, LED, and systems 1W to 50W	Keven Coates, Fluidity Technologies
	Designing Boards with Today's BGAs	Susy Webb, Design Science

FRIDAY OCTOBER 7, 2022

Time	Title	Speaker
10:00 a.m. - 12:00 p.m.	Principles of Building a PCB Stackup	Susy Webb, Design Science
	Mechanical Design to Control EMI	Rick Hartley, RHartley Enterprises
	Fan-Out Wafer/Panel-Level Packaging (FOW/PLP) and System-in-Package (SiP)	John H. Lau, Unimicron
12:00 p.m. - 1:00 p.m.	LUNCH-N-LEARN	
1:00 p.m. - 3:00 p.m.	The Mechanical Side of PCBs	Tomas Chester, Chester Electronic Design
1:00 p.m. - 4:30 p.m.	Circuit Design Principles for Flexible and Rigid Flex Circuits- Planning, Design, Fabrication and Assembly Processing	Vern Solberg, Solberg Technical Consulting
	A Multilayered Crash Course in PCB Design	Kirsch Mackey, HaSofu
3:00 p.m. - 5:00 p.m.	Proper PCB Layout of DDR2, 3, 4, etc.	Rick Hartley, RHartley Enterprises



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GS Swiss PCB AG	Polar Instruments, Inc.	Zuken USA Inc.

How to Specify Impedance on a PCB

Determining your optimum geometry, plus two methods for providing data to the fabricator.

CONTROLLING IMPEDANCE (RESISTANCE) is almost a given with today's technology. One day we are adding a wireless option to a common object and calling it the Internet of Things. The next day we're simply keeping up with the competition on processing the code. The trend is toward a greater percentage of the connections falling under the domain of impedance control.

Controlled impedance has two main branches: Single-ended transmission lines are the backbone of RF technology, while differential pairs do the heavy lifting for digital circuits. We'll start with the single-ended lines. They have a start and an end point. The signal is sent one way on the transmission line, and the circuit is completed over the adjacent ground plane.

The main factor influencing impedance is the width of the trace relative to the thickness of the dielectric material between the trace and the ground plane – or planes – used as a reference. What is a reference? It is usually a metal plane with zero volts – “ground” but can have a few volts of its own, either positive or negative relative to what's happening on the trace itself.

A basic rule of thumb is the width of the trace is nearly equal to the thickness of the dielectric material to achieve a 50Ω impedance on the line. The exact number is a product of a number of factors that define the optimum trace width.

Two primary factors determining the trace geometry are the thickness of the copper and the dielectric constant of the material (D_k or ϵ_r). Exotic materials are known for their thermal stability, their tight control over the dk and for a low-loss tangent. Those properties come at a cost. The ceramic materials are typically found in high-frequency and very high-speed applications. Good design practices with FR-4 usually do the trick.

Additional PCB layers above the trace have an impact, as they require a transition between stripline and microstrip

geometry. On balance, the line is normally thinner on the innerlayers, but you're compelled to provide a continuous ground plane on the layer above and below the innerlayer transmission lines.

The presence of solder mask can affect routing on the outer layers to some degree. Any kind of coating or large ferrous metal objects can affect an analog signal. The final line width and construction adjust for those factors.

Differential pairs in the real world. Turning to the digital logic side, our favorite way to spew ones and zeros is to calculate the difference between two matching lines, rather than trying to read a single line that is subject to momentary instances of noise as a voltage spikes across the landscape.

This is how differential pairs are different. Too much can go wrong with a long enough transmission line, and dropped packets are followed by check-sum bytes that do not add up to the number of bytes actually received. Whatever those instructions were, they must be repeated. The user gets beachballs, hourglasses or, heaven forbid, stalled video!

A good microphone cord has the triple connec-

JOHN BURKHERT JR.

is a career PCB designer experienced in military, telecom, consumer hardware and, lately, the automotive industry. Originally, he was an RF specialist but is compelled to flip the bit now and then to fill the need for high-speed digital design. He enjoys playing bass and racing bikes when he's not writing about or performing PCB layout. His column is produced by Cadence Design Systems and runs monthly.



FIGURE 1. A mixed-signal board is always a stretch, with the various functions vying for limited space.

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tion, so it doesn't pick up so much noise from the alternating current fields that flow around wherever they will. My guitar hits with a stronger signal, so the two-wire cord is fine. That's pretty much the two essential methods of data transport.

This plays out on the PCB as well. The second line, along with the ground, forms a balanced circuit. We can use a low voltage and still transmit good data over a fair distance. The common approach is to use edge-coupled lines. They are routed side by side, and the gap between them is a major variable. Loosely coupled lines are noted by the spacing between them being wider than the traces. Conversely, tightly coupled differential pairs have an airgap that is less than the trace width.

So, after determining the optimum geometry for your purpose, it's the fabricator's job to carry this out. They have material and equipment that is hopefully aligned with your goals. Otherwise, keep shopping. Giving the PCB fabricator the data can take one of two forms.

Method 1: Provide a target and let the vendor come up with a plan. First and most common is to have a set of instructions or a table on the fabrication drawing describing the target impedance of traces broken down layer by layer for each impedance type in use. Provide the line width and spacing where applicable, as well as the reference layer(s) for calculating the impedance based on specific materials and processes.

The note/table often reflects what is embedded in the PCB design software as the design rules. It's common to have a callout for every type on any controlled impedance layer designated in the constraints to fill in the blanks.

The board may or may not have used every kind of trace on every available layer. If you cross out the subset of design

rules not in use, it's one question they don't have to ask at tape-out time. Target the information they need by obscuring what is not in play if your flow uses a standard template for impedance.

Method 2: Provide an unwavering set of conditions. The other way is a little more authoritarian in that it establishes an exact type of material through slash sheets and listing other criteria deemed necessary. Then, there is no negotiation on the impedance control, only on the timeline and price for obtaining the material that meets the specifications.

This model served us well at a certain fab-less chipmaker where we could not be sure every type of material was suitable for the demands of Snapdragon chips. When a PCB is sent out for fabrication, the vendor may want to reduce the amount of copper in the via or somehow cut corners. We had data! There were exactly the right number of vias and copper width to get the job done as designed. More than enough would make the chipset bigger. Marketing sets that boundary. It's our job to make it work. We thus required a solid representation of the data, rather than using it as a jumping off point. The words "or equivalent" were strictly enforced.

A good number of vendors are still out there; it's beneficial to keep your options open. If you have a solid relationship with a vendor, they will be able to generate a proposed stackup that meets your needs. That information is applica-

ble to *that* vendor at *that* time. Not much else is guaranteed in this business. Whether you design to their spec or keep using the same rules as always is your business. □

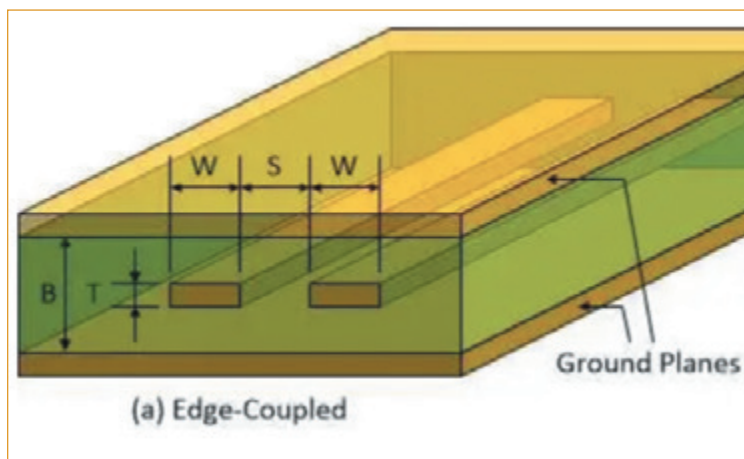


FIGURE 2. The noted dimensions create the space for the digital waveforms to propagate. The stuff between the metal is the medium whose properties determine the rest of the values. (Source: Maxfield EEWeb)

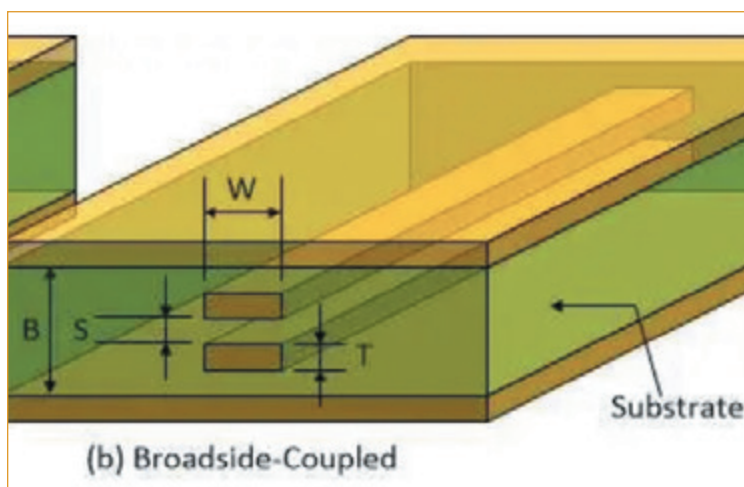


FIGURE 3. Stacking the traces calls for a tight layer-to-layer registration requirement. Missing by 25µm on a 100µm trace throws off the alignment 25%. (Source: Maxfield EEWeb)

Making Technology-Specific DESIGN CHARTS

IPC-2152 is an important baseline for determining current carrying capacity, but further work must be done for individual applications. by MIKE JOUPPI

In response to recent chatter about IPC-2152 in multiple online articles, I believed it necessary to reiterate the purpose behind the IPC design standard for sizing electrical traces.

IPC 1-10b is a task group of volunteers from several companies in the electronics industry. I was task group chairman from 1999 to 2016. We designed test boards and wrote IPC-2152, *Standard for Determining Current-Carrying Capacity in Printed Board Design*. The standard is intended to describe the test data used to define trace heating in a specific configuration through conductor sizing design charts. Testing was performed following IPC-TM-650, method 2.5.4.1A, “Conductor Temperature Rise Due to Current Changes in Conductors.” The design charts are only applicable to that configuration. Designs with different board sizes, thicknesses, and materials, including copper planes – when mounted by bolted fasteners or wedgelocks – have different trace temperatures for an applied current. People and corporations have to create their own charts if they want to have an accurate temperature for a given trace size and applied current. The information included in IPC-2152 provides that information. (Accurate temperatures can only occur from a design chart if that chart represents the specific technology.)

We created an appendix in IPC-2152 to help users understand a single design chart cannot be expected to describe the temperature rise of traces in all printed circuit board applications. Circuit boards vary in size and shape, have different dielectric materials, and vary in the number of layers and copper thicknesses, as well as mounting configurations.

It is not practical to perform current carrying tests to derive design charts that will be useful for all technologies. The intent of IPC-2152 is to provide enough information for companies to run their own testing or develop thermal models to determine conductor current carrying capacity in a given technology. Correlating a thermal model to IPC-2152 baseline data is a start. Correlating a thermal model to a known value validates the model. It is a practice to compare against a standard: in this case, IPC-2152.

The IPC-2152 Appendix includes baseline charts from test

data for 0.5oz, 1oz, 2oz and 3oz copper internal conductors, as well as 2oz and 3oz external conductors. In addition, we included test results for testing in air and in a vacuum environment (space and high-altitude applications).

All this testing was performed with a polyimide test board that was 14" long, 7" wide and 0.07" thick. We tested the board suspended vertically and horizontally in still air for the air/Earth environments and suspended in a vacuum chamber for the space environments. No copper planes were in the board. The appendix includes measured thermal properties for the board materials we tested.

In the appendix, we included thermal modeling results to illustrate the temperature gradients around the traces in the polyimide test board while suspended in still air. The intention was to bring attention to the parallel conductor rule for sizing traces in proximity to each other. This rule is not practical. A better way to estimate the temperature rise for multiple conductors is to manage power and power density, although power and power density are meaningless without design charts that represent the technology.

We created many thermal models of printed circuit boards. The models were correlated to the test data with excellent results. We then used those thermal models to simulate the presence of copper planes. We varied the copper-plane thickness and the distance from the copper plane to the trace. Results showed what we expected: a significant drop in the trace temperature rise when the plane is close to the trace and not as much when the plane is moved away from the trace. We provided guidance regarding board size and the expected reduction in trace temperature when a full copper plane exists at a specific distance from the trace, but it was *not* followed up with any testing.

We wanted to include mounting configurations as well. We wanted to simulate bolted connections and wedgelocks, but we didn't get to that. The mounting configurations will likely show a significant impact.

We collected trace heating data for FR-4 boards that were 14" long, 7" wide and 0.038" thick, as well as 0.059" thick.

TABLE 1. Unpublished Design Charts

Board Length and Width (inches)	Board Thickness (inch)	Board Material	Trace Thickness (inch)	Configuration
3x3	0.038	FR-4	1oz	Baseline
3x3	0.038	FR-4	1oz	1oz plane
3x3	0.038	FR-4	1oz	2oz plane
5x5	0.038	FR-4	1oz	Baseline
5x5	0.038	FR-4	1oz	1oz plane
5x5	0.038	FR-4	1oz	2oz plane
7x7	0.038	FR-4	1oz	Baseline
7x7	0.038	FR-4	1oz	1oz plane
7x7	0.038	FR-4	1oz	2oz plane
10x10	0.038	FR-4	1oz	Baseline
10x10	0.038	FR-4	1oz	1oz plane
10x10	0.038	FR-4	1oz	2oz plane
3x3	0.059	FR-4	1oz	Baseline
3x3	0.059	FR-4	1oz	1oz plane
3x3	0.059	FR-4	1oz	2oz plane
5x5	0.059	FR-4	1oz	Baseline
5x5	0.059	FR-4	1oz	1oz plane
5x5	0.059	FR-4	1oz	2oz plane
7x7	0.059	FR-4	1oz	Baseline
7x7	0.059	FR-4	1oz	1oz plane
7x7	0.059	FR-4	1oz	2oz plane
10x10	0.059	FR-4	1oz	Baseline
10x10	0.059	FR-4	1oz	1oz plane
10x10	0.059	FR-4	1oz	2oz plane
3x3	0.07	Polyimide	1oz	Baseline
3x3	0.07	Polyimide	1oz	1oz plane
3x3	0.07	Polyimide	1oz	2oz plane
5x5	0.07	Polyimide	1oz	Baseline
5x5	0.07	Polyimide	1oz	1oz plane
5x5	0.07	Polyimide	1oz	2oz plane
7x7	0.07	Polyimide	1oz	Baseline
7x7	0.07	Polyimide	1oz	1oz plane
7x7	0.07	Polyimide	1oz	2oz plane
10x10	0.07	Polyimide	1oz	Baseline
10x10	0.07	Polyimide	1oz	1oz plane
10x10	0.07	Polyimide	1oz	2oz plane
3x3	0.07	Bismaleimide Triazine (BT)	1oz	Baseline
3x3	0.07	BT	1oz	1oz plane
3x3	0.07	BT	1oz	2oz plane
5x5	0.07	BT	1oz	Baseline
5x5	0.07	BT	1oz	1oz plane
5x5	0.07	BT	1oz	2oz plane
7x7	0.07	BT	1oz	Baseline
7x7	0.07	BT	1oz	1oz plane
7x7	0.07	BT	1oz	Baseline
10x10	0.07	BT	1oz	Baseline
10x10	0.07	BT	1oz	1oz plane
10x10	0.07	BT	1oz	2oz plane
14x1	0.07	Polyimide	1oz	Baseline
14x1	0.07	Polyimide	1oz	1oz plane
14x1	0.07	Polyimide	1oz	2oz plane

These data were not published. Models were created for these configurations, and charts were created for these boards with no copper planes, a 1oz copper plane 0.005" from the trace, and a 2oz copper plane 0.005" from the trace. We then expanded the data set of charts to include the configurations listed in **TABLE 1**.

The configuration column represents three board configurations. The baseline has no copper planes. The 1oz plane designation represents a chart developed for when a single 1oz copper plane is included in the stackup that is 0.005" from the trace. The 2oz plane configuration is a chart with a 2oz copper plane that is 0.005" from the trace. We ran studies to investigate if the location of the internal trace (through the stack) had any significant impact on the temperature rise; it did not. We ran studies to see the impact of moving the trace to the edge; it did have an impact. We also ran studies varying the distance from the trace to the plane but didn't develop charts from those studies.

Managing Currents and High-Power Densities

To educate users on IPC-2152 and its predecessor IPC-2221, I recently participated in a couple webinars and a HackChat. As a result of those appearances, I received a number of questions about managing currents up to 300A and managing high-power densities. For example, one student was designing a bridge rectifier with four Mosfets that each dissipated 15W of power and had a peak current of up to 80A. The student had questions regarding thermal vias and how to size them. I created a spreadsheet to calculate the thermal resistance through the board and estimate a temperature rise through the board for the power he was managing. I included a way to calculate the power losses in the conductors that were bringing in the 80A of current. In this particular design, the power was managed on the backside of the board. This design required handling 60W of power from the FETs and the conductor losses from the 80A through the board. This would be a challenge. We identified areas for him to concentrate on to improve the design.

When managing high current in any application, I start by looking at the power dissipated (I²R losses or Joule heating) by the conductors in addition to the components. It is easier to account for conductor losses in a thermal model for high current applications than rely on estimated temperature rise from the IPC-2221 or IPC-2152 design charts for two main reasons. The design charts don't take into consideration copper planes or the mounting configuration. These two aspects have a significant impact on the thermal results in a PCB design. In addition, when we created the IPC design charts, our test data went only to 25A. Any calculations above 25A are an extrapolation. Small deviations or extrapolations of a few amps are reasonable, but up to 60A – and as much as 300A – require additional work. The charts are not valid for those applications.

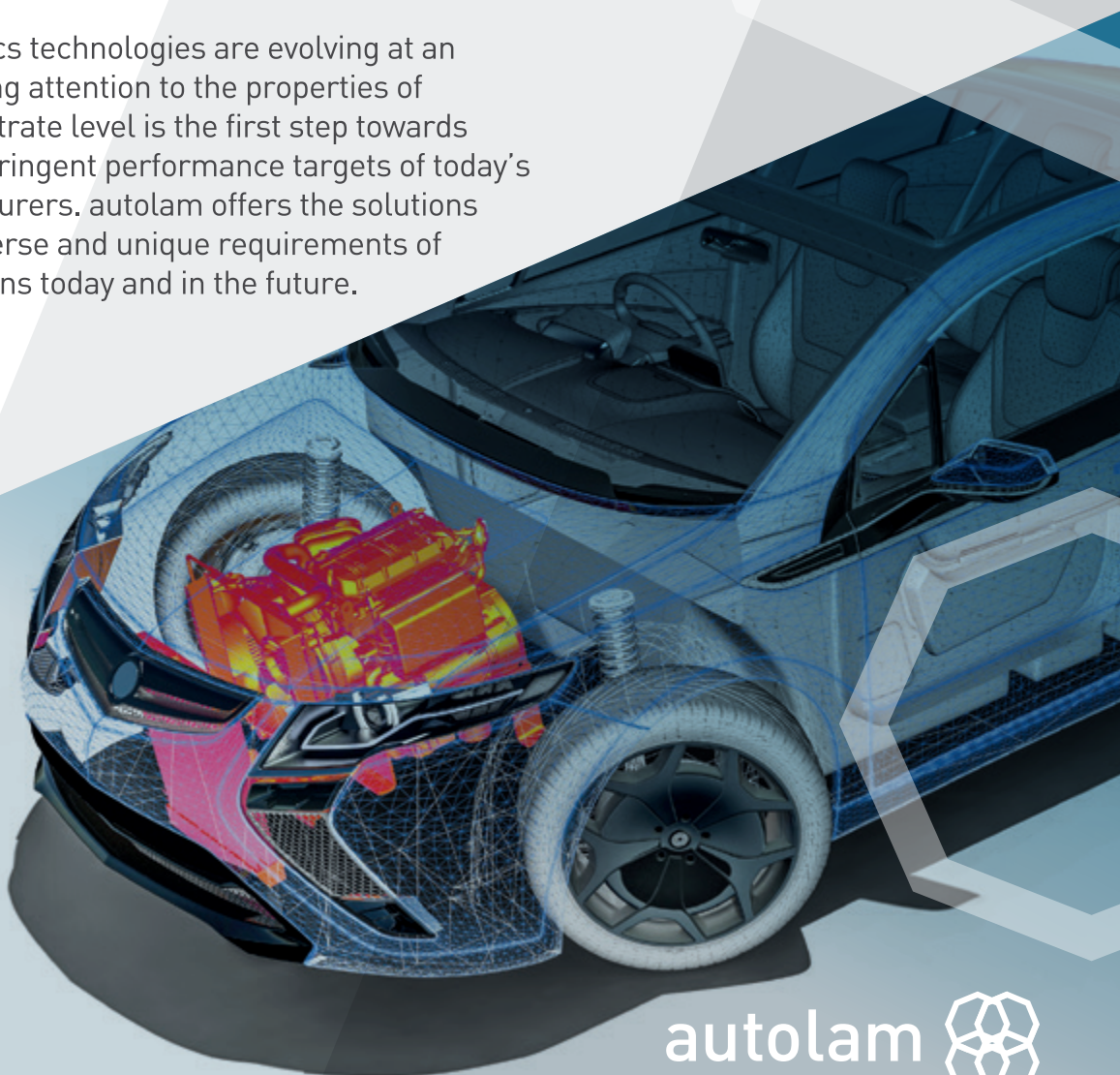


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The History of Conductor Sizing

Until publication of IPC-2152, people were using conductor sizing design charts published in IPC-D-275 and its successor, IPC-2221, *Generic Standard on PCB Design*. Those charts were the source of motivation to create IPC-2152. It took a few years (1998 to 2000) before we understood no one had actually collected and published internal trace heating data before. This was a revelation since there was a design chart for internal conductors (traces) in IPC-2221.

At some point, when multilayer boards were being constructed, a decision was made to create an internal trace heating chart. The internal chart shows up in the MIL-STD-275E standard that preceded IPC-D-275, which eventually became IPC-2221. The internal trace sizing chart was defined by using half the current from the external trace chart, not from test data. The logic behind that choice was never documented.

The IPC-2221 external trace sizing chart originated from work at the National Bureau of Standards from 1954-56.

TABLE 2. NBS Data for External Conductor Sizing

Materials, Processing and Conditions Used to Determine the Temperature Rises of Various Etched Conductor					
Code	Material and Core Thickness (in)	Copper Thickness (in)*	Additional Processing	Test Temp °C	Test Method**
A	5-7 XXXP 1/16	0.0027KK	None	50	IR & TC
B	2-7 XXXP 1/16	0.004K	None	50	IR & TC
C	4-7 XXXP 1/16	0.00135K	None	50	IR
D	4-10 Epoxy 1/16	0.00135K	None	50	IR & TC
E	5-7 XXXP 1/16	0.0027K	None	60	IR & TC
F	2-7 XXXP 1/16	0.0027K	None	60	IR
G	4-7 XXXP 1/16	0.00135KK	None	60	IR
H	5-7 XXXP 1/16	0.0027KK	None	25	IR
I	2-7 XXXP 1/16	0.004K	None	25	IR & TC
J	5-10 Epoxy 1/8	0.0027K	None	25	IR
K	4-7 XXXP 1/16	0.00135KK	None	25	IR
L	5-10 Epoxy 1/32	0.00135K	None	25	IR
M	4-10 Epoxy 1/16	0.00135K	None	25	TC
N	2-7 XXXP 1/16	0.00067K	None	25	IR
O	5-10 Epoxy 1/32	0.00135KK	None	25	IR
P	4-10 Epoxy 1/16	0.00135K	Coated with 0.005" Epoxy Resin	25	IR
Q	2-7 XXXP 1/16	0.00135K	Coated with 0.002" Insulating Varnish	25	IR
R	5-7 XXXP 1/16	0.0027K	Coated with 0.001" Silicone Spray	25	IR
S	4-7 XXXP 1/16	0.00135K	Coated with 0.003" Insulating Varnish	25	IR
T	2-7 XXXP 1/16	0.0027K	Coated with 0.006" Silicone Resin	25	IR
U	2-7 XXXP 1/16	0.00135K	Dip Soldered 10 sec. 250°C	25	IR
V	2-7 XXXP 1/16	0.0027K	Dip Soldered 10 sec. 250°C	25	IR
W	10-7 XXXP 1/16	0.00135K	Dip Soldered 10 sec. 250°C	25	IR
X	5-10 Epoxy 1/8	0.0027K	Dip soldered and Coated with 0.005" Epoxy Resin	25	IR & TC
Y	4-7 XXXP 1/16	0.00135K	Dip Soldered 10 sec. 250°C	25	IR
Z	2-7 XXXP 1/16	0.0027K	Dip Soldered 10 sec. 250°C	25	TC
1	5-7 XXXP	0.00135	Core Removed Conductor in Free Air	25	IR
2	6-16 G-5	0.00135	Core Removed Conductor in Free Air	25	IR
3	2-7 XXXP	0.00135	Core Removed Conductor in Free Air	25	IR
4	5-7 XXXP	0.0027	Core Removed Conductor in Free Air	25	IR
5	2-7 XXXP	0.0027	Core Removed Conductor in Free Air	25	IR
6	2-7 XXXP	0.0027	Core Removed Conductor in Free Air	25	IR
7	4-10 Epoxy	0.00135	Core Removed Conductor in Free Air	25	IR

*K denotes single-clad and KK denotes double-clad material. *IR = IR drop measurement. *TC = Thermocouple measurement

Several reports describe the efforts used to define the electrical characteristics of printed circuits and the dielectrics. Current carrying capacity was documented in NBS Report 4283. The first design chart was for external traces because they had only two-sided boards then (**FIGURE 1**). (Notice the word “Tentative.”)

TABLE 2 describes the datasets that went into creating that chart. The overall dataset results in a mix of variables that impact trace temperature rise include different board materials, different board thicknesses, and different board widths – as well as without copper planes. Board material, board thickness, and the presence of copper planes all have a major impact on the resulting trace temperature rise. A design chart comprised of a mix of variables used to assess the current carrying capacity of an external trace is misleading.

Each line of constant temperature rise in Figure 1 represents a dataset. Each data point in the set represents the amount of current required to raise given size traces to 10°C, or the temperature level for the specific curve (10°C up to 100°C). These data points were graphed by hand on log paper, and a French curve was likely used to define what was considered a best fit.

Table 2 contains a list of all the boards tested to create these design curves. There are four groupings. The group of boards used to create the curve for the final chart is from those labeled “None” in the additional processing column.

Many engineers did principal hand calculations, as well as computer modeling, in an effort to obtain results to match these curves. Not knowing where the data came from made it impossible to obtain a reasonable correlation, especially for the internal conductor sizing charts. (This is why we included as much information as possible in the IPC-2152 Appendix.)

The list of NBS boards includes different dielectric

materials: phenolic (XXXXP), epoxy and G5. The boards varied in thickness: 1/32 (0.0312", 0.793mm), 1/16 (0.0625", 1.588mm), and 1/8 (0.125", 3.175mm). Some boards had copper planes on the backside.

The boards with copper planes are of interest because they show the variance in current level for a given Delta T as a function of the distance from trace to a copper plane.

Either thermocouple or the IR drop method measured the trace temperature rise. The IR drop method is best. They tested

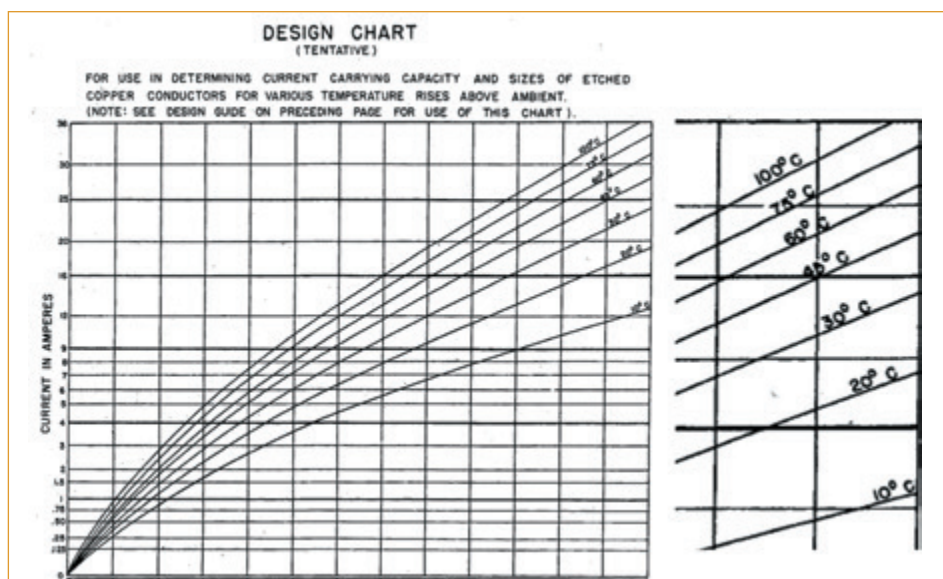


FIGURE 1. Tentative NBS chart.

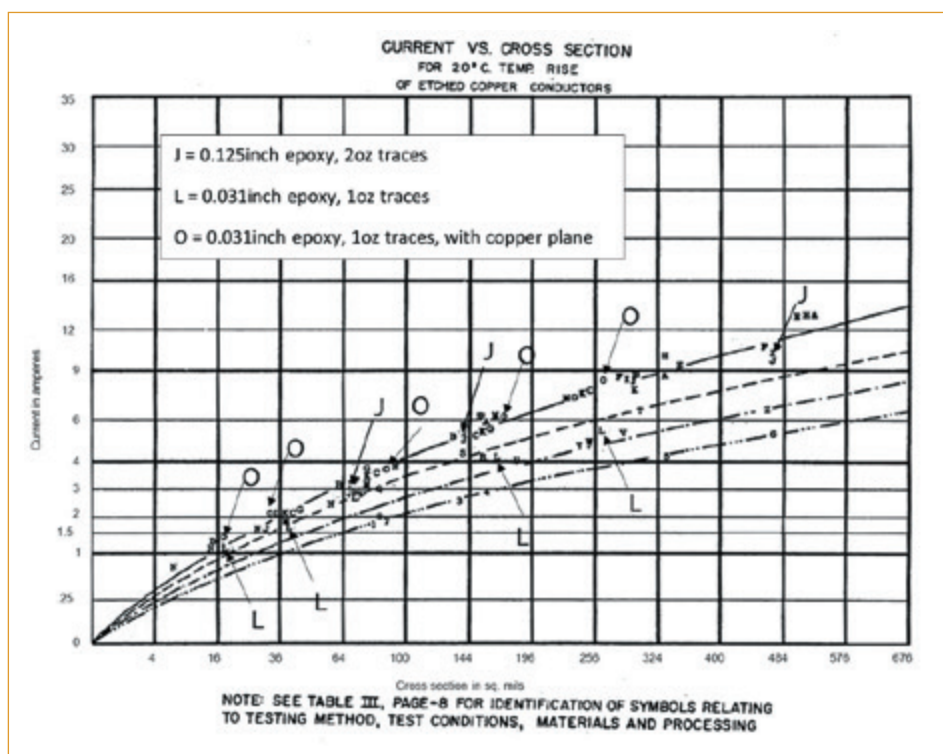


FIGURE 2. 20°C rise curve.

TABLE 3. Design Chart vs. Test Data

Design Chart/Test Board	Maximum Trace Temperature Rise (°C)	Notes
Chart #1 IPC-2221	365	Calculated using the parallel conductor rule.
Chart #2 IPC-2152	68	Calculated using the parallel conductor rule.
Chart #3 TSDC – 0.038" thick FR4, 5" x 5"	98	Calculated using the parallel conductor rule. (Thin boards run hotter than thick boards.)
Chart #4 TSDC – 0.038" thick FR4, 5" x 5", with 1oz copper plane 0.005" from trace	24	Calculated using the parallel conductor rule. (Thin boards with copper planes)
Test Data – 0.06" thick FR4, 5.5" x 8", no copper planes	53	Measured
Test Data – 0.06" thick FR4, 5.5" x 8", 4 copper planes	14	Measured

1oz, 2oz and 3oz copper traces, some with coatings and some stripped completely off the board. The traces stripped from the board are my favorites.

Ironically – or perhaps by design – the traces stripped from the board and tested in air come close to matching the IPC-2221 internal conductor sizing chart. A lot of information in that data aids understanding trace heating and validates the studies performed to develop IPC-2152.

The NBS 20°C rise curve data set is shown in **FIGURE 2**. It shows the variation in current level for a given cross-sectional area and the resulting 20°C temperature rise.

Technology-Specific Design Charts

Accurate design charts, incorporated in an easy-to-use software application, are one step toward a better predesign process for sizing electrical traces. As the industry becomes educated in the fundamentals of heat transfer, it will become obvious design charts that match a technology add more functionality than what we see today.

Many PCB design issues are unsolved. Vias aren't difficult to assess until multiple vias are used to pass current from one layer to another. If the vias do not share current equally, the design is more complex.

Flex circuits are essentially thin boards, some with copper planes and some without. I recommend the old internal trace sizing chart for flex without copper planes. When multiple-layer flex is made and the layers are booked, that becomes a really different problem. I like seeing the conductors sized to minimize the power loss. Calculating total power loss in the flex circuits assesses the thermal design.

Wagon wheels and neckdown areas can also be assessed by using power and power density as a criterion for assessing thermal limitations. Accurate temperature assessments can only happen with charts that represent the technology.

Another great use of technology-specific design charts (TSDC) and design criteria based on power and power density (to estimate trace temperature rise) is managing parallel conductors. Parallel conductors are traces running current at the same time, all closely spaced side by side and in the stackup.

Testing should be performed to understand all the aforementioned items. Parallel conductors are an area we accomplished some testing. The parallel conductor test measured seven 10-mil traces spaced 10 mils apart, all running 1A. Two boards were tested, one with no copper planes and one with four 1oz planes evenly spaced in the stackup. Both boards were 5.5" wide, 8" long and 0.06" thick. The traces were 1oz and were calculated to be 0.001" thick when 10 mils wide. (A resistance measurement is made with low current. Using the resistance and length of the trace, the cross-sectional area can be calculated. We did not get coupons.)

Parallel Conductor Test Results

Let's examine the temperature rise of the seven parallel traces. Seven 10-mil traces are spaced 10 mils apart, 0.001" thick, all running 1A. **TABLE 3** shows the results.

Conclusion

Many conductor issues in the predesign phase, aside from trace temperatures, become apparent after the board is made. Understanding conductor temperature rise for micro technology, as well as managing 300A of continuous current, can be a key element to successful designs. Thermal analysis and testing do a reasonable job of evaluating the end results, but it would minimize respins if we were a little closer in our predesign phase of printed circuit design.

Creating conductor sizing design charts for a given technology provides many insights that clear up old rules of thumb and the fallacy of internal traces running hotter than external traces. Many areas of design could benefit from better conductor design charts. IPC-2152 has all the information needed to make your own technology-specific design charts. ▢

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OSP MYTHS Dispelled

A new specification tackles the application and performance of organic solderability preservatives.

by MICHAEL CARANO

After many years of starts, stops and debate, an industry committee has finally developed a standard for organic solderability preservatives (OSPs). IPC-4555, *Performance Specification for High Temperature Organic Solderability Preservatives (OSP) for Printed Boards*, is out now, and it was a long time coming.

With the electronics industry fully entrenched in lead-free soldering, a standard for OSP is critical. There are more stringent requirements for solder joint reliability, resistance to corrosion, as well as additional requirements related to complex substrate designs.

The development and acceptance of IPC-4555 dispels the myth all OSPs are the same. With circuit boards fabricated around the globe, and small chemical firms attempting to introduce “new OSP processes,” buyers must be aware. Greater solderability requirements – measured as joint strength, paste spreadability and hole fill – and higher temperatures of lead-free soldering have greatly diminished use of conventional (standard substituted benzimidazole-based) OSPs. With the development of third- and fourth-generation organic solderability preservatives based on a novel aryl-phenylimidazole compound, however, OSP has regained its leadership role as a final finish, particularly in Asia and Europe. In addition, the technology shift to bare copper PWBs with selectively plated gold features requires OSPs that do not tarnish or deposit on the gold.

The Genesis of IPC-4555

Input from OEMs, EMS companies, PCB fabricators and chemical suppliers paved the way for the development and acceptance of IPC-4555. Several years ago, an IPC task group attempted to develop a standard governing OSPs. For a multitude of reasons, perhaps lack of understanding, politics, etc., the proposed standard never reached the ballot stage, a requirement for publication. A few years later, a new task group convened to bring an IPC standard for OSP to the industry. **TABLE 1** shows the charter of that group.

The charter shaped the work the IPC-4555 task group

undertook. The group also recognized the following:

- OSP (organic solderability preservative) technology is environmentally friendly, provides a coplanar surface, and requires very low equipment maintenance. The process is designed for horizontal, conveyorized processing. However, vertical immersion systems are easily integrated into the printed wiring board fabrication process.
- Third- and fourth-generation OSP formulations are robust and provide excellent protection against oxidation of the underlying copper through multiple IR reflows under lead-free assembly conditions.
- Various industry studies and OEM interviews as late as 2020 revealed that well over 55% of the circuit board substrates manufactured (by surface area) are produced with OSP technology. OSP is not going away any time soon. And with increased use of QFNs, IC packaging substrates, BGAs, etc., OSP use will continue to find additional applications.

That said, it is prudent to dispel some of the pervasive OSP myths.

OSP Myths and Truths

Myth #1: “An OSP is an OSP. They are all the same.”

This is not only a myth; it is categorically false. The world of lead-free assembly has separated the low-level OSP processes from those formulated and engineered for optimum performance. A simple look at formulations and molecular structures provides further insight into OSP technology. Part of the confusion stems from the name of the organic compound that is the main ingredient in OSP processes: azole. These five letters are attached to various formulations and often appear ideal for solderability preservation to the uninformed. As an example, conventional OSP processes based on long-chain alkylimidazole compounds and substituted benzimidazole compounds functioned adequately to protect the bare copper. These worked well for lead-based assembly, which takes place at lower temperatures. However, higher temperatures of lead-free assembly (including longer dwell times), along with a multitude of lead-free solder pastes, exposed many of these

lower-level azole processes. Ushering a new class of azole molecules based on complex reaction products, known collectively as aryl-phenylimidazole, these compounds are very stable up to 350°C. This formulation provides higher heat stability and can easily withstand the peak temperature of reflow for typical lead-free solders.

Myth #2: “One can always improve solderability of an OSP by increasing the OSP thickness over the copper surface.” Again, this is not true. The critical nature of an OSP is the coating should be as uniform as possible over the copper surface. In addition, excessively thick OSP films make it more difficult for no-clean fluxes and solder pastes to dissolve the OSP coating during the assembly process. When this occurs, the solder paste spread may not complete wet-out over the SMT pad.

The team addressed these issues in IPC-4555. Thickness ranges were not set, as they sometimes are in the metal finish type standards. Instead, it is left to the expertise of the individual OSP suppliers to provide the optimum thickness ranges for solderability performance. Thickness is not critical. Rather, it is the uniformity of the OSP over the base copper and the OSP film’s ability to reduce oxygen penetration to the copper.

Myth #3: “OSP technology does not have sufficient lubricity to function as a coating for press-fit.” This is also a myth. The IPC-4555 task group addressed press-fit with multiple stakeholders from connector and OEM end-users. OSP technology is in widespread use for press-fit applications. The published standard now addresses press-fit as follows:

Press-fit (inserted pin). Press-fit requirements shall meet Telcordia GR-1217-CORE and IEC 60352-5, *Solderless Connections – Part 5: Press-In Connections – General Requirements*. Also refer to IPC-9797 (evaluation guidance document).¹

Additional Information

A major challenge for OSP is providing a printed wiring board finish that will maintain solderability and provide a highly reliable joint with lead-free solders. This is no easy task. A multitude of different lead-free formulations and interactions with fluxes influence reliability. The surface finish must foster the optimum wetting and intermetallic formation under multiple thermal excursions and higher soldering

temperatures required for lead-free solders. How will the surface finish react to these greater temperature and time stresses? What will be the effect on solder paste spread and hole fill after thermal excursion? This is the critical success factor/integrity of the final finish and its ability to preserve solderability. Certainly the end-user often specifies the finish due to personal preference, history, cost, reliability, fit with certain PWB designs, and so on. Regardless, a walk through any EMS company will provide the visitor with the full range of finishes, depending on the various requirements of the customer.

The IPC-4555 task group members submitted statistically significant data to support solderability requirements as out-

lined in the standard. The data further supported that latest generation OSP technology was indeed an excellent finish for complex circuit designs, including BGA substrates, and compatible with many lead-free solder materials and fluxes.

The primary function of OSP is to provide a solderable surface finish capable of providing a coating durability rating of B, per J-STD-003C, *Solderability Tests for Printed Boards*. Coating durability B is “intended for boards likely to experience multiple soldering processes and/or other process steps using SnPb or Pb-free assembly profiles.”² This surface finish is suitable for all sur-

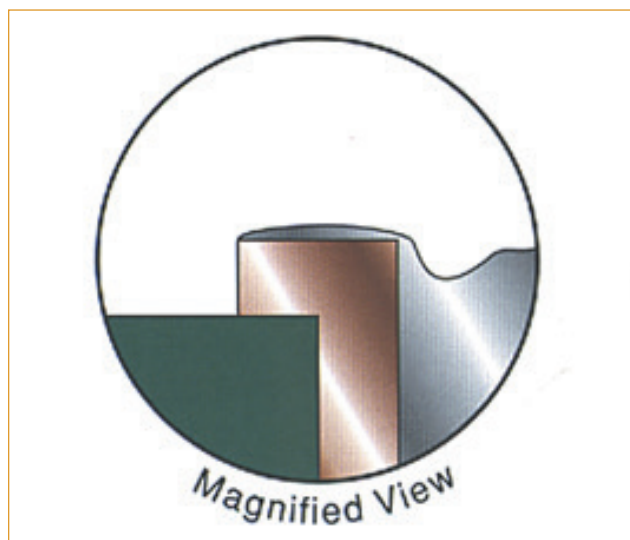


FIGURE 1. PTH solder requirement, per IPC-A-600H.

face-mount, hybrid and through-hole assembly applications. The solderability requirement is for all OSP-plated SMT features tested to wet with solder covering at least 95% of each feature. It is noted, if a static solder float test is utilized, factors including board thickness, feature hole aspect ratio, number of internal copper planes, etc., will have an impact on solderability testing results. For challenging designs, it is recommended to use the assembly soldering method for solderability testing. For through-hole solderability, the solder shall flow up through the via and wet the pad on the top side of the board (**FIGURE 1**).

Review visuals are as shown in IPC-A-600H, *Acceptability of Printed Boards*.

Storage, Handling and Shelf Life of OSP

No discussion – or a standard – would be complete without a full understanding of the storage, handling and shelf life of OSP-coated circuit boards.

The committee understood shelf life of OSP-coated circuits may not be as long as some metallic-finished boards. That said,



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TABLE 1. IPC-4555 Committee Charter¹

Design Chart/Test Board	Notes
Mission Statement	Provide industry standard for the use of OSP (organic solderability preservatives) in the electronics industry
Goals and Objectives	Identify appropriate content and provide input to IPC-4555 OSP specification efforts
	a. Distinguish between multiple formulations and provide uniformity to quality inspection of boards prior to assembly
	b. Define flux compatibility key parameters and data
	c. Define metrology for thickness measurements
	d. Define copper surface finish conditions for use (cleanliness, roughness, etc.)
	Develop metrology to nondestructively measure OSP thickness and uniformity of coating on incoming boards to assembly
	Develop performance measurement criteria for acceptance
Customers/Partners	IPC
Success Indicators	Publish lead-free performance characterization methodology and criteria
	Complete IPC specification documents with identified inputs included or processed
	New non-destructive OSP measurement metrology developed
Feedback Plan	Email to distribution
Scope/Priority	OSP surface finish in a lead-free assembly environment
Chartered Sub-Teams	As needed
Procedures/Meeting Frequency	One-hour meeting every two weeks
	• Minutes including ARs and decisions within 48 hrs (not including weekends)
	• Two-week horizon schedule
Decision-Making Process	Individual agreement to take on tasks
	Consensus approval on WG outputs
Decision Ratifying Body	Review and ratification of specification input content
	Review and ratification of metrology development plans

IPC-4555 lists the shelf life as a “minimum of six months.” Such coatings have been shown in real-time testing by the IPC-4555 task group to demonstrate a shelf life minimum of six months. With proper storage and handling, OSP coatings have been shown to have a 12-month shelf life.

It is recommended to perform either a classic solderability edge dip/solder float test or a solder paste print and reflow on the assembly production line prior to using OSP-coated product that is older than six months.

Storage and Handling of OSP-Processed PWBs

Before OSP-coated PWBs are packaged, the boards shall be free of moisture, particularly for small vias. The dry boards can then be packaged for shipping to the end-user. Operators should handle the dried boards on the edges and protect hands with impermeable gloves. This is necessary to prevent oils and ionic contamination from affecting the PWB performance. An outer slip sheet made of sulfur-free material should be placed on the top and bottom of the stack. Shrink wrap should be applied to seal the package. Sealed packages can be placed in

a box for shipping. Desiccant should be added to the box and the box sealed. End-users should keep boards in the shrink-wrapped package until ready for assembly.

We finally have an industry-recognized and accepted standard for the use of organic solderability preservatives. This should help level the playing field with respect to the reliability and performance of circuit boards fabricated with OSP finishes. IPC-4555 clearly sets the bar high for anyone wishing to supply or implement OSP finish. □

REFERENCES

1. IPC-4555, *Performance Specification for High Temperature Organic Solderability Preservatives (OSP) for Printed Boards*, April 2022.
2. J-STD-003C, *Solderability Tests for Printed Boards*, September 2017.

MICHAEL CARANO is a recognized subject matter expert in printed circuit, semiconductor, surface finishing and medical device industries. His focus is on process control and bring new technologies to market.

A ROYAL Summit

Summit Interconnect's chief executive explains the PCB fabricator's latest buy. by MIKE BUETOW

Summit Interconnect in May announced the acquisition of fellow printed circuit board fabricator Royal Circuit Solutions for an undisclosed sum.

But while the deal at first glance looks like the latest in a long string of capacity buys for the second-largest fabricator in North America, there is more to it than meets the eye.

For its part, Royal has engineering tools and staff that Summit can leverage to speed its own operations.

Royal also includes an electronics assembly operation, Aurora, CO-based Advanced Assembly. The EMS outfit's quickturn production capabilities fit well with Summit's commercial prototype programs. That the fab and assembly sides are integrated adds one more appealing facet to the acquisition.

Summit chief executive Shane Whiteside broke down the latest acquisition in an interview with Mike Buetow.

Mike Buetow: Besides the obvious capacity increase, what made Royal Circuit an attractive buy?

Shane Whiteside: The more we learned about Royal Circuits, the more we saw the benefits of adding its capabilities to Summit's portfolio of PCB services. Not only does Royal Circuits' speed and factory automation align well with our other facilities, but it adds more software expertise and interconnected systems to what we have now. It also has developed offshore support in India, which adds additional speed to its model and provides 24/7 front-end engineering support for operations in Hollister, Santa Ana and Denver.

MB: Are there things Royal is doing that you could adapt for your other facilities?

SW: Royal Circuits' processes were developed from the ground up to fabricate PCBs fast. It's very good at delivering very quickturns. There is definitely an opportunity to take what they've developed and deploy it more broadly across all the Summit sites, particularly to address the needs of the com-

mercial market.

The support from India provides a very broad advantage for non-ITAR products, and is something we're going to be able to scale across our entire company. Of course, we will continue to support ITAR products internally in the US at the site level.

MB: It's interesting because it wasn't just a capacity buy; it was a technology buy as well.

SW: That's correct. The acquisition of Royal Circuits added not just PCB technology in the conventional sense, although there is a lot of that as well. It was really everything I've described, with the software technology, automation, and just the velocity of its operations.

MB: Summit is weighted pretty well toward defense. Where does Royal align with that?

SW: Defense is a large market for Summit, but commercial prototyping is a very large market as well, with the addition of Streamline to our platform in 2018 and Eagle Electronics last year. We have positioned ourselves to serve the US commercial prototyping market, and the addition of Royal Circuit enhances that with additional quickturn capabilities.

At Summit, we want to be one of the leading commercial prototype providers in the United States. In the market research we've done, we've identified the two highest growth markets in North America as aerospace and defense and commercial prototyping, so we've aligned our company to meet the PCB needs of those growth industries.

MB: Summit has some flex capacity and rigid-flex capabilities. How does Royal's compare? Are they doing anything you previously were not?

SW: Royal Circuits has interesting flex and rigid-flex customers, but it doesn't significantly add to Summit's current capac-

ity in that area. We have two factories that already support quite a bit of flex and rigid-flex.

MB: The addition of Advanced Assembly is interesting. What do you plan to do with that operation? You didn't have any assembly in house prior to this, correct?

SW: We previously supported more assembly than you might think using turnkey partners. Advanced Assembly will allow us to continue to work with partners at higher volumes and longer lead times, but also to internalize a lot of the quickturn assembly opportunities. Additionally, Advanced Assembly is a very robust new customer development engine that has contributed to the rapid growth of Royal Circuits. We're looking to take advantage of that internal synergy as well and support some of the new customer work with our broader Summit factory footprint.

MB: So Advanced Assembly made the deal more attractive, not less.

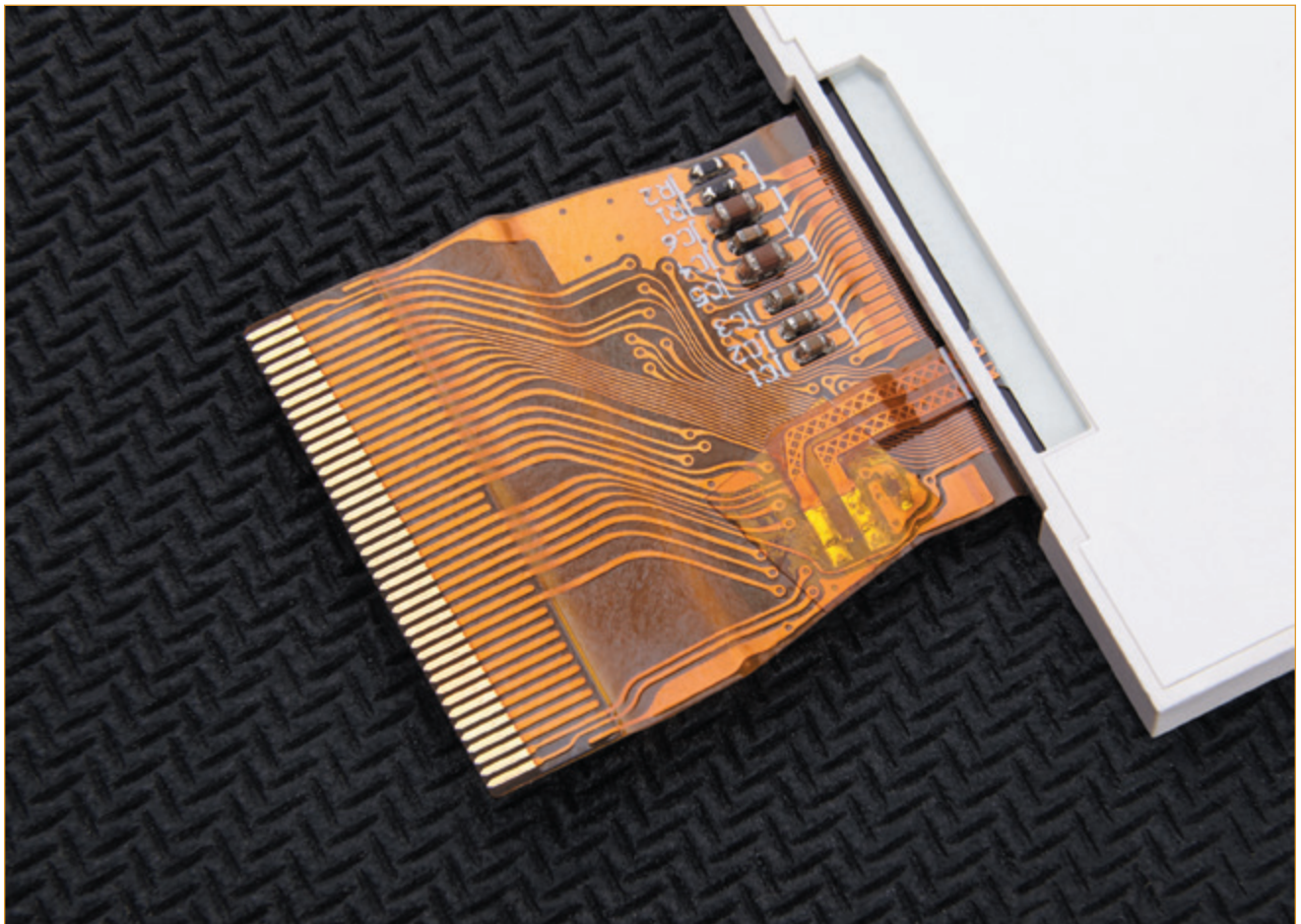
SW: Absolutely.

MB: Should we draw any conclusions insofar as Summit looking at more assembly capacity, or is this a one-off?

SW: In terms of our strategic priorities, this really fits the bill for what we wanted. We have always wanted a higher capacity, more robust assembly capability, and with the location and the facility of Advanced Assembly, I see a lot of opportunities to grow this operation. It has a great team, and we want to see how far we can take it.

MB: Royal's California base adds to Summit's capacity there, which has its pros and cons. What are your thoughts on the geographic balance of Summit's sites?

SW: There's no particular strategy to diversify geographically within North America. It is nice to have shops in the Midwest, and in Toronto in the Eastern time zone. Adding more facilities in California is not Plan A, but California does have a bit of an advantage in commercial prototyping because it's in the last time zone on the continent. Designers can send their data that many hours later, and Fedex picks up later than elsewhere in the country, so it's easier to support prototyping from the Western time zone. But, it isn't like we are pointing to a map on the wall.



The acquisition of Royal Circuits adds flex and rigid-flex capacity and high-end engineering. (Source: stock photo)

Nearshore or Offshore, We've Got the Right Solution

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Change has become a constant in the outsourcing equation. At SigmaTron International, we've developed a business strategy that gives your team the flexibility needed to deal with change. Our engineering team can help you cut product development time, improve manufacturability on the front-end or address cost or obsolescence issues over time. Our global facility network gives you choices which can change as your manufacturing location needs evolve. We can also customize a repair depot solution and support legacy product.

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Advanced Assembly gives Summit new quickturn assembly capabilities.

MB: I would add, if you're looking for an acquisition, and you're not looking greenfield, then you have to go where the plants already are.

SW: Yes, that's right. We're looking to partner with high-quality companies, and like you said, we have to go where they are.

MB: H.R.7677, The American Printed Circuit Boards Act of 2022, has just been introduced in the US House, and one of the provisions is a 25% text credit for domestically purchased circuit boards. If the bill gets passed, that has to be seen as very advantageous to the folks onshore.

SW: I think it would certainly be favorable, and it will be interesting to see who actually banks that credit: Is it the OEM or the EMS company? I'm just wondering aloud on that, but I think it would certainly have a stimulative effect toward favoring US PCB manufacturers.

Any sort of stimulus is interesting to me. It's one thing to try to get some Title III funding or a piece of the CHIPS Act to help modernize factories building printed circuit boards. That's great, but boards in the US are still going to be made in a high-cost region, unless we put some sort of boundaries on the market, which I think this bill attempts to do. We must shape the market somehow to make the free-market economy work and put more business in the United States. I wouldn't want to spend taxpayer money if we can't shape the market to push the equilibrium toward domestic manufacturing.

MB: Do you think the current events, specifically what's going on in Russia and reports that they are running out

of semiconductors for producing more tanks, is having any influence on the US government right now insofar as its attention to the domestic supply chain?

SW: I think so. In last year's US Partnership for Assured Electronics [USPAE] meeting, people from [the US Department of Defense] were pretty clear that for the past 15 years they have been under-concerned about the resilience and robustness of the supply chain that supports the DoD, including printed circuit boards, but other areas of microelectronics as well.

I think they now understand that a lot of our asymmetrical military advantage in the US – and our future advantage – has been enabled by our superiority in electronics. Moving forward, electronics is going to be a more significant part of our national defense, and we have to salvage some of these industries that have atrophied. I'm excited to see that the government is concerned on multiple fronts, but it needs to be done the right way. The [Printed Circuit Board Association of America] has made a tremendous impact in a year-and-a-half of existence, and we've gotten a lot of attention. IPC government relations have aligned with a lot of what the PCBAA is doing, and having everyone working in the same direction is making a lot of difference. □

MIKE BUETOW is president of PCEA (pcea.net); mike@pcea.net.

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An Industry 4.0 Approach to Employing 3-D AOI on an SMT Line

Correlating inspection trending with test data to fine-tune accept/reject parameters.

INDUSTRY 4.0 AUTOMATED inspection technology opens the door to enhanced levels of process control. In addition to having to upgrade equipment, however, fully leveraging the power of this technology requires a strong team, an accurate program validation database, and a methodology to track trends in continuous improvement activities. Here is a look at an implementation process for inline 3-D solder paste inspection and 3-D automated optical inspection following reflow on SigmaTron's SMT lines in Tijuana.

A planned phase two of this implementation includes adding 3-D AOI to secondary assembly operations post-SMT, plus correlating AOI trending with final test data to fine-tune AOI acceptance/rejection parameters. The facility is currently averaging 50ppm defect rates across its SMT lines. The goal of this greater inspection process is to drop that to zero defects; although, given material constraints are driving a defective component rate that represents a third of that 50ppm level on some programs, zero ppms may be unachievable until material availability returns to normal.

The inspection stations communicate with the screen printer and adjust paste deposition based on defects identified, creating a closed-loop system. They also track trends data, enabling the team to pare-to top-five defects, and where indicated, implement continuous improvement initiatives beyond process adjustments. The systems communicate to a database accessible via remote computers available to technical personnel. Trending analysis has already driven changes to stencil maintenance frequency and greater focus on monitoring pick-and-place machine placement variation. From a Lean perspective, the machine-to-machine communication aspect reduces process variability and represents a better use of resources by eliminating the need for human intervention within set parameters. Using the data to determine optimum maintenance activity frequency eliminates defects that would otherwise occur as stencils or tooling gradually slips out of acceptable parameters.

Setting up the systems, a team with a Six Sigma Black Belt and two mechatronic technicians performed gage R&R studies for repeatability and reproducibility using the Automotive Industry Action Group's acceptability definition, where:

- Ideal = a tolerance or study variance percentage of 10% or less, with a contribution percentage of 1% or less
- Acceptable = a tolerance or study variance percentage of 10 to 20% or less, with a contribution percentage of 1-4%

- Marginal = a tolerance or study variance percentage of 20 to 30% or less, with a contribution percentage of 5 to 9%
- Poor = a tolerance or study variance percentage of 30% or greater, with a contribution percentage of 10% or greater

CP and Cpk ratios were also calculated to measure the process capability against the voice of the customer (standards/requirements). In this analysis:

- Very good = Infinity, $CP(Cpk) > 1.67$
- Good = $1.33 < CP(Cpk) < 1.67$
- Need to manage = $1.00 < CP(Cpk) < 1.33$
- Need to improve = $0.67 < CP(Cpk) < 1.00$
- Poor management state = $CP(Cpk) < 0.67$

The studies and calculations showed the specification limits for all 3-D AOI were in acceptable GR&R condition and very good CP/Cpk condition. The program validation is used for machine verification every six months. Once control limits were established, programming parameters were adjusted for each printed circuit board assembly to assess acceptability based on IPC-A-610 and customer documentation requirements.

Following implementation, the team is focusing on two improvement tracks. The first deals with improving first-pass yields on product identified through weekly trends tracking. In one example, trends data led to the discovery a fixture had warped and was no longer seating correctly, which caused flex cable terminations to shift off pads. The fixture was replaced, correcting the issue.

The second improvement track is focused on improving the overall inspection process. One area being analyzed is the accuracy of operator decisions to override AOI decisions. Customers are evaluating a more efficient labeling strategy to provide full traceability. Test data have been transformed from raw, delimited data to formatted columns. Now remote computers are running a dashboard that visually conveys real-time SPC/Cpk and first-pass yield data, and allows remote debugging.

This Industry 4.0 approach is creating a system that autocorrects solder-deposition-related issues in real time and provides the trends data to enable the team to monitor tooling, equipment accuracy and customer design issues that may be causing defect opportunities. The comparison of AOI trending with test data is increasing AOI programming accuracy, and better understanding of equipment operational trends is helping fine-tune maintenance and calibration intervals. □

FILEMON SAGRERO

is continuous improvement engineer and a Six Sigma Black Belt at SigmaTron International's facility in Tijuana, Mexico; filemon.sagrero@sigmatronintl.com.



Swindlers' Lists

Engineers know a snow job when they hear it.

DEAR MR. CHRIST,

Knowing you're a busy man, we'll cut to the chase: Our firm is offering you an exclusive list of the five million attendees to your recent motivational speech on the mountain. Our proprietary Digitaldisciple algorithms identify those most receptive to your message, broken down by district in Judea, so you can focus on the finer points of conversion, based on leaders and laggards, attendance-wise. We've done the work, so you don't have to, for a very – dare we say it – revelatory price. Others promise salvation in the form of prescreened customer lists, but only we deliver. Accept no substitutes! Click the link at the bottom of this email, and a customer service representative will contact you soon about how we can make the Beatitudes work for you!

You know those lists? Of course you do.

They're the ones whose salespersons relentlessly appeal to our inner greed, breathlessly promising delivery to the recipient of a complete roster of attendees to one's favorite trade show. Or equipment users' group. Or industry association annual meeting. All guaranteed.

The unspoken and alluring premise is a name on a list is simply a customer you have yet to contact. Who doesn't want a new customer? Better yet, a complete list of vetted customers? These services furnish the list. All you have to do is follow up.

Their pitch probably lands in your inbox or spam folder regularly. For many, that means weekly. For a "privileged" cohort, daily. Usually deleted upon arrival. Too good to be true.

Is it?

Ever wonder how they work? I tried an experiment.

Beginning Feb. 7, 2022, and ending Jun. 10, 2022, I saved every email appeal for list services. In those 88 business days (no holidays included), 206 unsolicited pitches arrived in my inbox. That's 2.34 per working day, a sample size sufficiently large to assess the range and depth of what is being offered.

So, what is being offered?

Not much range and very little depth.

Like this:

Hi,

I am following up to confirm you are interested in acquiring the Visitors/Registrants List.

Space Tech Expo

May 23-25, 2022

*Long Beach Convention & Entertainment Center,
Long Beach, USA*

Registrant Counts: 4,280

Each record of the list contains: Contact Name, Email Address, Company Name, URL/Website, Phone No, Title/Designation

Seems tempting. But wait, there's more:

I am following up to confirm if you are interested in acquiring the Visitors/Attendees List.

Space Tech Expo

May 23-25, 2022

Long Beach, California, USA

Registrant Counts: 10,000

Different ads on different days but almost the same script. Different company (allegedly), same speech-writer. Probably the output of one server in someone's bedroom in a remote corner of Sumatra.

Bigger registration count. One highlighted a battalion, the other a regiment. This is a business model with a decidedly dim view of human nature. Bigger numbers mean bigger appeal. Don't forget that greed thing.

These are inflationary times, after all.

One of those 10,000 might hold the key to my retirement. (Then again, so would the lottery.) Except I have many other competing pitches for Space Tech, with projected quantities of attendees ranging all over the map: 2,000; 3,842; 11,000; 13,445; and 20,099. (Why didn't they just round that last number up to 20,100? Does 20,099 somehow look more authentic?) The regiment has grown to a brigade, even a full division. Which to choose?

Another Space Tech cold email badgered me 26 times in a one-month span, gradually reducing its price as I remained nonresponsive, from a starting \$800 to an ending \$400. Endure an extra month of digital harassment, and, by projection, it should fall to the quite-affordable rate of zero.

Another sample from the inbox:

Dear Exhibitor,

I am following up to confirm if you are interested in acquiring the Attendee List.

Houston Expo & Tech Forum

Mar. 24, 2022

Stafford Centre, Stafford, USA

Counts: 2,560

Each Record of the Attendee Includes: Client Name, Business Name, Title, Email Address, Phone

ROBERT BOGUSKI is president of Datest Corp. (datest.com); rboguski@datest.com. His column runs bimonthly.



Number, Web Address, etc.

Let me know your thoughts, so I can send discount cost and additional information.

And this:

Hope you are doing well!

We are following up to see if you would be interested in the Attendee list of:

Houston Expo & Tech Forum

Date: Mar. 24, 2022

Stafford Centre, Stafford, USA

Are you interested in acquiring the Attendees' info? (19,300+ Attendees)

Attendees' information fields: Company Name, Company URL, Contact Names, Title, Phone Number, Email Address

Let me know your thoughts, so I can send the cost and additional information.

We have a Special 50% Discount offer for this month.

We are looking forward to hearing from you!

Six identical pitches, each requesting my thoughts (thank you very much), received on the same day, two each from three different companies. Supposedly. All of them equally wrong in their attendance projections. The 2022 SMTA Houston Expo and Tech Forum, held on one day, Mar. 24, had attendance considerably south of 19,300, a small city. Actual attendance resembled a small neighborhood.

Then there's this:

Thank you for showing interest in our listings, and below are the details for list acquisition:

Project Details:

Show Name: Automotive Testing Expo Europe 2022

Total Counts: 20,000+ opt-in contacts

Discounted Price: €1,300

- *Data Fields: Contact Name, Title, Phone Number, Fax Number, Physical address, State/City, Company Name, Company URL, and verified email addresses*
- *90%+ accuracy and deliverability on all data fields*
- *Data will be provided in an Excel spreadsheet for unlimited list usage*
- *All the contacts are permission-based and authorized to receive the third-party information.*

Let me know if you need more details, and I await your response. Thank you!

It's reassuring the process is permission-based (what's the alternative, coercion-based?) and that it's 90% accurate (relative to what?). Pity the 10%, banished to Inaccuracy Purgatory.

Samples sampled randomly, and thus enticed, time to bite. So, I took the plunge and replied to a handful. The response was like blood sprinkled on a shark-strewn sea. Except some sharks are more discriminating than others.

For example, this is the five-figure approach:

- *Target List of prospects based on your specifications (zip*

codes, counties, etc.)

- *A fully managed multi-touch, multichannel lead management program*
- *Dedicated Sales Development Representative who will be making the calls*
- *Client Success Manager who will be your point of contact*
- *Quality Assurance Analyst to qualify every lead submitted meets your criteria*
- *Script, email templates, social and website marketing setup, which you will pre-approve prior to the start of the program*
- *Access to our web-based lead management platform, where you can monitor and organize, in real time, all the leads that have been qualified for you*

I'm sure this is what Jeff Bezos and Elon Musk use every day before breakfast, once the rich zip codes are fully saturated with sales. A bit beyond my pay grade and budget, but nice to know this service is available once I make my first billion.

Back on Earth, here is the more prosaic, poor person's approach:

It's a half-price sale!

We are offering a 50% discount.

You can now acquire the info at \$400.

Maybe they offer a payment plan.

Or there's the middle-of-the road, semi-tailor-made approach, filling space with words, revealing little:

What we do for each client is customized, so it really depends on exactly what your objectives are. However, based on what your website says, I think we would probably look at our automated outbound systems to very targeted prospects that would be a good fit for your business, using our process of rapid sales communication testing, combined with your experience, to identify the best messages to communicate to your buyers. Ultimately our objective is to set up a steady flow of new high-quality sales meetings for you each month.

Let me know if that resonates with you, and we could look at trying to find a time for a quick chat.

Automated outbound systems?

Soundwaves generally resonate with me. Businesspeople have conversations. They don't "chat."

Here's the thing: AI-inspired attendee databases are a mass-marketing approach that is unsuitable for small engineering businesses like ours. Our sales pitch is too technical. It can't be faked. Engineers know a snow job when they hear it. Test parameters, specifications and detailed requirements like power-on testing, JTAG, 4-wire tests and 1149.1/1149.6 rules don't lend themselves to a spreadsheet with 20,099 potential contacts. There may not have been that many JTAG users in the whole of human history. Nor does an x-ray inspection requirement stipulating resolution, focal length, scan energy, field of view, area of interest and desired pixel/voxel size find clear expression in a shotgun approach to marketing. At our

level, one needs to listen to the customer. After listening and digesting the need, you either provide the service or you don't. This includes supporting nontechnical customers who crave honest guidance on prudent use of their test dollars. A superficial, cold-calling approach to sales risks being more off-putting than enticing. Reputational risk is real. Our clients tend to have specific problems in need of very specific solutions. Test and inspection parameters, and their results, get scrutinized; often they're second-guessed once the data are known. A high degree of customer contact and handholding is essential. One can't afford to be dismissive or reluctant to explain (often repeatedly). Antagonize such prospects for any reason, and you'll never hear from them again.

Thank you, database and list folks, for your time, attention (a lot of that, once interest is shown) and education. Not now, but maybe in the future, as your systems get smarter,



Do all those spam emails offering huge contact lists that don't exist come from the same group?

better defined and more focused. Obviously some small single-digit percentage of your cold calls succeeds; otherwise, I wouldn't get 206 inquiries in 88 days. It's just that you and my company aren't a match. Yet.

Until then, the imagination still wanders and wonders:

Senator McCarthy, your recent speech in Wheeling, West Virginia, would have had a more accurate list of communists in government had you taken advantage of our Commienet services. Why be satisfied with only 205 names? For one low fee, our patented statistical analysis would have given you a list of 5,280 embedded subversives in the State Department and elsewhere in Washington. Consider the advantages of one-stop shopping and make technology your patriotic ally.

Mr. Haldeman, our Paranoiacom custom database will significantly expand your enemies list, virtually and literally, overnight. Why limit your outreach to The Washington Post and certain precincts in Manhattan? Data, like grudges, can be driven anywhere, and all the world's fair game. Fortunately, for your sake, there's us. Our firm provides the numbers – every name a prospective enemy – you can simmer over.

For us, refined application of the technology would appear to be in its infancy. Of such developments is progress made, knowing full well that infants' adherence to a script is, well, unpredictable.

And the folks who offer the declining balance? (See above.) This morning they renewed acquaintances with yet another discount offer: 28 days left for no fee. □

ROI, continued from pg. 18

introduced to manufacturing, the product is the best way for customers and suppliers, working together, to accomplish a cost-effective design. Too often this communication is wrongly assumed to occur. As much as frequent two-way communication should be happening when all is moving along with traditional technologies, it is critical the communication takes place when a new approach is contemplated that may be enabling for one but not necessarily for others.

The difference as to whether a technology is enabling or disruptive is determined only by the degree in which customer and supplier decide to work together. As our industry finds ways to tweak older, reliable technologies or develop paradigm-changing ones, understanding the enabling benefits and the disruptive nature will make the journey mutually rewarding. □

Board Buying, continued from pg. 19

ally sound, the cause most likely is moisture-related. A bake-out process before any additional assembly can remove most of the moisture, if not all of it. This permits the board to be assembled without issue.

IPC-1602, *Standard for Printed Board Handling and Storage*, provides suggestions for proper handling, packaging and storage of PCBs. It puts the full responsibility for PCB moisture content on the supplier, even after the finished product has left the manufacturing facility.

The way PCB suppliers package their products indicates their commitment to quality and reliability. It is the final step in the manufacturing process, and PCB buyers have a responsibility to ensure it is done right. □

AVERATEK ACL, CBF MATERIALS FOR A-SAP

Aluminum clad laminate and catalyzed buildup film use Toyo catalyzed aluminum foil that provides well-controlled surface texture and uniformly coated palladium metal. Developed for outer and buildup layers, ACL and CBF enhance use of HDI PCB and package substrate manufacturing technology A-SAP. Fill technical gap between mSAP HDI PCB and package substrates. A-SAP can be used for materials with thin electroless base copper layer. Liquid metal ink forms palladium catalyst, which permits less than 10nm of uniform metal coating.

Averatek

averatekcorp.com

CADENCE ONCLOUD SAAS SOFTWARE

OnCloud SaaS software provides toolsets for PCB design, multiphysics system analysis and computational fluid dynamics; direct and secure access to Cadence software and cloud data storage, without installation and licensing; and online support resources, including thousands of training courses and rapid adoption kits.

Cadence Design Systems

cadence.com

HIROSE KW30 CONNECTOR

KW30 1mm-pitch wire-to-board connector comes in two to eight positions. Miniature single-row connector offers reliability via a two-point contact design, combined with crimp contact deflection



prevention. Rib design provides secure fit when mating plug and receptacle. Center lock prevents incomplete mating, mis-insertion and lock damage. Is offered in straight or right-angle interface types; 28, 30 or 32AWG; and gold plating. Is for home appliances/white goods, medical devices, office equipment, industrial robots, FA controllers and servo motors. Has current rating up to 3.0A, voltage rating of 100V AC/DC and operating temp.

range of -55° to +105°C.

Hirose

hirose.com

NI TESTSCALE FUNCTIONAL TESTER

TestScale modules can be combined in custom configurations to meet coverage needs and slot into small industrial chassis that connects to host PC using USB. TestScale Chassis can be rack-mounted or mounted within fixture. Hardware connects to NI and third-party software such as TestStand, LabVIEW and Python using NI-DAQmx driver. Optimizes coverage with flex modular design and daisy-chain chassis. Reportedly reduces footprint up to 50%. Speeds fixture design with standard 37-pin connectors and production-optimized form factor.

National Instruments

ni.com

ROGERS R03003G2 LAMINATES

R03003G2 laminates now include a 9µm electrodeposited HVLP foil option. Are for antenna outer layers for millimeter wave (mWave) radar PCBs, for example. Can reduce copper reduction steps needed to meet final PCB copper thickness requirements after filled via formation. Unbalanced cladding options permit thicker copper to remain on ground layer.

Rogers Corp.

rogerscorp.com

UCAMCO UCAMX STENCIL SEAT

UcamX Stencil seat includes all standard UcamX functionalities, supplemented with StencilToolbox. StencilToolbox reportedly offers streamlined workflow; recognition of pad shapes; support for stencil specific shapes. Is independent from incoming data quality. Features instant overview on critical apertures; reshaping pads for optimal paste cohesion; nanocoating support; technical drawing.

Ucamco

ucamco.com

VISHAY EP2 TANTALUM CAPACITOR

EP2 tantalum capacitor comes with radial through-hole terminations with stud-mount option in B and C case codes. Reportedly is a drop-in replacement for competing parts or as higher capacitance alternative in mechanically equivalent

package. Features high capacitance from 2,700µF to 48,000µF in B case code and 3,600µF to 72,000µF in C case code. Voltage ratings range from 25VDC to 125VDC. Capacitance is 9,000µF at 80V and 58,000µF at 35V in C case size. Features standard capacitance tolerance of ±20%, with ±10% tolerance available. Optimized for pulse power and energy holdup applications in laser guidance, radar and avionics systems. All-tantalum, hermetically sealed case. Features high vibration (high frequency: 20g; random: 19.64g) and mechanical shock (50g) capabilities. Operates over temp. range of -55° to +85° to +125°C with voltage derating, and provides max. ESR down to 0.017Ω at 1kHz and +25°C. Is available with tin/lead and is RoHS-compliant.

Vishay Intertechnology

Vishay.com

ABB HIGH SPEED ALIGNMENT SOFTWARE

High Speed Alignment software reportedly can increase speed of six-axis robots 70% and improve accuracy 50%. PC-based software includes visual servoing technology using one or more cameras, combined with computer vision system, to control position of robot relative to workpiece. As robot moves, cameras capture images continuously; computer vision system takes information and cross-checks and adjusts robotic movements, delivering 0.01 to 0.02mm precision. Minimal programming experience is required. Is compatible with range of cameras, IRC5 and OmniCore robot controllers, and IRB 1100 and IRB 120 industrial robots.

ABB Robotics

new.abb.com/products/robotics



BOWMAN A SERIES MICRO XRF

A Series Micro XRF measures smallest features on semiconductors and micro-electronics. Accommodates large PCB panels and wafers of any size for full sample coverage and multi-point programma-

ble automation. Poly-capillary optics focus x-ray beam to 7.5µm FWHM. 140x magnification camera measures features on that scale; secondary low-magnification camera provides live-viewing of samples and bird's-eye macro-view imaging. Dual-camera system lets operators see entire part, click image to zoom, and identify feature of interest. Programmable x-y stage with movement of 23.6" (600mm) in each direction can handle large samples; precision down to $\pm 1\mu\text{m}$ for each axis; used to select and measure multiple points. Pattern recognition software and auto-focus features also do this automatically. 3-D mapping capability can be used to view topography of ENIG, ENEPIG, EPIG and other processes. Has molybdenum anode tube (chromium and tungsten also available) and high-res, large-window silicon drift detector that processes more than two million counts per sec.

Bowman

bowmanxrf.com

DELO-DOT PN5 JET VALVE

Delo-Dot PN5 microdispensing valve has dispensing frequency up to 300Hz. Plunger speed reportedly reaches twice the max. value of Delo-Dot PN3. Pneumatic jet valve features tool-free maintenance fluid system. Offers contactless application, preventing collisions between dispensing valve and component. High-viscous materials and difficult media can be dispensed. Offers interchangeable nozzles with different diameters, as well as adjustable plunger stroke. Reproducible using different drop sizes in nanoliter range. Plunger is made of ceramic and carbide. Suitable for prolonged use. When plunger wears out, nozzle and fluid plunger need replacing. Actuator has lifetime of more than one billion cycles. Measures 68mm x 28mm x 99.5mm. Cartridge retainer can be positioned in 90° increments; permits media to be fed from all four sides of device.

Delo

delo-adhesives.com

INDIUM NC-809 FLUX

NC-809 halogen-free, ultra-low residue, flip-chip flux is designed to hold die or solder spheres in place without risk of die shift during assembly. Reportedly leaves minimal residue after reflow and exhibits superior wetting performance. Is qualified for ball grid array ball for packages sensi-



tive to traditional water-cleaning processes. Offers high tackiness to eliminate die tilting or shifting during reflow; consistent flux deposition and wetting; compatibility with variety of underfills; reduced warpage of package and lower thermal stress.

Indium Corp.

indium.com



INSPECTIS HD-025-B UV LED RING LIGHT

Flicker-free HD-025-B UV LED ring light has homogeneous illumination at 365nm wavelength range. Powered via AUX output of Inspectis digital microscope or via optional power supply (HD-024-S) for compatibility with other devices. Mounts securely onto digital camera and includes UV protective glasses. Features integrated ON-OFF switch and brightness control.

Inspectis

inspect-is.com

SAKI 3DI AOI

3Di inline AOI system is for inspection of high-density printed circuit boards and boards with combinations of small



and tall components. Is equipped with new camera that reduces cycle and produces ultra-sharp high-res 3-D images; can simultaneously inspect extremely

small parts (008004 and 0201) and tall parts. Features camera resolution of 8µm, height measurement 25mm, and imaging speed of 4,500mm²/s.

Saki Corp.

sakicorp.com/en/

STACKPOLE TCR FOR CSSK0612 RESISTORS

TCR for CSSK0612 four terminal current sense shunt resistors has been improved down to 100ppm for resistance range from 0.5mΩ to 5mΩ. Are for power monitoring, management and control for a range of end-products.

Stackpole Electronics

seielect.com

INSITUWARE SM-100 SMART MIXER

SM-100 smart mixer provides solder paste mixing with real-time quality control and materials traceability. Automatically mixes solder paste jars to fit-for-use state. Monitors temperature, mixing time and fitness. Can mix solder paste directly from cold storage to bring to room temperature. Provides red, yellow and green light indicators of paste quality with reusable lid that attaches to solder paste jar. Reportedly eliminates hand mixing, reduces mix time and ensures repeatability. Mixing cycle provides SPC and documentation. Provides insight on paste quality before printing. Measurements correlate to J-STD-005 and IPC-TM-650.

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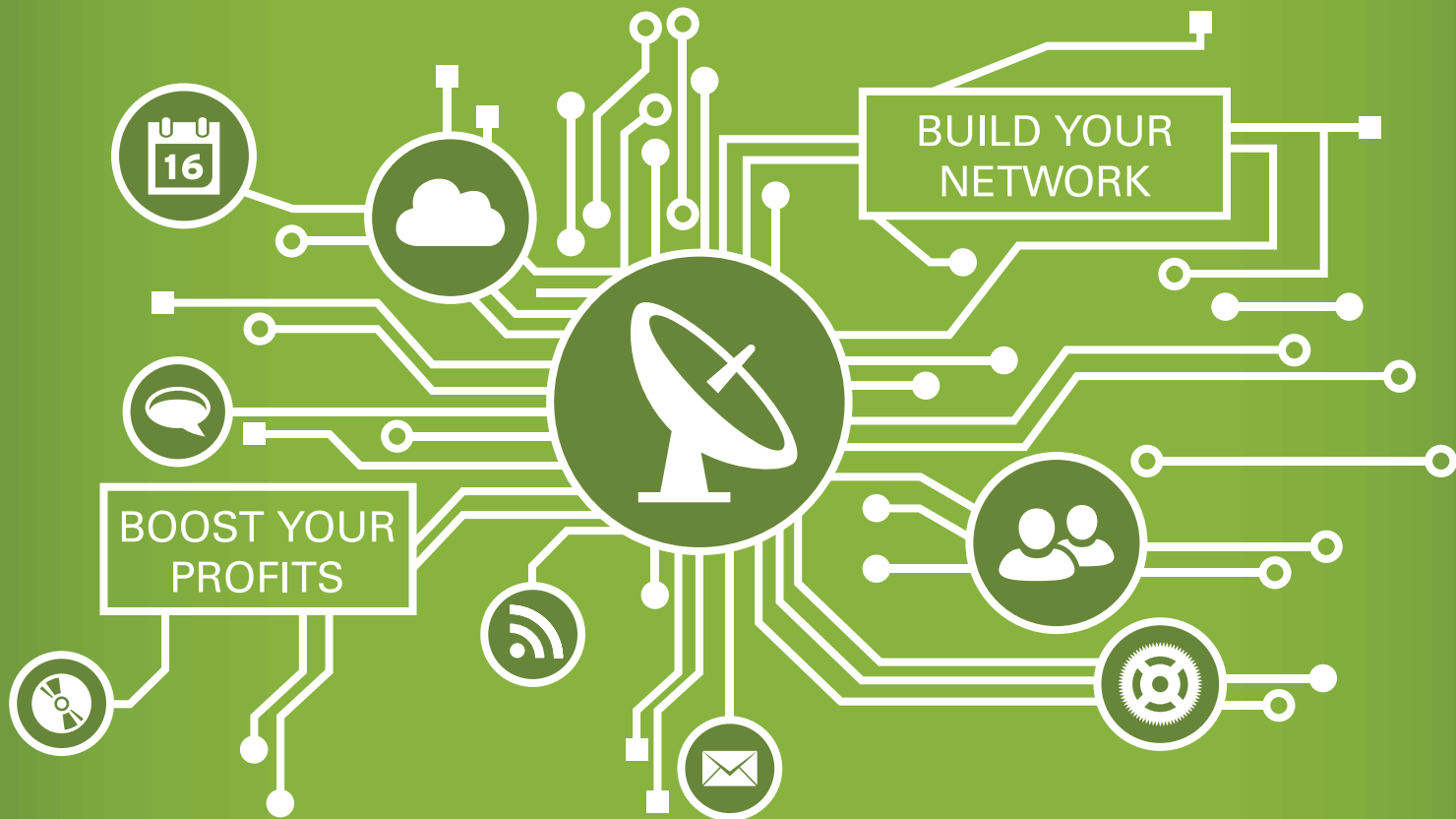
INSITUWARE CC-100 THICKNESS TESTER

CC-100 thickness tester provides nondestructive and contactless conformal coating thickness measurements. Measures dry thickness of conformal coatings to verify against IPC-A-610. Measures wet thickness of conformal coatings to provide insight for process adjustments. No ground plane required. No measurements of uncoated boards required. Multi-coating support: acrylic, polyurethane, silicone, epoxy and UV. Less than 5 sec. measurement time. Reportedly eliminates need for coating test coupons. Local and cloud data storage for traceability and process control.

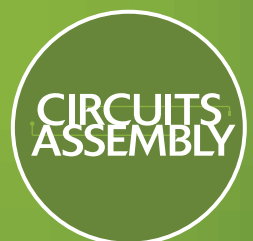
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In Case You Missed It

Flexible Wireless Electronics

“Room-Temperature High-Precision Printing of Flexible Wireless Electronics Based on MXene Inks”

Authors: Yuzhou Shao, *et al.*

Abstract: Wireless technologies-supported printed flexible electronics are crucial for the Internet of Things, human-machine interaction, and wearable and biomedical applications. However, the challenges to existing printing approaches remain, such as low printing precision, difficulty in conformal printing, complex ink formulations and processes. Here the authors present a room-temperature direct printing strategy for flexible wireless electronics, where distinct high-performance functional modules (e.g., antennas, micro-supercapacitors and sensors) can be fabricated with high resolution and further integrated on various flat/curved substrates. The additive-free titanium carbide ($\text{Ti}_3\text{C}_2\text{T}_x$) MXene aqueous inks are regulated with large single-layer ratio (>90%) and narrow flake size distribution, offering metallic conductivity ($\sim 6,900 \text{ Scm}^{-1}$) in the ultrafine-printed tracks ($3 \mu\text{m}$ line gap and 0.43% spatial uniformity) without annealing. In particular, the authors built an all-MXene-printed integrated system capable of wireless communication, energy harvesting and smart sensing. This work opens a door for high-precision additive manufacturing of printed wireless electronics at room temperature. (*Nature Communications*, Jun. 9, 2022, <https://www.nature.com/articles/s41467-022-30648-2>)

Sensors

“Neuro-inspired Electronic Skin for Robots”

Authors: Fengyuan Lei, *et al.*

Abstract: Touch is a complex sensing modality owing to a large number of receptors (mechano, thermal, pain) nonuniformly embedded in the soft skin all over the body. These receptors can gather and encode the large tactile data, allowing humans to feel and perceive the real world. This efficient somatosensation far outperforms the touch-sensing capability of most of the state-of-the-art robots today and suggests the need for neural-like hardware for electronic skin (e-skin). This could be attained through either innovative schemes for developing distributed electronics or repurposing the neuromorphic circuits developed for other sensory modalities such as vision and audio. This review highlights the hardware implementations of various computational building blocks for e-skin and the ways they can be integrated to potentially realize human skin-like or peripheral nervous system-like functionalities. The neural-like sensing and data

processing are discussed, along with various algorithms and hardware architectures. The integration of ultrathin neuromorphic chips for local computation and the printed electronics on soft substrates used for the development of e-skin over large areas are expected to advance robotic interaction, as well as open new avenues for research in medical instrumentation, wearables, electronics and neuroprosthetics. (*Science Robotics*, Jun. 8, 2022, vol. 7, no. 67, <https://www.science.org/doi/10.1126/scirobotics.abl7344>)

Soldering

“Effect of Remelting Heat Treatment on the Microstructure and Mechanical Properties of SnBi Solder Under High-Speed Self-Propagation Reaction”

Authors: Yang Wan, Longzao Zhou and Fengshun Wu

Abstract: The heat source based on the self-propagation reaction of Al/Ni thin foil has the characteristics of concentrated heat, fast temperature rise/fall rate and small heat-affected zone. It can complete the melting and solidification crystallization of solder within milliseconds to realize solder interconnection, which can solve the problems of damage to heat-sensitive materials and components caused by monolithic heating of package structure. However, due to the highly nonstationary interconnection process, the resulting microstructure morphology may affect the service performance of the interconnected joints. In view of this, to investigate the post-solder microstructure of solder based on the self-propagation reaction, this paper analyzes the effect of the initial microstructure on the post-solder microstructure by heating 300- μm -thick SnBi solder with a 40- μm Al/Ni thin foil. The results indicated the short melting time could result in the incomplete melting of heterogeneous phases and the nonuniform distribution of elements during the melting process, which had a significant effect on the morphology and composition distribution of the solidified microstructure, as well as the hardness distribution of the melted zone. The above conclusions have the potential to improve the interconnection process based on the self-propagation reaction, which is critical for both theoretical guidance and engineering application. (*Scientific Reports*, Jun. 9, 2022, <https://www.nature.com/articles/s41598-022-13776-z>)

This column provides abstracts from recent industry conferences and company white papers. Our goal is to provide an added opportunity for readers to keep abreast of technology and business trends.

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