### **Weiner: Covid Creations**



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### FIRST PERSON

6 THE ROUTE

Right on Target. Mike Buetow

### MONEY MATTERS

#### 18 ROI

When you want to write a check, but can't. Peter Bigelow

#### 20 BOARD BUYING

Extra size, extra costs. Greg Papandrew

22 FOCUS ON BUSINESS

Exit strategies. Susan Mucha

### 24 WHAT'S OLD IS NEW

Covid innovations. Gene Weiner

### TECH TALK

25 DESIGNER'S NOTEBOOK Beyond PCB constraints. John Burkhert, Jr.

### 28 MATERIAL GAINS

Lined up for onshoring. Alun Morgan

### 29 FLEXPERTS

The flex stackup. Nick Koop

#### 62 TECHNOLOGY FLASHES

Updates in silicon and electronics technology. Binghamton University

#### 70 TECHNICAL ABSTRACTS

### DEPARTMENTS

8 AROUND THE WORLD

### 16 MARKET WATCH

67 OFF THE SHELF

### PRINTED CIRCUIT DESIGN & FAB CIRCUITS ASSEMBLY

### **FEATURES**

#### 32 SIMULATION

#### **Reflections from Discontinuities**

Reflections, even from a single discontinuity, can destroy a signal, but the effect of the major discontinuities can be predicted with validated models before the board is designed. by YURIY SHLEPNEV, PH.D.

#### 38 SIGNAL INTEGRITY

### How to Calculate Trace Length from Time Delay Value for High-Speed Signals

Managing propagation delay and relative time delay

mismatches is a challenge. We need to know how to calculate trace length from time delay value to implement the PCB trace routing accordingly. by LANCE WANG

#### 44 SUPPLY CHAIN

#### Will US Government Incentives Spur Domestic Investment?

Fresh off its inaugural meeting, the PCBAA gets legislative good news. What's next for the organization that wants to rebuild US production? Travis Kelly, president and chief executive of Isola and chairman of the PCBAA, explains. by MIKE BUETOW

#### 48 PROCUREMENT

#### The Production Sourcing Approach

Working with a contract manufacturer can be daunting, particularly if it lacks experience sourcing challenging parts in a challenging market. by BRIAN LANEY

#### 50 IC CLEANING *cover story*

#### **Defluxing of Copper Pillar Bumped Flip-Chips**

A case study showed a well-balanced aqueous cleaning agent removed lead-free, water-soluble tack flux residues better than straight deionized water. by RAVI PARTHASARATHY and UMUT TOSUN

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### ON PCB CHAT (pcbchat.com)

SOLDERING AND SMT with DR. RON LASKY

#### US PRINTED CIRCUIT BOARD LEGISLATION with TRAVIS KELLY

#### SMTA SMT CERTIFICATION

with DR. RON LASKY and JIM HALL





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### THE ROUTE



MIKE BUETOW PRESIDENT

### 'At the Edge' of a Data Revolution

AVE BIG BOX stores learned lessons that can be applied by electronics manufacturers?

One of the big takeaways from the Future Compute conference on the campus of MIT in May was a definitive "yes!"

There, we heard about how some of the large retail chains like Target use software, hardware and data in all kinds of customer experiences.

Almost every employee has handheld devices tracking the billions of sensors and cameras in use across some 1,900 stores and 50 regional distribution centers. At each store, it runs about 100 different software applications. They look at traffic trends: When is the peak? When is the lag? And how can they be modulated?

Now consider an electronics manufacturing operation. There could be hundreds of operators, thousands of PCBs, millions of components, billions of solder joints, each one needing traceability.

When making its purchases, Target sources from end-products all the way back to raw materials. It sources some of the cotton used in Target brand clothing directly from farms. In this era of instant outrage, every public relations debacle is just a leak and a tweet away. Say a farm used a verboten pesticide. Target might also need to know what was close to that source: nearby waterways, for example.

Likewise, PCB fabricators and assemblers buy everything from standalone process equipment to raw tin and copper. In our industry, we are looking into hard-to-reach places like the Democratic Republic of Congo, for instance, to trace the origin of certain metals and minerals.

And like Target, we use all sorts of software and systems to do so. A distributed ledger like blockchain could be a perfect tool for managing these transactions. It allows companies to track parts quickly and monitor traceability at a granular level.

The trick is to turn all that data into something useful, of course, and the cost simply to track and house all that data can overwhelm many companies. It goes a long way toward understanding why most supply chain decisions are reactive.

Where Target stumbles is how to manage its multiple cloud environments with local-level computing applications. The cloud is seen as too slow for responding to situations on the ground. Meanwhile, local networks have low latency, but lack the capacity to perform the immense analytical computations needed to adjust to changes in real time.

Edge computing, which loosely describes everything in-between, helps the processing of data gathered at local nodes. But, for now, it is seen as expensive, especially relative to the local sites, requiring a GPU at every store. Even a \$100 billion entity like Target says it can't afford it.

That's where industrial manufacturing has an advantage. While we process millions or billions of pieces of data per day, we do so across much fewer production sites. Target has 2,000 sites to gear up, but even the largest of the Tier 1 EMS companies generally have fewer than 100 factories, and the NTI-100 PCB fabricators even less. They are in a better position to leverage edge solutions and – potentially – evolve into predictive supply chain management.

Another eye-opener at Tech Compute was the notion put forth that, for the greatest efficiency and implementation, artificial intelligence must be commoditized.

To do so, top-level companies need to coordinate a solution for others to follow. We see this to a degree in our industry, where Cadence, Zuken and others have been leading the effort to develop a comprehensive approach to capturing design intent and sending that downstream to fabrication, assembly and test, an effort known as IPC-2581. At PCB West (pcbwest. com) this year, they will join companies such as Koh Young, which will talk about leveraging the IPC-CFX standard (for Connected Factory Exchange) that establishes requirements for sharing information among the manufacturing processes and software systems used in PCB assembly.

As the amount of information that can be captured and shared grows, it begs for a holistic approach. What we see, however, is companies focused on the data often lose sight of the strategy. They are defining the solution – and customer – before they've defined the strategy.

This is where Target shines. The firm has spent two years of the pandemic under consumer siege. Today it's a run on hand sanitizer. Tomorrow it's toilet paper. It has to treat almost every day like "Black Friday." Its use of blockchain to trade beef with supermarkets, for example, could be adopted by electronics manufacturers for component exchanges.

From traceability to data processing solutions, best practices might just come from outside our manufacturing environment. Don't discount them. It may be the low-cost retail chain that has the answer to industrial manufacturing's problems.



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### **PCDF** People

**Anaya Vardya** of American Standard Circuits and **Doug Dixon** of 360Biz have joined the Printed Circuit Engineering Association (PCEA) board of directors.

Boston Materials named **Rafael Padilla** sales director – electronic solutions.



Casco Automotive promoted **Russ Steiner** to global ECAD manager. He joined the company in 2018, and has been in printed circuit design and engineering since 1979.

Google named **Jonah Stephenson** staff electronic packaging engineer. He spent the previous seven years at Facebook, and has more than 23 years' experience in design engineering.

Insulectro named **Joe Harbour** director of operations, East and Midwest regions.

Meta named Oscar Miguelino PCB design engineer.

Paul Trio is now director of the SEMI International Standards program.

### **PCDF Briefs**

Altix announced a significant order for direct imaging and contact printer equipment to be installed at a new plant in Jiangxi province.

Atotech and Schweitzer Engineering Laboratories will partner at SEL's manufacturing facility under construction in Idaho.

Daikin America and LiloTree became members of the High Density Packaging (HDP) User Group.

**DuPont Microcircuit and Component Materials** is collaborating with **Industrial Technology Research Institute** of Taiwan to demonstrate the value of DuPont Green-Tape LTCC material used in antenna-inpackage applications.

**DuPont Interconnect Solutions** completed its \$250 million expansion of Kapton polyimide film and Pyralux flexible circuit material production in Circleville, OH.

**DuPont** joined **Apple's** Supplier Clean Energy Program.

Siemens Digital Industries and Nistec signed an agreement for distribution in Israel of Siemens' PCBflow simulation tools.

Ucamco said the biggest PCB maker in Thailand has purchased two of its Calibr8tor photoplotters.

### Summit Acquires Royal Circuit and Affiliates

**ANAHEIM, CA** – Summit Interconnect announced the acquisition of printed circuit board fabricator Royal Circuit Solutions and its assembly affiliate Advanced Assembly for an undisclosed sum.

The deal includes Royal Circuit's operations in Hollister and Santa Ana, California, and the Advanced Assembly EMS site in Aurora, Colorado.

The acquisition expands Summit's PCB offering in rigid, flex, rigid/flex and ATE PCBs, significantly strengthens engineering and service resources providing CAM, DFM/A, PCB design/layout, and also adds quick-turn, prototype SMT assembly services.

The move solidifies Summit's position as the largest privately owned PCB manufacturer in North America, based on PCD&F estimates, with a footprint that will now encompass eight manufacturing facilities. PCD&F estimates the acquisition brings Summit's revenues to at least \$200 million a year.

The deal also significantly broadens the scope of Summit's product offering, while expanding the company's business portfolio of key customers and end-markets.

Summit, which ranks only behind TTM Technologies among PCB fabricators in terms of US-based revenues, now has facilities in California, Illinois, Colorado and Toronto, Canada.

### TTM Technologies to Acquire Telephonics for \$330M

**SANTA ANA, CA** – TTM Technologies has agreed to acquire Telephonics in a debt-free cash transaction for \$330 million, subject to customary working capital adjustments at closing.

Telephonics provides intelligence, surveillance and communications solutions deployed across land, sea and air applications. The transaction is expected to broaden TTM's Aerospace and Defense product offerings.

The transaction is subject to customary closing conditions, including regulatory approvals. It is expected to close in the second quarter of 2022.

"We expect the complementary portfolio and skills will enhance TTM's strategic capabilities and growth opportunities, enabling us to deliver significant benefits to our Aerospace and Defense customers," said Tom Edman, CEO, TTM. "We expect the transaction to be immediately accretive to our non-GAAP EPS."

TTM's A&D is expected to be approximately 40% of total company revenues, or approximately \$1 billion. The acquisition would more than double the company's A&D design and development engineering talent, with the addition of systems engineering expertise in RF/microwave-based integrated systems.

TTM has identified approximately \$12 million in pretax, run-rate cost synergies expected to be realized by the end of 2024. The firm expects to finance the purchase with cash on hand.

At the end of 2021, TTM had \$538 million in cash on the balance sheet.

### Simmtech Subsidiary Opens Manufacturing Plant in Malaysia

**BATU KAWAN, MALAYSIA** – Simmtech Holdings, through its Malaysia-based subsidiary, Sustio, in May officially opened its new manufacturing facility here, according to reports.

It's the company's first advanced manufacturing facility based in Penang, says Southeast Asia managing director Jeffery Chun.

"It is also our eighth factory, along with other operations in Korea, China and Japan. In May last year, Sustio broke ground on an 18-acre site at BKIP, investing

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8 4 7 - 9 1 3 - 0 1 6 2 WWW.FUJIAMERICA.COM **Ucamco** also established a subsidiary in North America: **Ucamco NV**.

**US Circuit** has acquired the accounts of PCB fabricator **Rocky Mountain Circuits**, which will shut down production.

### **CA** People

Benchmark named **Beth Kufahl** director, materials, and Benchmark Space Systems named **Bharat Patel** avionics engineer.

Bestronics hired **Alison Shyu** as program manager.

Creation Technologies named **Steve Heinzen** strategic account leader.

Emerald EMS appointed **Lucian Soaita** chief operating officer.

Essemtec named **Quintin Armstrong** North American service manager.

**Irene Sterian**, director, technology and innovation development at Celestica and founder of REMAP, passed away on May 8.



Ethan Mueller, Kyzen's regional manager – Midwest, received a 2022 40 Under 40 Award from *Products Finishing Magazine.* Mueller manages sales and customer support functions in

the Midwest US.



Libra Industries appointed Sam Reed (left) director of operations for its Cleveland EMS location and Luis Montiel chief financial officer.



MicroCare appointed Marufur Rahim technical director to oversee the company's laboratory, research and development and quality teams. He has over 20 years' experience

in technical direction and management, having held director and manager roles at Chemence, Dymax and Selena, among others.

Neways appointed Loi leng (Fiona) Lam chief financial officer.

Viscom named **Christian Schweizer** head of central service.

### **CA Briefs**

**BayaTronics** purchased a complete **Juki** line for its new facility in Concord, NC.

**BTU International** expanded its distribution relationship with **Stratus Vision** to include Pyramax reflow ovens in Germany, Austria and Switzerland. more than RM600 million. Despite the lockdown caused by the Covid-19 situation, the practical construction work took only nine months to complete, and the factory is now fully equipped and ready to run mass production. This new factory has already employed more than 700 workforces, and it will reach its full employment of more than 1,000 employees by next year. This new factory will also deliver the first Made in Malaysia semiconductor memory chip packaging substrate and printed circuit board, bolstering Malaysia's semiconductor supply chain even further."

The factory is expected to increase Simmtech's total capacity of substrates and PCBs 20%, according to Chun.

### Icape Acquires German PCB Supplier SAFA2000

**MUNICH** – Icape Group in April acquired German PCB supplier SAFA2000 for an undisclosed sum. SAFA2000 had 2021 revenue of €15.5 million (US\$16.8 million), with 28 employees and 360 active customers.

"Icape Group is well established in Germany," said Cyril Calvignac, CEO, Icape. "Our business unit recently moved to brand-new offices. We deployed more logistics solutions in Nuremberg. We invested in the acquisition of BA Elektroniks in 2021, and we are now moving forward with the acquisition of SAFA2000, which brings another experienced structure to our organization, with very interesting tools, new customers, an expansion of our suppliers' list, and advanced logistics services with a fully operational warehouse to manage our activities in this dynamic country that represents our biggest market share in Europe."

The German company will be integrated into Icape Deutschland in 2023.

### Icape Prepares IPO, Aims for Revenue of €500M by 2026

**FONTENAY-AUX-ROSES, FRANCE** – Icape Group is preparing an initial public offering on the small-cap market of the Euronext exchange. The planned IPO is subject to regulatory approval of the company prospectus, admission to the exchange, and favorable market conditions.

The printed circuit board fabricator and assembler had revenue of €169 million (US\$182.4 million) in 2021, up 34%. The company aims for revenue of €500 million by 2026.

The company is currently owned by its founder, managers and employees.

Icape consists of 27 subsidiaries. The company believes its global organization is structured and sized to absorb a new phase of significant growth.

### Cicor Completes Acquisition of SMT Elektronik

**DRESDEN GERMANY** – Cicor Group completed its acquisition of SMT Elektronik, according to reports. No financial terms of the agreement were disclosed.

The transaction will be financed by existing credit facilities and funds from a mandatory convertible bond issued in January.

SMT Elektronik is integrating approximately 130 employees here, expanding its electronic manufacturing services business in Germany. The merged firms will operate as Cicor Deutschland, effective immediately.

SMT Elektronik's customer base is related to Cicor's target markets of medical and industrial technology. The company generated sales of some €20 million in 2021.

As part of the deal, Cicor also acquired SMT's data logger business, including Monilog products.

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**CalcuQuote** launched a beta version of StockCQ, a peer-to-peer platform for OEM and EMS companies to directly trade inventory with each other.

**Electronic Manufacturing Services Group** purchased a **Hentec/RPS** Vector 460 selective soldering system.

**Escatec** partnered with electronics design house **Byte Lab**.

**Europlacer** named **SmartRep** distributor in Germany.

**Foxconn** said its goal is to achieve net zero greenhouse gas emissions by 2050. The EMS/ODM aims to reduce carbon emissions 21% by 2025, 42% by 2030, and 63% by 2035.

Holo Industries has signed with Partner-Tech Europe to co-develop products, and sell and support Holographic Touch technology in Europe, Africa and Latin America.

Koh Young Technology celebrated its 20-year anniversary in May.

Kulicke and Soffa received two purchase orders, from two separate customers, for its Luminex advanced display system.

**OK International** appointed **Bench Top Solutions** manufacturers' sales representatives for **Metcal** in New Jersey, Southern New York, Long Island, and Eastern Pennsylvania.

**Quality Circuit Assembly** has received \$2.2 million in new orders from its EV customers.

**Rehm Thermal Systems** is training three staff members as "energy scouts" in Baden-Wurttemberg, Germany.

Scanfil is partnering with the EcoVadis responsible procurement program and enhancing its collaboration with suppliers.

Schweitzer Engineering Laboratories added two Universal Instruments FuzionXC platforms in its Lewiston, ID, facility.

**Technical Support** installed a **Europlacer** Atom A1 pick-and-place machine.

**TestEquity** has become an official authorized distributor of **Kurtz Ersa** products.

Texas Instruments awarded Kulicke & Soffa its 2021 Supplier Excellence Award.

XDry appointed TechSystems manufacturers' representative and entered into an exclusive distribution agreement with Bentec to sell XDry humidity-controlled storage cabinets in Europe.

Yxlon International is rebranding as Comet Yxlon.

### Cnergenz Seeks to Raise RM58M from IPO in Malaysia

**BURSA**, **MALAYSIA** – Cnergenz expects to raise RM58 million (US\$13 million) from a planned initial public offering in May, according to reports. The Penang-based electronics manufacturer said the IPO involves the public issue of 100 million shares and an offer for sale of 50 million offer shares by way of private placement.

From the public issue, 25 million shares will be made available for application by the public, while 10 million shares will be designated for application by directors and employees. The remaining shares will be reserved for investors.

The proceeds will be allocated for the firm's operations facility, in addition to R&D development and working capital.

### SEC OKs Registration Statement on Tempo, ACE Acquisition

**SAN FRANCISCO** – Tempo Automation and ACE Convergence Acquisition said the registration statement in connection with their previously announced proposed business combination has been declared effective by the US Securities and Exchange Commission.

The deal is estimated at an equity value of \$919 million post-transaction. The transaction could include cash of more than \$500 million.

ACE will hold a general meeting May 5 during which shareholders will be asked to consider and vote on proposals to approve the merger and related matters.

The deal is expected to close shortly after the meeting, subject to shareholder approvals and the satisfaction or waiver of the conditions in the agreement and plan of merger and other customary closing conditions.

Upon closing, the company will be renamed Tempo Automation Holdings.

### Henkel Opens Technical Application Center in Silicon Valley

**SANTA CLARA, CA** – Henkel opened an application center here designed to support product development for the materials company's electronics customers in the Silicon Valley. The \$2 million investment includes dispensing robots, 3-D printers, mechanical property evaluation equipment, coating and jetting systems and failure analysis capabilities, among other assets.

In addition to the hands-on laboratory, the facility provides multiple secure collaboration spaces for Henkel technical staff and customers, as well as digital platforms for virtual engagement opportunities.

"The current pace of technology progress is unprecedented," said Stefan de Diego, regional head of electronics, Americas and Europe, Henkel. "And, for today's innovators, being first to market is integral to commercial success. With our knowledgeable team and extensive lab resources – located in the global epicenter of tech innovation – Henkel can provide even more immediate and impactful prototype design and analysis support for our customers, helping them meet critical time-tomarket windows with tested, proven devices."

Henkel's application center offers a co-development environment, with access to resources required for technology design and testing.

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Trends in the US electronics equipment market (shipments only)	JAN.	% CH. FEB.	ANGE Mar.	YTD%	
Computers and electronics products	1.9	1.3	-0.3	5.6	
Computers	2.5	3.7	-2.9	-3.1	
Storage devices	6.8	2.4	-0.1	8.5	
Other peripheral equipment	-3.7	8.7	6.8	6.4	
Nondefense communications equipment	8.0	1.0	-3.1	10.8	
Defense communications equipment	6.0	-2.0	-4.1	8.6	
A/V equipment	34.5	-8.7	-1.0	48.7	
Components <sup>1</sup>	2.8	2.7	0.7	14.5	
Nondefense search and navigation equipment	1.0	-1.2	-2.0	1.3	
Defense search and navigation equipment	0.8	1.1	-2.0	0.8	
Medical, measurement and control	-0.3	0.7	-0.1	2.7	
<sup>(</sup> Revised. *Preliminary. <sup>1</sup> Includes semiconductors. Seasonally adjusted. Source: U.S. Department of Commerce Census Bureau, May 3, 2022					

US MANUFACTURING INDICES					
	DEC.	JAN.	FEB.	MAR.	APR.
PMI	58.8	57.6	58.6	57.1	55.4
New orders	61.0	57.9	61.7	53.8	53.5
Production	59.4	57.8	58.5	54.5	53.6
Inventories	54.6	53.2	53.6	55.5	51.6
Customer inventories	31.7	33.0	31.8	34.1	37.1
Backlogs	62.8	56.4	65.0	60.0	56.0

Source: Institute for Supply Management, May 1, 2022

KEY COMPONENTS						
	NOV.	DEC.	JAN.	FEB.	MAR.	
EMS (North America) <sup>1</sup>	1.43	1.55	1.58	1.52	1.44	
Semiconductors <sup>2</sup>	24.5%	28.3%	26.8%	<b>26.2%</b> r	<b>23</b> % <sup>p</sup>	
PCBs <sup>3</sup> (North America)	1.10	1.17	1.18	1.16	1.05	
Computers/electronic products <sup>4</sup>	5.34	5.32	5.24	5.17 <sup>r</sup>	5.23 <sup>p</sup>	
Sources: 1PC 2SIA (3-month moving average growth) 3PC 4Census Bureau Poreliminary (revised						

### Hot Takes

- DRAM revenue is expected to grow to \$118 billion, up 25% in 2022. NAND flash memory will reach \$83 billion, up 24%. Both would be records. (Yole Développement)
- 2021 was a record year for the semiconductor industry and OSAT revenues, but the outlook for 2022 is less certain. (TechSearch International)
- Overall electronic component sales sentiment for April beat expectations by more than 13 points, as the index measurement grew from 113.6 to 119.6. (ECIA)
- Nine in 10 electronics manufacturers surveyed are currently experiencing rising material costs, while nearly four-fifths are experiencing rising labor costs. (IPC)
- Research and development spending by semiconductor companies worldwide is forecast to grow 9% in 2022 to \$80.5 billion after climbing by an above average 13% in 2021 to a record-high \$71.4 billion. (IC Insights)
- In 2021, the top 50 semiconductor suppliers, not including the pure-play foundries, represented 89% of the total \$614.6 billion worldwide semiconductor market, up eight points from the 81% share the top 50 companies held in 2010. (IC Insights)
- Global semiconductor revenue is projected to total \$676 billion in 2022, an increase of 13.6% from 2021. (Gartner)
- The electronic component sales sentiment index for April grew from 113.6 to 119.6. Survey participants expect growth in May but softened expectations to 111.5, a drop of 8.1 points and the lowest level since November 2021. (ECIA)
- Notebook brand vendors are mulling raising their prices to reflect rising logistics and other costs in the second half of 2022, according to industry sources. (DigiTimes)

### Report: Most Electronics Supply Chain Lead Times to Increase into 2023

**PASADENA, CA** – Continuing electronics supply chain challenges at the beginning of this quarter suggest there will only be pockets of relief through the remainder of 2022 and into 2023 for many commodities, according to new data from Supplyframe.

Through the first quarter of 2023, more than 70% of lead times are forecast to increase, the market watcher said in May. During that time frame, analog, complex semiconductor (ASICs, MCUs, MPUs and PLDs), flash memory, non-ceramic capacitor, resistor and standard logic devices are forecast to rise in price with very limited exceptions. Most of the same devices will also remain at or exceed already elevated lead times.

Commodity supply tightness and cost inflation are impact-

ing most inputs across categories. This includes shortages of resin feedstocks and additives, increasing costs for fuels and metals, and challenges related to the affordability and availability of labor and freight capacity.

One category that remains particularly stubborn and hostile is the active components market. From analog power to standard logic to ASICs and sensors, this space will be swimming in a sea of red indicators for the next four quarters. This is happening as strong demand continues, production is at capacity, lead times are extended, and rising prices plague most devices.

Passive components are not as constrained as active ones. However, like active components, passive commodities also suffer from raw material challenges and labor shortages.



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### All Stretched Out

Shipping, Covid-19 and inflation challenges rival supply chain issues when securing capital equipment.

WHEN I MADE my 2022 capital investment plan, I never thought it would be my 2023 capital investment plan. However, with a couple minor exceptions, equipment will be put in service during 2023, not this year as originally planned.

I thought I was the exception, but in conversations with colleagues, I realize I am the current norm. A trio of events had the combined impact of making what should be simple investments in machinery and equipment anything but.

The most talked about, problematic event has been the strained supply chain. I am not sure exactly how much of the problem getting machinery and equipment is directly attributable to the supply chain, but it has indeed had an impact. When obtaining lead-time quotations, availability of parts, chips, etc., are always the culprit cited for the long length of time to build the equipment, whether a complex custom-built item or simply a copier for the office.

That is only half the story, however. Shipping times to get equipment from location of origin to your facility are also taking significantly longer than before. It doesn't matter if the machine is shipped from Asia, Europe or North America, or if the delivery is foreign or domestic; availability of planes, trains or container ships is as stretched as the supply chain of parts. Events taking place in Ukraine are exacerbating availability of raw materials, parts and shipping options.

Navigating the Covid world has also had its impact on the ability - and especially speed - to select what machinery and capital equipment to purchase. When compiling a capital budget, it is easy to say you need a drill, image, press or pick-and-place machine, but doing the due diligence to select the correct machine is something quite different. Historically one could attend trade shows, visit sites, see the equipment in action and run test jobs to see the results - all activities most efficiently handled by in-person visits to possibly multiple locations. In the Covid world of Zoom, WebEx, etc., doing the necessary due diligence required to select the best piece of equipment and then get approval to invest considerable sums in capital equipment has become much more challenging and a far lengthier process.

PETER BIGELOW is president and CEO of IMI Inc.; pbigelow@imipcb. com. His column appears monthly.



In particular, a process to select, prove out, and negotiate the purchase of a piece of equipment that in the past might have taken weeks now takes up to a year – and that is before pulling the trigger to commence the order. Companies that once let an equipment supplier and potential customer in to see a piece of equipment and run samples now may not allow visitors. Capital equipment manufacturers may have sold the demo equipment normally available for running tests. Equipment manufacturers' sales and demo staffs may be working remotely – with no equipment available – and limited access to their factory to conduct sales demonstrations. Altogether, unless you are buying a duplicate of what you already have, the selection and due-diligence process rivals the supply chain issues, consuming valuable time in the equipment selection and procurement process.

The final challenge is inflation, which is relatively new but may become significant. With demand so high for all sorts of industrial and consumer items, and with the supply chain in such a strained state, the cost of components, raw materials and, therefore, the finished product is escalating at rates not seen for decades. When budgeting a capital expenditure, and completing the (long) process of selection and due diligence, finding out the cost is five to 10% or more higher may necessitate rethinking the equipment or timing of the investment. For any purchased capital investment via a loan, lease or line of credit, rising interest rates inflate the total cost of investment.

As much as inflation has impacted prices of new equipment, it pales in comparison to the impact inflation has had on the used equipment market. With lead times for new equipment stretched so far, a premium is now paid for readily available used equipment in good condition. In fact, it has been reported some used equipment is selling for more than it costs new. The lack of availability of new equipment, coupled with long lead times for new machines, is compounding the effect of inflation. As supply chain difficulties continue, inflation may become the biggest challenge in planning specific capital investments and preparing a capital budget.

So, regrettably, I am looking good for putting 2023 capital investments in service, but not so for 2022. I guess it's time to plan for 2024 ... or maybe even 2025.

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### PCB Panelization Costs: It's All About the Real Estate

Just like housing, a little extra size can cost a lot more.

PRINTED CIRCUIT BOARDS in panel or array format increase the efficiency of the assembly operation, especially in volume applications. Takt time is greatly reduced, and handling of product is easier. However, rising material prices are cutting into that advantage because more material is required to produce those arrays.

PCB costs are based on the amount of raw material required to make a particular board. The metal finish, like ENIG or silver, plays a part in pricing, but it is the amount of fiberglass and copper needed that really determines the final cost.

The quoted price for most boards in panel or array format is based on a fabricator's desired panel price for a particular technology or quantity, divided by the number of arrays (or pieces) that fit on a standard 18 x 24" manufacturing panel. The more arrays or pieces

that fit on the panel, the lower the cost.

Whether that price is dictated by the number of boards (arrays) that can fit on the standard manufacturing panel, or by the total square inches of the finished array, a quarter or halfinch too long in one direction may mean a double-digit price difference.



FIGURE 1. A PCB in one of three configurations. Less real estate equals savings.

That price difference is a double-edged sword: Either the board eats into profits because it is costlier to buy, or it's a missed sales opportunity because the board could have been quoted at a lower cost.

I have seen inefficiently panelized PCBs so many times. Sure, there is always some waste in manufacturing, but how much money is the contract manufacturer throwing away on *every* assembly?

Maybe that board does need a full inch of material railing on all four sides for it to be assembled, but it's worth asking whether that was the original array when the assembly was still in its prototype stage. Could it be it was never optimized for production? Did anyone bother to ask?

Buyers who want better panelization pricing must ask:

"Do we have to have railing on all four sides?" "Does the railing need to be that wide?"

er railing *is* needed, especially if a particular assembly requires something special. An example is a component that overhangs the edge of the board and requires extra spacing. In that case, the PCB buyer's engineering department should let purchasing know of any special requirements prior to sending them to the fabricator for a quote.

"Can we score instead of route?"

realized when the right questions are asked.

ing only 12 arrays per manufacturing panel.

FIGURE 1 shows a PCB placed in an array in one

The tab-routed array on the left with a large railing

The design in the middle has a much thinner railing, but still on all four sides, with scored spacing in

of three configurations, revealing the cost difference

on all four sides is the least cost-effective design, yield-

between the boards instead of the route. That half-inch

difference in one dimension makes all the difference.

and just two thin rails are needed along the longer

edge. Eight more arrays (a 75% increase) are available

from that same manufacturing panel compared to the

routed array.

Depending on

the board manufac-

turer, square inches

of the finished prod-

uct can also be used

to calculate pricing,

especially for larger

volume orders, and illustration

holds true for that

method as well.

Fewer square inches

mean a lower cost

Sometimes larg-

per array or piece.

this

The design on the right is the most cost-effective, where the PCBs are "butted" up against one another,

permitting 25% more: 15 arrays total per panel.

Additionally, board buyers need to talk to their production and engineering departments and ask for a company standard for assembly criteria that can be incorporated into PCB fabrication specs.

Ensure your PCB suppliers have those specs in hand, so the quotes they submit meet your assembly criteria without adding unnecessary costs or delaying quote response times.

The wasted green I see on the production floor is not solder mask. It's dollars. PCB buyers need to see that too.

GREG PAPANDREW has more than 25 years' experience selling PCBs directly for various fabricators and as founder of a leading distributor. He is cofounder of Better Board Buying (boardbuying.com); greg@directpcb.com.





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### EMS M&A: Will Your Exit Strategy Be Customer Beneficial?

Firstronic and Lacroix took a long-term approach to joining forces, eliminating the usual learning curve.

AS A 40-YEAR veteran of the electronics manufacturing services industry, I've seen my share of EMS mergers and acquisitions from both sides of the equation. The basic EMS industry business model adds complexity to that equation not found in most industries because EMS companies are an extension of their customers' manufacturing operations or, in some cases, their entire manufacturing operation. If a larger conglomerate acquires the company that manufactures your dish soap, you won't notice unless the product's effectiveness or branding changes dramatically. If your EMS provider is acquired, it's obvious on day one.

In many transactions, the only consideration of impact to an EMS company's customer base is visits to key customers during the due diligence phase to enable the acquiring entity to assess whether the business levels they anticipate are likely to continue in the new entity. The alignment of EMS brand/differentiating processes and facility redundancy are often minor considerations.

Choices to sell typically fall into one of six categories: aging or death of key ownership, desire of a primary investment partner to exit, seller's perception of economic trends in its markets, financial distress, desire to divest a subsidiary nonaligned with parent company financial performance goals, or an incredibly good offer.

Reasons for buying also typically fall into six categories: expansion into new geographic or industry markets, growing market share, acquisition of specific customers, pressure from a dominant existing customer to add capabilities or geographic reach, investment partner pump-and-dump rollup strategies, or the ability to acquire an operation at fire sale prices.

The rationale behind selling and acquiring EMS companies isn't necessarily bad. While the ones with the weakest business reasons or greatest operational redundancy often have steep learning curves or take longer than anticipated to become accretive, most acquisitions succeed. The new entity integrates, and customers that fit the model stay. However, the nature of M&A transaction motivation drives a short timeline that may not prioritize maintaining an unchanged customer experience business model.

Recently, I watched Firstronic go through this process. Since John Sammut and his team joined the company in 2011, Firstronic has had a tradition of breaking industry paradigms, so it is no surprise their approach in this area was also innovative. It is one of the more unusual – and customer-beneficial – transactions I've seen over the last 40 years.

When Sammut's team started at Firstronic, they had limited capital for expansion and were targeting a customer base that wanted a global network of facilities. To address that, they focused on building a North American footprint with factories in Michigan and Mexico and set up a joint venture in China and strategic alliances in Eastern Europe and India. As their business evolved, they decided to use this model to align with a partner capable of acquiring the business longer term, essentially setting up a business succession strategy.

In 2017, Lacroix, an EMS provider headquartered in France, purchased a minority stake in Firstronic, then acquired majority control of the company in 2021, when Firstronic's primary investment firm chose to exit the business. That exit strategy included soliciting and entertaining other offers, so there was no valuation downside to this longer-term approach to exit-strategy planning.

From an organizational and customer perspective, this approach was extremely beneficial. The original relationship was based on mutual need. Firstronic needed a strong EU footprint to reassure customers desiring the flexibility to implement a regionalized manufacturing strategy that it could accommodate them across all regions. Lacroix needed a strong North American and China footprint for the same reasons. Firstronic had the North American footprint, and its joint venture partner Maxway provided the China footprint. In short, there were no redundant facilities, and the combined facility locations aligned with customer support preferences. (Maxway remains a shareholder and a valued partner in the combined entity.)

There was also alignment in industry focus. Firstronic's focus has been automotive, industrial and medical. Lacroix targets industrial automation, home and building automation, civil avionics and defense, and healthcare. From a capabilities perspective, Firstronic's approach to Lean manufacturing and operational metrics was attractive to Lacroix. Lacroix's larger size and associated economies of scale were attractive to Firstronic. Lacroix also added design engineering capabilities to the mix.

However, the largest benefit has been the time the teams have had to develop processes to work together. When an M&A transaction happens on a short timeline, integration has a learning curve that customers

continued on pg. 37

SUSAN MUCHA is president of Powell-Mucha Consulting Inc. (powellmuchaconsulting. com), a consulting firm providing strategic planning, training and market positioning support to EMS companies, and author of Find It. Book It. Grow It. A Robust Process for Account Acauisition in Electronics Manufacturing Services: smucha@powellmuchaconsulting. com.



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### **Covid Class Creations**

The PCB East keynoter gives a roundup of innovative technologies to come out of the pandemic.

WE HAVE GONE where no mask has gone before! The Printed Circuit Engineering Association (PCEA) held its first regional conference and exhibition in Marlborough, MA, in April.

A resurrected PCB East drew attendees from as far as the West Coast and Florida. There is nothing like in-person contact. The social aspect of networking has been missing for far too long. The enthusiasm of the attendees bodes well for future face-to-face regional gatherings.

It was great to see so many old friends in the real world, while meeting new young engineers and entrepreneurs such as Yitzi Ehrenberg and David Kanarfo-

gel of Conformant, who have developed a new additive circuit process based on an innovative CVD system.

IPC and retired industry legend Dr. Laura Turbini joined many notable attendees, including Dr. Hayao Nakahara, Anaya Vardya, John Vaughan, Chrys Shea and Peter Bigelow, president of the SMTA Boston Chapter.

The many design and engineering programs conducted during the three-day meeting and exhibition by such experts as Susy Webb, Rick Hartley and Steph Chavez brought attendees up to date.

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This aerospike rocket engine was engineered in Hyperganic Core using advanced software algorithms and has never seen a single piece of manual CAD. It's likely the most complex additive manufactured part ever produced; it broke all conventional workflows. The part could not previously be designed, let alone built. It is said to be about 20% more efficient than previous bellshaped parts.

structures by the precision dispensing of a variety of conducting and insulating materials, Dr. Jaim Nulman of the AME Academy stirred our imaginations with a two-hour introduction to 3-D additive manufactured electronics.

During my keynote "From Possibility to Reality," I discussed new and emerging technologies from Israel, Germany, the US and Japan. The image of a rocket spike created by Hyperganics' algorithmic engineering platform that used AI to design and print the complex part amazed a full lecture hall. The detailed combustion chambers, which can only be created by software, ensure it doesn't overheat.

The theme was Covid Class Creations: products and processes developed, improved, modified and introduced during the pandemic. A number of new products under advanced development or on the verge of commercialization not yet seen in the marketplace were presented.

Luminovo's rapidly growing software suite for PCB design and manufacture, not yet available in the US, drew a lot of attention. Among its features is one

> that can calculate and predict design violations. It also calculates supply chain risk assessments.

> Averatek's A-SAP process (semi-subtractive process, or SSP, by some) allows the design and fabrication of  $25\mu$ m lines and spaces, illustrated by a part produced at American Standard Circuits, as was Rogers' new resin for 3-D additive manufacturing (by spray) that resulted in printable and plateable parts.

> Atotech's new electroless – yes, I said electroless, *not* immersion – tin process was intriguing! The process did not dissolve copper from the base plated, is not dependent on its position in the periodic table in reference to the metal(s) – usually copper – and did not stop depositing when

the base was sealed. Therefore, no dissolved copper contaminates the solution. The company also introduced a new oxide replacement for MLB manufacture, which left a smoother surface for HF and VHF needs.

As we contemplate new materials for 5G and 6G

### Reasons to Go Beyond the PCB Constraints

Keeping some margin on the table increases the chances of immediate success and leaves a little bit for later.

THERE ARE MANY more ways to constrain a PCB layout than when I started my journey as a semiintelligent designer. Guardrails were put in place to smooth transition into fabrication once the layout is completed. The other thrust of newer rules concerns the shrinking timing budget of our digital interfaces, particularly the memory banks.

We have so many aspects we can control that it can be tempting to disable or ignore some of them. That is a completely rational choice to make. New features take time to learn and implement. It may not be so easy to get everyone on board for a new feature or a whole new iteration of the software.

I remember getting buy-in to move up to a different whole number revision of the ECAD tools by and soldering the components to the board with a high yield. The test team has to bring up and debug the prototypes while working out a test plan for mass production. In final assembly, or second-op, hands are laid upon the completed board, and it is installed wherever it may have to go. Regulatory, quality, reliability, sales, marketing and other technical and nontechnical groups depend on our skillful use of tools we have been given to do our jobs. Last on the list but first in priority, the true owners of the design are our end-customers.

All these people, along with the company's shareholders, have a stake in what we do every day. Someone approved the purchase of these CAD tools based on the promise that it would enable a smooth evolu-

reminding the team we didn't *have* to use any of the new features and could go on using the tool exactly as before. It's easy to get comfortable with what you have if that gets the job done to everyone's satisfaction.

What we do is observed by many of the people around us. A narrow focus ends with the various EEs and your management team. Truly satisfying everyone takes a much wider view of the situation. Who is watching?



FIGURE 1. PCBs of all shapes and sizes have room for improvement.

tion from concept to fully realized product. These end-to-end solutions are typically tied to whatever the chip team uses for the silicon, if you happen to be part of a company that has its own chipset. The onus is on us to make the most of the tools with which we are provided to make that vision come true. To do that, we have to get inside the PCB factory and analyze how materials flow through and are combined in the process.

JR. is a career PCB designer experienced in military, telecom, consumer hardware and, lately, the automotive industry. Originally, he was an RF specialist but is compelled to flip the bit now and then to fill the need for high-speed digital design. He enjoys playing bass and racing bikes when he's not writing about or performing PCB layout. His column is produced by Cadence Design Systems and runs monthly.

**JOHN BURKHERT** 



Practically the whole company – and then some.

We also serve the document control group with cohesive data in terms of names and descriptions that match what is established by the system. Purchasing has to bear the brunt of the flurry of technical questions when our documentation or design work is not up to standards. The PCB fabricator's CAM team has to create the phototools from the geometry we provide. What they may have to do in the name of global micro-editing might surprise you. The manufacturing engineers have to automate the process of attaching The imperfections of layering: The cake is a lie!

One of the first things to consider is layer-to-layer misregistration. No factory can consistently replicate what we have on our screens. If it could, we would not need a capture pad on the via. The drill and all the artwork would lay up perfectly, and that is not the case. The drill does not hit the exact spot over and over, and every layer of the board varies in its precise location (registration) with respect to the others.

Unless the PCB is Class III, it is designed to permit

the drill enough positional leeway to miss the center of the pad by enough that it winds up with 25% of the hole outside of the copper area. Even if every layer has that kind of breakout in a different direction, that is still an acceptable board according to IPC standards for Class II PCBs.

An industry standard via hole is 8 mils (0.2mm) with an 18-mil pad. That's plus five-thousandths all the way around in a perfect world. First, we consider the drill tolerance, and note it has to start out larger than the finished hole because the fabricator has to add a minimum amount of plating to the barrel of the via. That plating takes up one of the 5 mils we have to play with.

Account for drill size (+0.003/-0.018) and location accuracy (+/-0.003) over layers of naturally mis-registered artwork, and the 18-mil pad is not enough to contain it all. This is an important point, so let me put it anoth-

er way: Simply deleting the capture pad on a layer does not mean the drill won't require the same amount of metal pullback from the circuit pattern as if the via's pad were left in place.

Deleting nonfunctional pads does not create space. While doing so might look better to the signal integrity simulator, those nonfunctional pads serve a function. They help anchor the plating in the via. Plating down into little mechanically drilled holes isn't easy. Most board designers have had a call from a vendor who wanted to discuss reducing the minimum plating requirement for the via walls, even though we're using standards.

but it happens.

By worst case, I mean as far out of specification a layer can be while still meeting the misregistration requirements set forth in the design. If we could have tooling holes with plus/minus zero on both size and positional tolerance, this stuff would be

> easy, and our monitor would depict the actual nature of the boards. Of course, even non-plated holes have their tolerances. For this reason, I like to have a little more of a buffer around the via on the trace layers. Where possible, using a via-to-line spacing rule that is a little more than the via-to-shape rule will keep the trace from ending up over a void when accounting for misregistration. You can use the same value for both, route everything and never see a design rule violation.

> In our imperfect world, that is a recipe for routing over those voids by just a little. When you look at

> > simulations of a high-speed line running next to a void, the EMI fields will be more prominent near the broken plane. Tiny discontinuities add up, especially with analog designs. Higher bit rates start to look like RF traces too, so no one is safe from natural variation.

#### Parallelism and crosstalk.

Running traces in parallel causes crosstalk. Using the minimum manufacturable spacing is fine over the short haul. Even a little bit more space means a lot. I just finished a board where I used 5-mil traces for the default non-impedance-controlled line width, then changed all of them to 4 mils once every-

Knowing we have to account for the slop in the process is the first step to glorious results. The anti-pad or via-to-shape rule is one of those places in which I've seen designers try to cut corners. Tightening that up ignores the bulge in the via's pad permitted by the drill tolerances. One of the things we're advised to watch out for is routing over a void.

Monte Carlo simulations: Gaming the system. We could come up with random numbers that permit natural variation of the location of the relevant ground planes and their adjacent layer traces. A worst-case scenario on one layer meets a worstcase scenario on the next layer very rarely in the real world, thing was routed. Four mils is enough width for innerlayers, while reducing the metal, and thus the amount of overall radiation of the system. Going from 5 to 6 mils on the air gap reduces crosstalk considerably, since crosstalk is a squaring function rather than a linear one. A little space goes a long way.

Emissions and susceptibility, the two tenets of de-sense, are both favorably impacted by this approach. Down the road, that cumulative space will not be wasted. Going that extra mile also preserved a tiny bit of open space that could be taken on Rev 2, where it seems inevitable we will add a signal somewhere among those traces where there is just enough extra air gap – and then some.  $\Box$ 



FIGURE 2. Breakout is expected in Class II PCB layouts. (Source: Viasystems)



FIGURE 3. Start with three queens and see how many times you

can fill the dance card by playing the same hand 100 times. Mod-

ern video poker allows such scenarios. We set up the parameters

and get the results in production. Good luck.

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### **Onshoring and Second Sourcing**

The current difficulties call for a more strategic approach to arranging our global supply chains.

THE SUPPLY CHAIN chaos in the aftermath of the pandemic has highlighted the risks associated with globalization. As a phenomenon, globalization has served many of us well. Its ideological opponents, however, see today's situation as justification for its demise. There is no denying current events have highlighted shortcomings. We would be foolish not to learn and adapt.

I've addressed the subject of onshoring as a potential antidote to globalization many times in the past. Arguably, now, the idea makes more sense than ever. On the face of it, shorter supply chains promise some protection against the unpredictability of today's world. Hot on the heels of the pandemic, we now have the Ukraine crisis, and there is the fallout from Brexit, which has made for difficult and time-consuming trade between the region's most influential economies. One major obstacle to the return of onshoring is essential indigenous-supporting industries have been largely swept away as activities have migrated offshore, taking expertise and investment with them. The conditions that caused and drove the offshoring remain in place, perhaps masked by current logistical difficulties. Accessing the data needed to move manufacturing activities from an established location is another barrier to reshoring.

If replacing globalization is not practicable, then arranging protection against its disadvantages is surely a sensible move. We might forgive ourselves forgetting this wisdom during the long period of relative peace and stability we have enjoyed in the West, probably since the end of World War II. Logistics is a major aspect of our business, which is to supply high-value materials. Without good logistics, there is no way to deliver, and without a delivery mechanism, there is no business. Keeping the supply chain simple, with as few external partners as possible, has protected against many problems over the past few years. The more partners there are in any supply chain, the more difficult it becomes to control, and the greater the risk that a link will fail.

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**ALUN MORGAN** 



Now, after the pandemic and while critical resources like shipping are still struggling to return to their normal places and routes, we have the Ukraine crisis. We have not yet felt the full effects of this. Some lead times for important materials in PC fabrication have increased to a year, which seriously challenges companies' ability to control deliveries to customers.

A large proportion of important natural resources, such as titanium and lithium deposits, are found in Ukraine. Forty percent of the world's palladium, which is used in catalytic converters, is mined in Russia – and is no longer accepted in leading bullion markets. This alone could seriously impact Europe's car producers, which, of course, are dependent on other materials heavily influenced by Russian suppliers, such as steel.

I believe we will not feel the full impact of the Ukraine crisis for some time. However, the effect will be significant. Other less high-tech industries are also affected by the disruption to materials supplies. Ukraine supplied about 25% of all clay consumed by Italy's ceramics industry, which had already been struggling with sharply rising gas prices at the onset of the conflict. To use sources from other locations, the ceramics engineers will need to modify their mixes. There are always imaginative reworkings of products and ideas, as industries deal with externally imposed changes. Our shared industrial heritage is all about adaptation in the face of adversity. However, workable alternatives often take time to conceive and implement.

This raises the question of second sourcing as a means of protecting against shortages in critical parts and materials. This is a sensible idea companies often do not enact simply because it is difficult, time-consuming, potentially more expensive, and, under most foreseeable circumstances, not needed. I remember when the earthquake and tsunami of 2011 in Japan caused an industry-wide shortage of a specialty pigment that was manufactured only in a single plant, which happened to be in the affected region. It was a strange problem, largely unforeseen, that had unexpectedly serious – although entirely predictable – consequences.

The problems we are all experiencing right now will likely continue for some time, so the need for a second source may become increasingly apparent as the crisis continues, but now is not a great time to be desperate for a rare commodity.

As an industry, if we are to remodel our global supply chains to be more resilient and provide protection against future disasters, we may benefit from developing easy and cost-effective approaches to arranging a second source.

Of course, making large changes also requires investment, which requires a worthwhile return for investors. So, if reshoring some of the industry's key activities were to make sense from a political or ideological standpoint, or for environmental reasons, there are substantial practical justifications for reshaping and ruggedizing the structures we have.

### Where is My Flex?

When designing a rigid-flex, start with flex in the middle of a stack-up and move outward.

YOU'RE DESIGNING A new rigid-flex. Devices are getting fanned out, via structures defined, and layer count is becoming clearer. You have determined how many flex layers you need from rigid section to rigid section. There are competing considerations on how those flex layers are configured: foil and dielectric thickness, bonded or unbonded, and where they will be in the stack-up of layers. All this impacts flexibility and how the part will bend in the installed application.

For today, let's concentrate on where the flex layers land in the stack-up and the effect that can have on manufacturing and end-application use. Several strategies have rational logic and can be successful in select situations.

The most common and lowest impact is to place the flex at the middle of the stack-up. There are several advantages. First, it permits symmetry of the stack-up. Symmetry provides the opportunity for the flattest stack-up with the least tendency for bow and twist. This is more and more critical as component pitches get denser, and the size of BGAs and FPGAs gets larger. This is also the easiest to fabricate with the lowest cycle time, resulting in the lowest cost. If you can put the flex in the middle of the stack-up, this is the best option.

In some cases, the flex needs to be a little offset from top to bottom. For example, maybe you only want one or two rigid layers before you get to the flex, but then on the bottom you need four layers for the remainder of the design. Maybe you needed to do this to get some sensitive signals down the flex with the minimum amount of via distance and stub length. This is usually fine. There may be some increased tendency for warp, but it should be manageable.

In other cases, flex layers are moved close to the top or bottom of the stack because they may move the bend radius inward or outward. While this is true, it may only change the bend radius by 0.010" to 0.050". Hopefully the safety factor of the design is not so slim that this is the only option to achieve an acceptable solution. Depending on the total thickness on one side versus the other, this can result in warpage. Differential contraction of the materials during cooling after lamination causes this warpage. In many cases, this will impact assembly such that the surface of the panel is sufficiently warped, and solder joints are compromised. Without some post-processing (re-lamination), the part may not meet bow-and-twist requirements. Or if it does, it may warp during SMT assembly. I have seen cases in which the warpage was so severe we could not finish processing the circuit panel fabrication. We could not lay it down on a drill or send it through wet process equipment.

Another design strategy is to place the flex at the outer layer(s), like in **FIGURE 1**. While this can be done, it requires some technical consideration. For starters, using this example, there will be distortion of the flex material at the rigid to flex transition. Since there is no prepreg between layers four and five, the flex substrate for layers five and six will follow the topography above it. If layer six has traces that span from the rigid-to-rigid section, the conductors will distort as well. In some cases, when the traces are narrow, they may be prone to etch flaws, lowering yield. Resist coating, imaging and etch are affected by this distortion. Conductor distortion may also lead to assembly failures, if those conductors are bent tightly or are under strain. They may be more prone to cracking.

Additionally, these types of designs cannot have through-vias that are filed and capped. This is because the planarization operation will almost certainly damage layer six and the associated substrate.

On the flip side, this type of construction does have an advantage from a conductive anodic filament (CAF) point of view. If the design has sub-0.8mm-pitch packages, and microvias are used from layer six to five, there is no risk of CAF between these vias, as the polyimide flex substrate has no weave; thus, it is not susceptible to CAF.



FIGURE 1. A design strategy placing flex at the outer layer(s).

A variation on this theme involves the outermost layer as part of a flex core, but it only has copper features in the rigid regions of the board. Using Figure 1, layer five still has conductors in the flex and rigid regions, but layer six only has features in the rigid

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continued on pg. 47



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### Printed Circuit Engineering Professional

#### Table of Contents:

### Chapter 1: Professional Overview

- 1.1 Printed Circuit Engineering Layout Overview Profession overview
- **1.2 Basic Fabrication of a Printed Circuit Board** Materials and construction
- 1.3 Basic Assembly of a Printed Circuit Board Materials and process
- **1.4 Basic Electronics in a PCB** Fundamental understanding and concepts
- 1.5 Basic Printed Circuit Engineering Layout Overview – Layout process
- **1.6 Project Management (PM)** Enabling project success and accountability
- 1.7 Communication –throughout the process

### Chapter 2: Circuit Definition & Capture

- 2.1 Libraries to Bill of Material (BOM) Integrated library: symbols, land patterns
- 2.2 Surface Mount and Thru-Hole Technology Components and process
- 2.3 Schematic Types and Conventions– Functional, logic, flat and hierarchal
- 2.4 Schematic Symbol Placement Orderly circuits improve comprehension
- 2.5 Schematic Review Complete and accurate
- 2.6 Circuit Board Types Rigid, Flex and Printed Electronics
- 2.7 IPC MIL Standards and Specifications Reference listing of standards
- 2.8 Verification, Testing, Compliance & Qual. Assurance
- 2.9 Mechanical Board Information –Physical requirements
- 2.10 Database Links and Iterative Data Exchange Development iterations

### Chapter 3: Board Layout Data & Placement

- 3.1 Board Parameters Set-up CAD environment
- 3.2 Stackup Design Z-Axis relationship
- **3.3 Constraints and Rules –** Define and implement accurate reliability
- **3.4 Placement for Assembly** Performance and buildability
- **3.5 Placement of Components** Solvability, performance, and manufacturing
- 3.6 Schematic Driven Placement Cross-probing
- 3.7 Placement Dense Digital Circuits (LSI) Large Scale Integration
- **3.8 Placement Power Delivery** Source, distribution, and usage
- 3.9 Placement Mixed Circuit (RF/HSD) Together
- 3.10 Placement Review Milestone Approval for routing

### Chapter 4: Circuit Routing & Interconnection

- **4.1 General Overview of Routing** Fundamental parameters
- 4.2 Routing Dense Digital Circuits Modular approach
- 4.3 Routing with Signal Integrity Applications Managing energy fields
- **4.4 Routing Power Delivery** Source, Distribution, and Usage
- **4.5 Routing RF Circuits** Managing dissipation and loss
- 4.6 Routing Review Milestone Approval of routing

### Chapter 5: Flex Printed Circuits (FPC)

- 5.1 Flex and Rigid-Flex Technology Overview and Introductions to FPC
- 5.2 Flexible Printed Circuit Types IPC definition
- **5.3 Flexible Circuits Applications** Industry sectors and usage
- 5.4 Materials for Flexible Circuits Properties and process
- 5.5 Design Start Considerations Physical and electrical
- 5.6 FPC Stackup Constructions Usage and process
- 5.7 Flex Design Practices Physical and electrical aspects
- 5.8 Production Process Consideration Process flow
- **5.9 Conductive Surface Finishes** Overview of types and process
- 5.10 Stiffeners Types and applications
- 5.11 Shielding Material EMI and EMC considerations
- 5.12 Design for Manufacturability and Assembly Unique concerns building FPC

### Chapter 6: Documentation & Manufacturing Preparation

- 6.1 Documentation Overview Prepare for the final design effort
- 6.2 Resequencing Reference Designators Backannotation
- 6.3 Silkscreen Providing visual intelligence
- 6.4 Industry Standards Design, document and build compliance
- 6.5 Post-processing Procedure Know what to expect at your company
- 6.6 Manufacturing Deliverables Documentation
- 6.7 Fabrication Drawing Instructions to fabricate the bare board
- 6.8 Assembly Drawing Reference drawing used to assemble the PCA
- 6.9 Schematic Database and Drawing Circuit capture and BOM origin
- 6.10 Bill of Materials (BOM) Controlling document
- 6.11 Final Deliverables Formats and creation process
- 6.12 Transfer to Manufacturer Manufacturing interface

### Chapter 7: Advanced Electronics, EM Applications

- (During the review class only cursory coverage of Chapter 7 will be provided due to the advanced nature of this content.)
- 7.1 Energy Movement in Circuits –EM Theory
- 7.2 Critical Frequencies in Circuits on PC Boards Frequency and Rise Time (Tr)
- **7.3 Transmission Lines in PC Boards** Relational nature in electronics
- 7.4 Understanding Impedance of Transmission Lines Modification from layout
- 7.5 Impedance Control of Transmission Lines Controlling impedance in layout
- **7.6 Controlling Impedance of Digital ICs** Controlled and set to specific values
- 7.7 Controlling Noise Margin Critical lengths understanding
- 7.8 Crosstalk and Cross-coupling Capacitive and inductive coupling
- 7.9 Controlling Timing of High-speed Lines Timing matched, not length

### **Reflections from DISCONTINUITIES**

A single one can destroy a signal, but predictions with validated models can be made. by YURIY SHLEPNEV, PH.D.

An ideal digital interconnect is a lossless transmission line with characteristic impedance and phase delay flat over the signal bandwidth and termination resistors equal to the characteristic impedance. In such interconnect, bits generated by a transmitter would flow seamlessly into the receiver with no limits on the bit rate. Such a utopian transmission line exists only in our imaginations and textbooks. The physics of our world prohibit it. One way to describe "what happens to the signal on the way to a receiver?" is to use the balance of power that can be written for the passive interconnect as follows:

#### P\_out = P\_in - P\_absorbed - P\_reflected - P\_leaked + P\_coupled

This is frequency domain over the bandwidth of the signal.<sup>1</sup> P\_out is the power delivered to the receiver, and P\_in is the power delivered by transmitter to the interconnect. All other terms in the balance of power equation describe the signal distortion. The formula above expresses all we need to know about the interconnects. (It should be "cast in granite."). As they say, "a formula is worth a thousand words," almost literally in this case. To understand it, imagine the interconnect system as a multiport with the transmitter at port 1, receiver at port 2 and multiple other ports for links coupled to the link connecting port 1 and 2 and terminations to real impedance (not necessarily identical at all ports) – something like this below, together with the definition of waves and scattering parameters (or S-parameters):



FIGURE 1. The multiport interconnect system with waves and S-parameters.

Harrington's concept of "loaded scatterers" allows us to turn any interconnect system (even malfunctioning as an antenna) into a multiport and describe it with the waves and scattering parameters as it is done in the image above. Also, choice of real Zo for all ports makes those waves the "power waves." Now we can define the powers in the balance of power equation through the multiport waves a and b as follows:

- P\_in is power delivered into the interconnect by transmitter:
   P\_in = |a1|^2 [Wt]; |a1| is magnitude of the incident wave at the transmitter end or port 1;
- P\_out is power delivered to the receiver: P\_out = lb2l^2
   [Wt]; lb2l is magnitude of the transmitted wave at the receiver er end port 2, assuming la1l != 0 and no incident waves on the other ports lakl = 0 for all k != 1;
- P\_absorbed is power absorbed by dielectrics and conductors (more below);
- P\_reflected is power reflected back to the transmitter: P\_ reflected = lb1|^2 [Wt]; lb1| is magnitude of reflected wave at the transmitter end, assuming no incident waves on the other ports lak | = 0 for all k != 1;
- P\_leaked is power leaked into the other coupled interconnects, modes and possibly into the power distribution network (PDN) and into free space (radiated): P\_leaked = sum(lbkl^2 [Wt], k != 1,2; lbkl are waves transmitted to the ports of the coupled interconnects; lakl = 0 for all k != 1;
- P\_coupled is power gained from the other coupled interconnects, modes, PDN and free space: P\_coupled = lb1|^2+lb2|^2 [Wt]; a1 = 0, a2 = 0, ak != 0 for all other k.

Let's examine those terms further. First, let's assume the link is localized somehow – no coupling or P\_leaked = P\_coupled = 0. It is hard to do for the real-life open waveguiding systems such as PCB or packaging interconnects but is close to reality for properly designed interconnect systems. The remaining balance of power is:

#### P\_out = P\_in - P\_absorbed - P\_reflected

What can we learn from this simple expression? P\_out characterizes the transmitted signal and includes signal distortions from absorption or dissipation<sup>2</sup>, as well as from all kinds of reflections. This is important to know. If more power is reflected or absorbed, then less power is delivered to the receiver. That means more signal degradation or distortion. It is a little more complicated with the complex termination impedances. So, let's stay with the real termination impedances; the "black box," can take everything in. (It is not a simplification or approximation because all reactive parts of the termination impedance can be easily embedded into S-parameters.)

P\_out can be expressed as insertion loss (IL, positive number) in dB as follows:

$$IL = 10*log(P_in/P_out) [dB]$$

This is by definition. We can rewrite it with the magnitudes of the multiport waves as follows:

$$\begin{split} IL &= 10*log(|a1|^2/|b2|^2) = 20*log(|a1|/|b2|) = -20*log(|b2|/|a1|) = -20*log(|S21|) \end{split}$$

S21 is the transmission parameter – transmission from port 1 to port 2. The insertion loss is negative magnitude of the transmission parameter S21 in dB.

P\_absorbed characterizes all power losses to heat the materials (inevitable contribution to the increase of entropy). It can be expressed as follows (no coupling):

$$P\_absorbed = P\_in - P\_out - P\_reflected = |a1|^2 - |b2|^2 - |b1|^2 [Wt]$$

This is a useful formula, in case you want to evaluate the absorbed or leaked, if leaks are modeled with the absorbing boundary conditions, for instance.

P\_reflected characterizes the reflections and can be expressed as the return loss (RL, positive number) in dB as follows:

RL = 10\*log(P\_in/P\_reflected) [dB]

Again, this is by definition. We can also rewrite it with the magnitudes of the multiport waves as follows:

$$\label{eq:RL} \begin{split} \mathsf{RL} &= 10^* \log(|a1|^2/|b1|^2) = 20^* \log(|a1|/|b1|) = -20^* \log(|b1|/|a1|) \\ &-20^* \log(|S11|) \end{split}$$

Here S11 is the reflection parameter – reflection at port 1. The return loss is negative magnitude of the reflection parameter S11 in dB.

The absorption or dissipation losses in dielectrics and conductors were recently discussed.<sup>2</sup> Such losses are inevitable but can be effectively mitigated at the stackup planning stage; selection of dielectric and conductor materials and stackup geometry defines the maximal possible communication distance for a particular data rate and power required to transmit the signal.

Considering the reflections, they can be further separated into the following three categories:

- 1. Reflections from mismatch of transmission line impedance and terminations<sup>3</sup>
- Reflections from single discontinuities: transitions, vias, AC caps, length compensation structures and gaps in reference plane, etc.
- 3. Reflections from periodic discontinuities: fencing vias and cutouts, fiber-weave effect, etc.

Item 1 was discussed.<sup>3</sup> The most important thing for understanding the reflection is the formula for reflection parameter from a segment of transmission line with complex propagation constant Gamma, characteristic impedance Zc and length l terminated with Zo:

$$S_{1,1} = \left(Z_c^2 - Z_0^2\right) / \left(Z_c^2 + Z_0^2 + 2 \cdot Z_c \cdot Z_0 \cdot cth(\Gamma \cdot l)\right)$$

EQ. 1.

The reflection reaches the maximal values at frequencies where the transmission line length is the quarter of wavelength in line (Lambda) or Lambda/4+n\*Lambda/2 in line. (See definitions.<sup>3</sup>):

$$\max(S_{1,1}) = (Z_c^2 - Z_0^2) / (Z_c^2 + Z_0^2 + 2 \cdot Z_c \cdot Z_0 \cdot th(\alpha \cdot l))$$
  
$$\max(S_{1,1}) = (Z_c^2 - Z_0^2) / (Z_c^2 + Z_0^2), \text{ if } \alpha = 0$$

EQ. 2.

Here alpha is the attenuation constant that increases with the frequency.<sup>2</sup> This is another remarkable formula; the reflections are smaller for lines with more losses (greater alpha) and at higher frequencies.<sup>3</sup> The last part is valid only if there are no discontinuities. It makes everything clear with the choice of characteristic impedance; the closer Zc to the termination impedance Zo, the lower the reflections. A link with Zc = Zowould be the best link, if it would be possible to design and build it like that. What prevents us from doing so are all kinds of transitions. In reality, some parts of interconnects look like and can be modeled as the transmission lines. There are also transitions between the transmission lines: packages, connectors, via holes, length compensation structures, AC coupling capacitors, transitions between the transmission lines of different types or with different cross-sections. Accurate analysis of a complete link with the discontinuities usually requires validated software with 3-D electromagnetic analysis capabilities.

Before providing examples of such numerical analysis, let's write a couple of practical formulas for qualitative and quantitative analysis of the reflections from the discontinuities. The first formula is for the input impedance of a transmission line segment loaded with ZL impedance as follows:



**FIGURE 2.** A formula for the input impedance of a transmission line segment loaded with ZL impedance.
It can be easily derived starting with the exponential expansion by setting the boundary conditions on the right side. <sup>3</sup> The formula for the impedance can be used recursively starting from the receiver by including discontinuities in a transmission line that have expressions for the impedance: capacitances, inductances or combinations, stubs and so on. All you need to know is how to connect the complex impedances in parallel and in a series. As soon as we know the input impedance of the link at the transmitter side, the reflection parameter can be computed as follows:

$$S_{1,1} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0}$$

#### EQ. 3.

Note this is exactly the same value as the reflection coefficient usually designated with Gamma.<sup>4</sup> There are no differences in this context. The formula can also be inverted, to compute *Zin* from the reflection parameter.

Now, let's examine a few cases. First, if ZL = Zc then Zin = Zc, and the reflection parameter is S11 = (Zc-Zo)/(Zc+Zo). This is reflection from the ideally terminated transmission line segment or from the infinite transmission line. It correlates well with the S11 provided earlier for the transmission line segment with the infinite length. (cth is the unit in this case.) Another limit case is ZL = infinity. This is an open-circuited segment of transmission line. In this case, Zin is simple:

$$Z_{in} = Z_c \cdot cth(\Gamma \cdot l)$$

#### EQ. 4.

What can we learn from this in the context of interconnects? They can be used to model and explain the effect of stubs. The first order approximation for a via hole discontinuity is a transmission line model. If a via is going through all stackup layers, but connects only one surface layer with an interior layer, for instance, the remaining part of the via is a stub connected in parallel to the link. If stub length is a quarter of wavelength in a corresponding equivalent transmission line model, we have input impedance of the stub as follows:

$$Z_{in} = Z_c \cdot th(\alpha \cdot l)$$

EQ. 5.

It is zero if alpha or attenuation is zero. That means it short-circuits the link. With zero Zin, the reflection is S11 = -1. It doesn't matter what the other parts of the link look like. Never let it happen at the frequencies close to the Nyquist frequency! It is all transmission line trigonometry.

After having fun with the formulas and the limit cases, let's analyze a couple of ideal discontinuities first. The analysis can be done with the formulas as well (a good exercise), but it is much easier to do it with the software: Simbeor in this case. A 0.1pF capacitor connected in parallel into a segment of an ideal  $50\Omega$  transmission line (yes, ideal transmission lines exist

in the software as well) will have a magnitude of reflection (left graph, left axis, red line) and phase of reflection (left graph, right axis, brown line) (FIGURE 3).

Time-domain reflectometry (TDR) is also shown on the right plot. It is much easier to recognize the capacitance on the TDR plot as the "capacitive" dip. The TDR is computed here directly from the frequency-domain response with 40ps Gaussian step function.

Next, let's take a look at 0.25nH inductance connected in a series into the same ideal  $50\Omega$  transmission line segment (FIGURE 4).

The frequency-domain reflection magnitude shown in blue on the left graph is exactly as the reflection from the capacitance. (The values are intentionally selected to have it like that.) However, the phase is different, though difficult to conclude something from, and the TDR shows a clear "inductive" bump.

What if we combine 0.1pF capacitance and 0.25nH inductance as a C/2-L-C/2 circuit? The reflection will go down as in **FIGURE 5**.

That actually explains how the transmission line works: t-line has both capacitance and inductance with the ratio equal to the characteristic impedance,  $Zo = \text{sqrt}(L/C) = 50\Omega$ , as in this case. Although, the reflections in the frequency domain are small but not zero. This is because the model uses lumped L and C in the middle of continuous transmission line segment, and it behaves as the t-line only at lower frequencies. But TDR with 40ps rise time is almost flat and does not resolve such lumped discontinuity in this case.



FIGURE 3. The magnitude of reflection and phase of reflection of a  $50\Omega$  transmission line.



**FIGURE 4.** A 0.25nH inductance connected into a series in a  $50\Omega$  transmission line segment.



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Finally, a few practical examples of the electromagnetic discontinuity analysis with validation used in our DesignCon 2020 tutorial.<sup>5</sup> The first example is the capacitive via from the CMP-28 validation platform designed by Wild River Technology (FIGURE 6).

Modeled and measured magnitudes of the transmission and reflection parameters are shown on the left graph, and corresponding TDRs are on the right. The link includes coaxial connectors and launches (inductive bumps at the beginning and end).

The reflections in this case are not a showstopper; the link is short, and the added capacitance is not big. It was intentionally capacitive. (See more analysis-to-measurement correlation examples from the CMP-28 platform.<sup>6</sup>)

Two other practical examples with the analysisto-measurement correlation are from the EvR-1 project.<sup>7</sup> (See also app notes #2018\_01, 2018\_07 and webinar #8 at simberian.com.) **FIGURE 7** shows the modeled and measured magnitudes of the differential reflection, transmission parameters and differential and common-mode TDRs for a differential link with two vias from bottom to inner6 layers with stubs (structure EvR1-C1).

The via stubs almost short-circuited the link at about 20GHz. The reflection parameter (reddish lines

with circles) went up, and the transmission parameters (bluish lines with stars) went down around the stub resonance frequency. With the transmission below -30dB, the signal harmonics at those frequencies will not go through. Corresponding differential TDR shows a big capacitive dip at the via location, though it is difficult to conclude from TDR at which frequency the via would destroy the signal. Notice the correlation between the model and measurements is as good as it usually gets. This is because of the "sink or swim" approach.7

What can be done to avoid such harmful reflections? Via backdrilling and optimization. FIGURE 8 shows structure EvR1-C2 with the backdrilled and optimized via holes for the transition between the same layers.

The reflection is below -10dB up to 30GHz and no bumps at the location of the vias. The link is as good as it can be for all practical purposes. Note the correlation of smaller reflections is more difficult to achieve because of the manufacturing variations that were also investigated for this particular board.<sup>7</sup>



FIGURE 5. The reflection of 0.1pF capacitance and 0.25nH inductance combined as a C/2-L-C/2 circuit.



FIGURE 6. Capacitive via from CMP-28 validation platform (Wild River Technology).



FIGURE 7. Magnitudes of the differential reflection, transmission parameters and differential common-mode TDRs for a differential link with two vias.

#### SIMULATION

The bottom line is the reflections, even from a single discontinuity, can destroy your signal. But the effect of the major discontinuities can be predicted with validated models before the board is designed (pre-layout analysis) and must be predicted after the board is designed and before it goes into manufacturing (post-layout analysis).

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#### Focus on Business, continued from pg. 22

often see played out in service anomalies. Comparatively, the teams have been working together for more than four years. There have been joint NPI efforts for customers using multiple facilities, so that process is already well understood. When Firstronic added equipment during that timeframe, they considered Lacroix's focus on Industry 4.0 automation strategy, in addition to customer requirements. At a systems level, there is enough compatibility to take a measured approach to any change. While Firstronic's ERP system will likely change to Lacroix's platform, at least for financial reporting purposes, Lacroix is evaluating Firstronic's MES as a potential companywide standard. In short, the integration process is likely to enhance the customer experience in terms of service delivery, since post-transaction Firstronic's customers have greater access to design engineering resources and the support capabilities found in a much larger entity.

From an economies of scale perspective, the combined entity has climbed to number 43 on *Manufacturing Market*  *Insider's* Top 50 EMS list, and Lacroix has achieved its goal of becoming the largest French EMS provider. Firstronic's long-term approach to laying the groundwork for its lead investor's eventual exit has achieved all the objectives of a traditional M&A transaction, with none of the learning curve issues of a fast transaction. Customers are seeing expanded capabilities and the economies of scale that come with a Tier 2 EMS company, without the growing pains that growth would bring if it happened organically. Financially, the acquisition has been immediately accretive to Lacroix. It is a win-win for all parties.

The concept of succession planning within management teams is well established to ensure continuity within an organizational hierarchy. The concept of succession planning in terms of this type of organizational evolution is not well developed in the EMS industry. The Firstronic-Lacroix transaction demonstrates the organizational and customer benefits that can occur with a longer-term approach to exit strategy planning.



FIGURE 8. Structure EvR1-C2 with backdrilled and optimized via holes.

## How to Calculate Trace Length from Time Delay Value for HIGH-SPEED SIGNALS

Here's an effective process for implementing PCB trace routing. by LANCE WANG

To keep a good high-speed signal quality from driver to receiver on a PCB is not an easy task for designers. One of the most challenging issues is managing the propagation delay and relative time delay mismatches. To manage the time delays, we need to know how to calculate trace length from time delay value to implement the PCB trace routing accordingly. Here's the process:

According to physics, electromagnetic signals travel in a vacuum or through the air at the same speed as light, which is:

 $Vc = 3 \times 108M/sec. = 186,000 \text{ miles/sec.} = 11.8 \text{ inch/} nanosec.$ 

A signal travels on a PCB transmission line at a slower speed, affected by the dielectric constant (Er) of the PCB material. The transmission line structure also affects the signal speed.

There are two general PCB trace structures\*: stripline and microstrip.



FIGURE 1. PCB trace structures.

The formulas for calculating the signal speed on a PCB are given in Equation 1, below:

Signal speed on striplines:
$$V_{p \ (inner)} \approx \frac{Ve}{\sqrt{Er}} \approx \frac{11.8 \ in/ns}{\sqrt{Er}}$$
 (1a)Signal speed on microstrips: $V_{p \ (outer)} \approx \frac{Ve}{\sqrt{Ereff}} \approx \frac{11.8 \ in/ns}{\sqrt{Ereff}}$  (1b)

\*Note: Different microstrip and stripline structures will affect the signal speed but only slightly. where

*Vc* is the velocity of light in a vacuum or through the air. *Er* is the dielectric constant of the PCB material.

*Ereff* is the effective dielectric constant for microstrips; its value lies between 1 and Er and is approximately given by:

 $Ereff \approx (0.64 \ Er+ \ 0.36) \ (1c)$ 

With those formulas, we know the speed of signals on a PCB is less than the signal speed through the air. If  $Er \approx 4$  (like for FR-4 material types), then the speed of signals on a stripline is half that of the speed through the air; in other words, it is about 6 in/ns.

#### Calculating Propagation Delay (tpd)

The propagation delay is the time a signal takes to propagate over a unit length of the transmission line.

Equation 2 shows how we can calculate the propagation delay from the trace length and vice versa:

$$t_{pd} = \frac{1}{v}$$
 (2a)

EQ. 2.

where

Vis the signal speed in the transmission line.

In a vacuum or through the air, it equals 85 picosec./in. (ps/in).

On PCB transmission lines, the propagation delay is given by (Eq. 3):

$$t_{pd} \approx 85 \sqrt{Er} \ ps/in$$
 in striplines (2b)

$$t_{pd} \approx 85 \sqrt{Er_{eff}} \, ps/in$$
 in microstrips (2c)

EQ. 3.

#### Case Study

To comply with JEDEC specifications, the maximum skew among all the signals shall be less than +/-2.5% of the clock period driven by the memory controller. All the signals of SDRAM are directly or indirectly referenced to the clock.

In this example, a conventional FR-4 material with a dielectric constant of 4 is used on the PCB with a differential clock rate of 1.2GHz (i.e., 833ps clock period):

**Question:** What is the maximum skew of the trace length for all the signals?

Answer: Max skew in time delay =  $\pm$ -2.5% of the 833ps clock period = 20.825ps FR-4 Er $\approx$ 4, Ereff $\approx$ 2.92

So, for striplines, the maximum skew should be less than +/-(20.825/(85\*SQT(4)) = +/-0.1225 in. = +/-122.5 mil.

For microstrips, the maximum skew should be less than +/-(20.825/(85\*SQT(2.92)) = +/-0.1433 in. = +/-143.3 mil.

Keep this information in mind the next time you're calculating trace lengths; it should make the job a little easier.

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LANCE WANG is a solutions architect at the Zuken SOZO Center (zuken.com). He supports the CR-8000 product line, mainly focusing on high-speed PCB design and signal integrity features. When not behind the keyboard or in front of customers, he is a Tom Brady fan and enjoys playing ping pong in his spare time.

What's Old is New, continued from pg. 24

applications, Isola introduced hybrid laminates, combining PPE with outer layers on FR-4, as well as other combinations. The company also provided data on its new green materials.

Nano Dimension provided information on the progress of its activities to make 3-D inkjetted printed circuit structures containing passive components,  $75\mu$ m lines and spaces, and  $45^{\circ}$  pad-less interconnects between levels with its most recent DragonFly IV system.

PulseForge's use of photonics to replace IR or laser for soldering permits soldering to curved or flexible surfaces, soldering to PET or paper (e.g., LEDs to flexible substrates), reel-to-reel

and soldering batteries to substrates for single-use medical devices. The use of photonics can be used to cure protective coatings or sinter metallic pastes – all in seconds with 75% less power than IR. The company illustrated its activities to develop cycles for BGA assembly. The photonic soldering process reportedly provides fewer voids in SAC alloy joints than conventional thermal processes.

IO-Tech, winner of recent innovation awards at Productronica and Lopec, introduced its unique patented laser system for application of precisely and rapidly depositing type 6 solder spots with resolution of 100 $\mu$ m in diameter and 25 $\mu$ m (or finer) pitch – faster than dispensing 2,000 droplets. I predict fabricators will be challenged to make substrates that take full advantage of this system's capabilities! Die bonding is another potential application for this system, as deposits are extremely flat. (Roughness is <5 $\mu$ m.) It can print on components for multiple chip stack applications. And, for this application, the



The author (right) greets attendees following his keynote at PCB East in April.

system is said to be faster than dispensing 10,000 droplets.

This is only the beginning of a new age in the design and manufacture of electronic packages. It's difficult to see how the chip shortage problem will be resolved in the near future, as the world's supply chains are experiencing new disruptions due to the conflicts in Europe. It is also too soon to know how or if active components will be part of the future of additively built constructions.

In the interim, we'll continue to see more consolidation. There will be more vertical integration. Partnering and cooperation, perhaps even system or facility sharing, will increase.

Even when supply chain issues are resolved, we still need to build new infrastructures for the new designs promulgated by so many new innovations. Then we will need new standards and new tests to determine quality.

Stay tuned! Better yet, join the parade and march forward with your contributions to the developing world of electronic design, manufacture and packaging.



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# Will US Government Incentives Spur DOMESTIC INVESTMENT?

Fresh off its inaugural meeting, the PCBAA gets legislative good news. What's next for the organization that wants to rebuild US production? **by MIKE BUETOW** 

In early May the Printed Circuit Board Association of America, or PCBAA, held its first annual meeting, at which they shared progress on their overarching goal, which is to advance US domestic production of PCBs and base materials.

Coinciding with that meeting came an announcement from a pair of US legislators that they had introduced a bill to incentivize purchases of domestically produced PCBs, as well as industry investments in factories, equipment, workforce training, and research and development.

The bill, known as the Supporting American Printed Circuit Boards Act of 2022, is said to be modeled on the CHIPS Act of 2021, a much-touted piece of legislation that earmarks more than \$50 billion toward new onshore semiconductor fabrication plants.

Timing is everything, right?

Travis Kelly, president and chief executive of Isola, the materials developer, and chairman of the PCBAA, spoke with PCD&F/CIRCUITS ASSEMBLY in May.

Mike Buetow: Travis, I want to chat about the May meeting, but first, can we get your thoughts on the Supporting American Printed Circuit Boards Act, or what I'm going to call the "Boards Bill?" What in your estimation are the key provisions?

Travis Kelly: That's a great question, Mike. The association is grateful to Representatives Eshoo and Blake for taking on this important issue. As you know, the US PCB industry has shrunk to the point where we only produce 4% of the world's PCBs, down from approximately 26% 20 years ago. This means the semiconductor industry, as well as other microelectronics industries and segments, are reliant on [offshore] PCBs because, as we know, chips don't float. What's important here is the legislation that's been introduced calls for \$3 billion of investments in the fol-



Travis Kelly, president and chief executive, Isola

lowing areas: domestic manufacturing and PCBs, research and development facilities and workforce initiatives, and then also there's tax incentives to companies that purchase domestic PCBs. It's approximately a 25% tax credit for the purchase of American-made PCBs that will help offset – and this is the important part – the cost-differential that has happened because other countries, primarily in Asia, have heavily subsidized other industries, so it's very difficult for some domestic fabricators and other microelectronics suppliers to compete. This levels the playing field.

# MB: So, \$3 billion is about \$3 billion more than has been invested by the federal government in the PCB industry in, oh, about 30 years.

TK: And that's just it. It goes back to the CHIPS Act, too, with the \$52 billion earmarked for that. You and I have talked several times, and the PCBAA continues to educate, advocate and legislate not only government but industry. It is a large and complex ecosystem that we're operating in. Semiconductors get the most focus right now because of supply chain issues and how that relates to vehicles and the long wait for people trying to order cars, but it's much more complex. We don't talk about advanced packaging. We don't talk about the fact

> that, although we can build foundries in the US, we still send those chips back to primarily Asia for packaging, and then you have to embed them on a printed circuit board. Once again, chips don't float. We need people to be conversant on that and work together to figure out the root cause problem that we're trying to solve and the corrective actions we need to implement to make sure we have a sustainable, viable and trusted source of PCBs and the material supplies that go into them.

> MB: That comment about the \$3 billion investment is tongue-in-cheek, of course.

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But in my experience, the US government puts its money where its priorities are, and that it is committing any sum to the printed circuit board industry is a step in the right direction insofar as the recognition of how critical this industry really is.

I want to talk about that 25% tax credit. That really levels the playing field in terms of making costs more comparable to Southeast Asian sources. Do you think that will stick in the final bill?

TK: It's hard to say. Ultimately, we're very pleased this bill was introduced because, at the very least, it's showing momentum. The government is investing into this microelectronics system called a printed circuit board, and there's recognition people are becoming more conversant on the topic. However, let's be realistic. It is an election year. We're going into midterms. It's always hard to gauge Congress's intent to move legislation, so I don't want to opine on what they will do. I think part of the bill will be passed, and what parts will be passed and what won't be passed are very difficult to say going into such a volatile midterm election. It's good Representatives Eshoo and Moore recognize the dire straits our industry is in, and I look at that as a positive. Microelectronics are largely hidden in the shadow of the chip shortage. This [bill] allows us to ensure people viscerally understand it's a lot bigger than just semiconductors. We're optimistic the bill was introduced; it's the national priority that has too long been invisible to anyone outside our industry, so I look at all of this as very positive for the overall industry.

MB: I don't want to politicize this, but it can't hurt that the supply issues Russia is currently experiencing underscore the point on just how important it is to have these supply chains and materials available on short notice.

TK: It seems every time you and I talk there's another issue from around the globe. What's happening in Ukraine and Russia, the rolling blackouts in China relative to Covid-19 and Omicron variants spreading there rapidly ... every time I think there is a glimmer of hope and people see the supply chain is correcting itself, we are back to where we started. We see the supply chain gets tighter because, even though the port in Shanghai is open, it's still not to the efficiency levels it was before the shutdowns. A lot of containers are trapped on ships waiting to get into that port. Typically you won't see the ramifications of that until 60 or 90 days after the blackout. To your point, we're going to continue as a nation to have to make conscious decisions relative to where we are willing to invest, where we are willing to maybe spend a little bit more for that trusted supply chain and resilient supply chain, and these conversations are bipartisan. As a nation we have to make sure we can fulfill the demands of our people to be sure we have what need to be successful.

MB: About that bipartisan support. Anna Eshoo represents a portion of the Silicon Valley, a California district that is heavily invested not just in electronics manufacturing but also in their customers. Blake Moore comes from Odgen, Utah, which is home to some key US defense manufacturing operations. Spartronics has the EMS site there, the former Inovar. And TTM has the board fabrication shop in Logan, less than an hour down the road. Has PCBAA had conversations with Eshoo or Moore, and if so, what is your general sense of their focus on this bill?

TK: That's a great question, and let me answer it by first segueing into the Printed Circuit Board Association of America meeting we had in Washington, DC. It was our inaugural annual meeting, and although it was our first year, we got a lot of consequential things done.

When you and I spoke several months ago, we had five founding members. We've grown the PCBAA to 17 members, and all were represented in Washington.

We had three great speakers. First, we had the Honorable Alan Shaffer, the former deputy undersecretary of defense for acquisitions and sustainment. He brought really good insights into the way the Department of Defense views our industry and how we can best serve the men and women in uniform. That was a fantastic speech. He also had dinner with our members and got into some very candid, transparent discussions relative to the needs of the Department of Defense and Pentagon moving forward.

We also had Dr. Lara Brown of George Washington University, who works at the graduate school of political management. She gave a nice summary of the state of play in Washington and what it means for midterm elections, the different partisan and bipartisan approaches to certain bills that will be passed and that will be introduced.

Finally, to your point, although Congress was in recess, Congressman Blake Moore took the time to talk with our members via live feed from Utah. He spent more than 30 minutes with our team, answering and asking pointed questions. We were all very happy and impressed with how conversant Representative Moore is on the industry. I was pleasantly surprised he understands [the loss in global market share]. The right number is obviously not to bring everything onshore, but it's definitely higher than 4%. He is passionate about the bill that was introduced relative to supporting PCBs, and it really has garnered a lot of bipartisan support, with Moore representing the Republicans and Eshoo representing the Democrats, working hand-in-hand to get this bill introduced. It was a great discussion. From an industry standpoint, when you look at defense spending, and what that means for our microelectronics industry, it is a relatively small portion of the overall sales within the US. As you know, the demand signal is volatile at best; it's high-mix, low-volume, so it's really looking at what can we do to supply certain critical components, as opposed to just looking at defense. What about banking? What about medical? What about critical infrastructure like 5G? Is there a potential way to aggregate that demand signal, so if you're at a domestically located PCB or material supplier, you can actually have some stability with that demand signal, and a demand signal that's big enough where you're willing to invest those capex dollars? Coming out of the meeting, we have a lot of work relative to

how we continue to garner that momentum and get consequential things done into future years.

#### MB: I know building your membership has to be a priority for the coming year, but where does the Boards Bill stand in that priority list, and what else is on that list?

TK: We look at a bunch of things. When you think about all the offshoring that's taken place over the past 20 years, you're not just offshoring the brick and mortar; you're offshoring the technological knowhow. I use examples like signal integrity engineers and the like that's absolutely critical for what we do as an industry.

The focus of the PCBAA is to continue to educate, advocate, and legislate on behalf of the industry. But what does that really mean? Let's look at some of the top critical items we need to really get our voice around. One would be STEM. How do we get the right sciences and mathematics and so forth into the schools to ensure we have the right talent we need to be successful as an industry? On top of that is workforce development. For people out of school, how can we continue to get them up to speed on the nuances of our industry? How can we continue to train and develop that workforce? And ultimately, how do we build out the right infrastructure, the automation of factories? The tax incentive is definitely helpful, but we as an industry have to innovate as well. How can we take costs out of our system, whether it's through value-stream mapping and Kaizens?

The PCBAA's focus now is to protect some of the wins we have because everyone's legislating every year, and we have to [maintain] the wins we have with the National Defense Authorization Act and the Supporting American Printed Circuit Boards Act; our members had their hands in helping form that language. But we as an organization also need to focus on continuing to develop that resilient supply chain. It's more than just, "We need to build more printed circuit boards and have more material suppliers." It's building up the education. It's building up the workforce development, the infrastructure.

It's like eating an elephant. It has to be a bite at a time. If you just try to solve all the problems you want to, it's overwhelming. You can't offshore over 20 years and expect to flip a switch and get it fixed in a year. This is a marathon, not a sprint.

I'm very thankful for the work our complementary organizations are doing – the PCBAA, the USPAE. We are getting a lot more traction, and more people are talking about the PCB and microwave electronics industry. I'm very encouraged with what I've seen over the last 12 months. □

MIKE BUETOW is president of PCEA (pcea.net); mike@pcea.net.

#### Flexperts, continued from pg. 29

regions. Layer five gets etched at the substrate level, and since there are no conductors crossing the transition on the outer layer, the imaging and etching challenges for layer six are eliminated. This can work well and has been successful in very demanding applications.

The final consideration here for flex as an outer layer is whether or not the conductor pattern will get copper-plated during the hole-plating operation. If plated, flexibility will be



FIGURE 2. A design option spreading the flex layers apart, with rigid layers in the middle and flex toward the top and bottom.

impacted. If the layer is selectively (button) plated, then the outer layer will not carry as much current. This is not right or wrong, but something that needs to be considered.

Another option is to spread the flex layers apart, with rigid layers in the middle and flex toward the top and bottom. This is often symmetrical. Sometimes it is done to incorporate certain via structures. Other times it is done to try to create some physical separation between the flexes. Some say this separation eliminates binding of the flex when bent. I'm not sure I buy that argument.

This can be – and is – fabricated regularly but can increase cost somewhat. The manufacturer has to decide when to remove the internal rigid layers from the part during fabrication. In some cases, they may be removed at the innerlayer process, or near the end of the process. Both have pros and cons, but in either case, it impacts cost. This is because the manufacturer has additional operations to remove these materials from the middle of the stack that they do not need to worry about if the flex is at the middle. It can also impact layer registration if there are large openings routed into the internal layers.

When developing a stack-up, start with the flex at the middle, and work your way out, if you can. This provides the lowest cost, shortest cycle time, and most planar construction. When you need to deviate from the center, keep in mind how it might impact board fabrication and subsequent assembly.

# The PRODUCTION SOURCING Approach

Engineers looking to scale up production are victims of their success if they don't have a long-term supply chain plan. **by BRIAN LANEY** 

The situation: Your engineering team is looking to move from idea to production. You reach out to a contract manufacturer. Question: When does it begin to feel like a partnership?

As a business owner or engineer, working with a contract manufacturer can be daunting, particularly if it doesn't have experience sourcing challenging parts in a challenging market. How can we as a community of manufacturers help solve this problem? We must put in the time to clearly identify the challenges, set aside time, and build resources to assist customers in real time – and offer a stratified path to a solution based on the type of client. Sounds easy, right? But don't flinch when it comes to defusing bombs.

Recently, customers have tapped us to bring production to the US from Asia. These customers have been using turnkey, rapid-turn, low-volume solutions and are now looking at scaling production to about 1,000 from less than 100.

They just have one problem: flaws in their designs. Don't get me wrong. Their designs work great and have been tested and retested with evolving firmware and investment as they have progressed through design and prototyping stages. They're now looking for 500 to 1,000 boards. The quantity makes them a victim of their success.

Finding 50 ICs right now can be difficult. Finding 1,000 can be a 56-week lead time bordering on forever. This situation isn't acceptable for early-stage companies or companies rushing to complete designs to fill market needs for their products. It literally can be life or death.

It is our experience many production shops will enable this walk down a dangerous path, not intentionally but because sourcing is not completed in a holistic manner. They are grabbing parts to build the order, not planning for the future. The cost associated with the path I'm proposing is certainly steeper as a manufacturing services provider, but the wins for customers that have previously whistled past the graveyard make them lifelong clients.

The sourcing approach, rather than the cost of the product or service provided by a supplier, is part of supply chain management and emphasizes customized results and strategic partnerships. In addition, emphasis on building meaningful buyersupplier partnerships promotes collaboration, accountability, and innovation throughout the supplier lifecycle. Ultimately, this approach achieves the overall goal of strategic sourcing: to reduce costs while improving the efficiency and reliability of the supply chain. I walk the halls and repeat the same words daily: "Add value at the very first step."

Alert Tech SMT offers a projected purchasing plan with its quotations, highlighting the components that are hard stops for various volumes on the one-year and two-year roadmaps. This isn't usually a warm, fuzzy moment in the quotation presentation. We're talking red lines on BoMs the customer has never seen before. Not because there was never a problem, but because they have not been exposed to the reality of lead times at scale. ("Mouser shows 150 on hand! What is the problem?") Not what we envision for our quote delivery meetings.

The only thing your customer can't afford is out-of-date or incorrect information. Bringing that information to them is step one. Step two is solving the problem. We have been fortunate to be able to point to what our customers are competing with in the market for their components. Broadcom BCM2837B0 or ATmega328P were chips they selected because they were familiar with them on Raspberry Pi or Arduino. Bad news: Their team wasn't the only one with that idea.

The 0603 resistor is much harder to source now than the 0805. Why did they pick that part? It takes a bit more time in the weeds than many shops seem to be used to spending. These customers are smart. They are solid engineers, but they aren't familiar with scaling production. As a community of manufacturers, we are. I suggest putting in the additional work on these BoMs to pull together alternative parts and packages that can be a clean kit much quicker, suggesting proactive purchases and blanket POs to round out the future needs.

For some customers with a full team behind them, this will be enough to set them on a quick path to reposition their BoM. Does this fix the problem for most? Unfortunately, no.

The most common reply is "these are the components our product needs, and we don't have the resources to reengineer



With out-of-stock conditions rampant, new approaches for scaling production are needed.

software and hardware to work in alternate parts." And this is where the road forks.

Some of these customers don't have on-staff engineering to handle these changes and will not be able to scale their builds unless they find those resources. These are typically small customers. I have helped startup customers source consulting engineers on the terrific platform UpWork to help them over this hump. Being on a call with these consulting/contract engineers to explain the problem on behalf of customers can cut down the time to their success, as well as move them along in the business pipeline. It is win-win.

For customers who see the problem for what it is – nonnegotiable in many cases – and have the resources to move quickly, we offer in-house engineering services to ECO design changes and open the alternate parts.

We have repeatedly warned customers against continuing preproduction builds, hoping their component availability will improve before mass production. The best time to pivot was yesterday; the next best time is today. Many of these parts will be in the red for another year at least. If they are successful in their sales and suddenly must scale up, they will potentially make on-the-fly changes to hardware and software to fulfill demand without proper design process and testing. Looking at the problem through the eyes of our customers, but with our experience, getting 1,000 boards and determining they all need rework: That is the worst-case scenario for them, the cold sweat moment when they have to "make it work" because they don't have the resources to scrap that order.

Drop-in replacements aren't always available. If you haven't considered having a firmware engineer in your factory before, investigate the opportunity. We help move our customers past roadblocks that are often much less of a hurdle than they appear at first glance. Often there is greater component availability moving to a smaller on-chip memory or reduced on-chip capabilities from the same semiconductor manufacturer that satisfies the customers' needs and requires less software engineering than expected. Having talented firmware engineers on staff has been key to unlocking doors.

Customers of all sizes are facing business risks around their manufacturing that is unprecedented. The slow slide of manufacturing to foreign markets once looked flawless on planning documents in board rooms around the country. That day is past. The turnkey fast-turnaround board shops will not have the time or economics available to put in the extra effort. The best time to start building value for customers is now.

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# Defluxing of COPPER PILLAR BUMPED Flip-Chips

A case study showed a well-balanced aqueous cleaning agent removed Pb-free, water-soluble tack flux residues better than straight DI water. **by RAVI PARTHASARATHY and UMUT TOSUN** 

Solder bump technology is problematic below 150µm pitch, since it is challenging to manufacture and assemble. As the bump pitch size shrinks, solder bumps have many limitations in the fine-pitch process. Bump printing, plating or bump drops, along with bump pad sizes, are the major constraints; as a result, risk of shorts increases. Today, dies in production have as many as 25,000 bumps per die. It has been predicted this number will increase to 50,000 to 60,000 per die in the next year or two.<sup>1</sup>

Another form of bump gaining more popularity is the copper pillar. These bumps, instead of being spherical in shape, are in the form of a pillar, with various shapes and sizes. The most popular shape is in the form of a cylinder. The pillar shape allows the high ratio of bump height to bump diameter, therefore permitting very tight pitch, even when bump heights are large. Sometimes a solder cap is formed on top of the pillar to help with connectivity with the mating chip.<sup>1</sup> Due to the cylindrical shape and non-collapsing nature of Cu pillar bumps, they can be easily mounted on the fine trace of the laminate. Copper pillars are terminals used to flip-chip IC chips to a substrate in a semiconductor package by thermal compression flip-chip (TCFC) technology. Copper pillars are formed on aluminum electrode pads of an IC chip.

pes and sizes. The most linder. The pillar shape o bump diameter, therewhen bump heights are d on top of the pillar to

applications.<sup>2</sup>

the coming years.<sup>3</sup>

bump metallization (UBM), and higher I/O density. Also, it can be used for extreme fine-pitch-on-silicon package devices down to 40µm for through silicon via (TSV) and chip on chip (CoC). Packages using copper pillar bumps have more intercon-

FIGURE 3 shows a representative picture of miniaturization of

traditional Pb-free and Cu pillar bumps for fine-pitch flip-chip

sented about 25% of the market in 2013, increased to over

50% by 2020, and is projected to make up about 80% of the

flip-chip market by the end of 2024. Copper pillar is likely to

become the most dominant type of flip-chip interconnect in

Copper pillar technology has been well documented to be

The use of copper pillar technology for flip-chip repre-

nects per surface area, resulting in tighter pitch and lower standoff gaps. As standoff gap reduces, flux residues have less

The bump height can vary anywhere from  $5\mu$ m to 100 $\mu$ m and diameter from 10-20 to 100 $\mu$ m and larger. Most pillar bumps now in production are larger than 20 $\mu$ m in height.



FIGURE 1. Copper pillar bump typical structure.



FIGURE 2. SEM image of Cu pillar bumps.



FIGURE 3. Flip-chip bump miniaturization typical data.

area to outgas during reflow. This results in more active residues under the die.

Flux residues can affect reliability in two ways: First, on the solder bump, substrate or die, thin films of flux residue can significantly reduce interfacial adhesion between the flux and the surfaces. Once the underfilled device is stressed by thermal shock, humidity or other factors, the underfill delaminates from the surface, and a gap can be detected using acoustic microscopy; second, fluxes can also affect reliability by physically impeding the flow of underfill material. Flux residue buildup in the gap between bumps or between the die and the substrate can narrow the gap to a point where the underfill cannot flow, or the edges flow faster, encapsulating air and creating a void. To ensure a void-free underfill, homogenous wetting of the underfill must occur on all surfaces. If wetting is not homogenous, voids in the uncured underfill may translate into reliability problems later.<sup>4</sup>

Most copper pillar applications rely on cleaning with deionized (DI) water only for OA flux removal. Numerous studies already conducted suggest water is beginning to reach its cleaning limitation, however, favoring use of aqueous processes.<sup>5, 6, 7</sup> Increased use of Pb-free solder, which typically requires higher soldering temperatures, is one reason. This results in more burned-in fluxes that are much harder to remove as they begin to produce water-insoluble contamination. DI water alone has limited to no ability to solubilize nonionic residues on the board surface.

Second, cleaning water-soluble fluxes, especially under



FIGURE 4. Historical and forecast growth of copper pillar technology within the flip-chip market.



FIGURE 5. Surface tension values.

components, has grown more difficult. In other words, water, with its high surface tension of more than 70 dynes/cm, cannot remove flux residues under bump pitch less than 40µm.

Aqueous is a term that implies the use of aqueous-based chemistry: for example, an application concentration of 15% mixed with DI water. The level of active concentration actually is secondary; however, aqueous implies the addition of aqueous ingredients. Aqueous cleaning agents diluted in deionized water significantly reduce the surface tension, providing better cleaning through lower ionic contamination, which in turn provides higher product reliability. These cleaning agents are pH-neutral to mildly alkaline in nature, having corrosion inhibitors as part of their formulation, exhibiting full compatibility with a variety of metals (Sn, Ag, Cu, Ni, Al, etc.) present on the copper pillar die. Lack of corrosion inhibitors can easily attack these metals, causing galvanic corrosion reactions.

This study explores the impact of flux cleaning using DI water and a well-balanced aqueous cleaning agent on copper pillar bumped flip-chips. The scope is limited to copper-pillar bumped flip-chips having pitch of 150µm. This study enables the authors to determine the wash parameters and conditions required to effectively clean flux residues underneath these components to ensure reliability and functionality of the final product.

Results are verified via analytical test (IC, SEM/EDS and FTIR) and reliability test methods, including thermal cycling, high temperature storage life (HTSL) and moisture sensitivity level 3 (MSL-3) testing.

The outcome of this study can be used as a benchmark for conducting further studies involving bump pitch less than  $15\mu m$  and denser packages, including 2.5-Ds and 3-Ds.

#### Material Specifications

Substrate specification. The substrate used in this study was organic-based with a thickness of 960µm, having a daisy-chain function. The core material was E-679FGR using PSR4000-AUS703 solder resist. The surface finish on the pads was electroless nickel/immersion gold (ENIG).

Wafer specification. An 8" wafer was selected with a base oxide layer composed of plasma-enhanced tetraethyl orthosilicate (PE-TEOS) and TiN/Al-0.5%Cu metal layer composition. The passivation layer was a combination of high-density plasma/plasma-deposited SiN (HDP/ P-SiN), and the metallization selected was TiCu/Cu. The bump material was Cu/Sn-2.5Ag.

Chip specifications. In this study, 10mm x 10mm flipchip with a daisy-chain structure was used. Cu pillar was designed with 150 $\mu$ m bump pitch and a 30 $\mu$ m Cu pillar height. The pad size was 100 $\mu$ m square with the bump size of  $\Phi$ 75 $\mu$ m. There were a total of 3,721 pads/chips.

- Chip size: 10mm x 10mm
- Number of pads: 61 x 61 = 3,721 pads/chips

#### IC CLEANING

- Pad size: 100µm square
- Pitch: 150µm
- Passivation opening: Φ 80μm
- Bump height: Cu 30μm + SnAg 15μm
- Bump size: Φ 75μm

The geometry of the copper pillars used in a test vehicle are shown in (FIGURE 7).

FIGURE 8 shows a cross-section of copper bump.

Flux specification. The flux used in this study was a Japanese Pb-free water-soluble tacky flux, one of the most commonly used materials in semiconductor packaging, including copper pillar bump applications. The staging time between reflow and cleaning at chemical supplier site was 24 hr., representing a worst-case scenario.

Assembly process. The assembly process requires proper optimization of chip placement on the substrate to get an optimized solder profile. For that reason, it was decided to collaborate with Universal Instruments Advanced Process Lab, which has the capability to assemble and perform reliability testing. The die and substrates were sent to the UI lab for assembly. Die placement was performed using a Universal Instruments' FuzionSC platform.

The water-soluble tacky flux was applied using a linear thinfilm applicator (LTFA), which is an on-board dipping process that provides maximum efficiency to facilitate the wetting of the solder bump. The LTFA creates a thin film of flux, solder paste or adhesive. The packages are individually or gang-dipped, thereby applying the necessary amount of material to the appropriate area. It uses a plate about 38µm thick to create a film.

X-ray inspection. Post-placement, inspection was done using x-ray to ensure the bump was aligned properly to the pad.



FIGURE 6. Chip specification.



FIGURE 7. Copper pillar geometry.



FIGURE 8. Cross-section of copper bump.

First article inspection (FAI) was conducted using x-ray prior to chip placement on the remaining lot, and necessary adjustments were made to align the die.

Reflow profile. The package was reflowed using a Pb-free solder profile using a BTU Pyramax 125 10-zone convection reflow oven under nitrogen (less than 200ppm) with a peak temperature of 250°C (FIGURE 9). Several reflow profiles were evaluated until the heating and cooling rate was sufficiently controlled to get an optimum bump profile post-reflow and minimize stress on the reflowed bump. Open bumps can occur on the reflowed side or at the die-to-bump interface due to coefficient of thermal expansion (CTE) mismatch and substrate warpage during reflow.



FIGURE 9. Reflow soldering profile used.





Equipment. A conveyorized spray-in-air inline cleaner was used for this study. FIGURE 10 shows a schematic of the inline cleaning system.





TABLE 1. Test Plan Used in the Study

Cleaning Agent	Concentration (%)	Belt Speed (FPM)	Wash Exposure Time (Min.)	Total Substrates to be Cleaned
DUM /	100	2	2.6 (2 min. 36 sec.)	54
DI Water	100	3	1.73 (1 min. 44 sec.)	54
Cleaning	-	2	2.6 (2 min. 36 sec.)	54
Agent	5	3	1.73 (1 min. 44 sec.)	54
			Total	216

TADLE 2. ITTITLE CIEditer Trocess Farantieler	TABLE	<ol><li>Inline</li></ol>	Cleaner	Process	Parameter
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Wash Stage								
Equipment	Spray-in-Air Conveyorized Inline Cleaner							
Cleaning Agent (Concentration)	Cleaning Agent (5%); Pure Deionized Water (100%)							
Flux Used	Lead-Free Water-Soluble Tacky Flux							
Conveyor Belt Speed	2.0 and 3.0 fpm							
Pre-Wash Pressure (Top/Bottom)	40 PSI / 40 PSI							
Wash Pressure (Top/Bottom)	80 PSI / 60 PSI							
Wash Hurricane Pressure (Top/Bottom)	40 PSI / 40 PSI							
Wash Temperature	150°F / 65.55°C							
Chemical Isolation Pressure (Top/Bottom)	30 PSI / 25 PSI							
Rinsing S	tage							
Rinsing Agent	DI Water							
Rinse Pressure (Top/Bottom)	85 PSI / 60 PSI							
Rinse Hurricane Pressure (Top/Bottom)	40 PSI / 40 PSI							
Rinse Temperature	140°F / 60°C							
Final Rinse Pressure (Top/Bottom)	25 PSI / 25 PSI							
Final Rinse Temperature	Room Temperature							
Drying St	age							
Drying Method	Hot Circulated Air							
Drying Temperature	160 - 220°F							

Cleaning agents. The cleaning agents included:

Pure deionized water at 100% concentration (10 Meg-Ω resistivity).

■ An aqueous-based cleaning agent specifically developed for the removal of Pb-free water-soluble fluxes from various package types, including those under test.

#### Experimental

A total of 216 packages were built for this study.

The process settings in TABLE 2 were used in the inline cleaner.

The cleaning trials were split into two groups to minimize the flux staging time and keep it the same. The first set of 108 substrates were processed and assembled at Universal Instruments and shipped overnight to the cleaning agent supplier to be cleaned with DI water. The second set of remaining 108 substrates were processed and assembled the following day and

shipped overnight to be cleaned with the cleaning agent.

Post-cleaning, all the substrates were shipped immediately back to Universal Instruments for reliability testing. This included thermal cycling, high-temperature storage life (HTSL) and moisture sensitivity level 3 (MSL-3) test. The remaining cleaned substrates were subjected to analytical test (IC, SEM/EDS and FTIR).

**TABLE 3** details the reliability/analytical test performed on the substrates cleaned with both deionized water and the cleaning agent.

In addition, ion chromatography testing was performed on bare substrates (5 in total) and substrates having Pb-free water-soluble tacky flux (5 in total) to determine their cleanliness levels and ionic species.

Post-cleaning, the substrates were underfilled using a liquid epoxy encapsulant specifically formulated for tight bump pitch, and a narrow gap in flip-chip BGA applications was used. The process was carried out using an Nordson Asymtek Axiom X-1020 dispenser configured with an Asymtek DJ-9500 DispenseJet valve for noncontact jetting of precise volumes of fluid in dots, lines and patterns.

TABLE 3. Reliability/Analytical Test Performed<sup>8, 9, 10, 11, 12</sup>

Reliability/ Description/ Analytical Test Reference Document		Deio Water I	nized Process	Deior Water F	nized Process
		2.0 fpm	3.0 fpm	2.0 fpm	3.0 fpm
Thermal cycling with event detection (1000 cycles at - 40°C to 125°C)	JESD22-A104E	15	15	15	15
HTSL (1000 hr. at 150°C)	JESD-22-A-103C	15	15	15	15
MSL-3	IPC test per J-STD-020E	15	15	15	15
Ion Chromatography	IPC-TM-650 Method 2.3.28	5	5	5	5
FTIR	FTIR mapping and spot measurements	2	2	2	2
SEM/EDS	SEM for electron imaging & EDS for elemental analysis	2	2	2	2

#### **Reliability Test Results**

A prerequisite to package reliability testing is moisture preconditioning to classify package MSL class and ensure it survives reliability test post-moisture soak. Packages were subjected to MSL-3 preconditioning at 60°C/30% RH for 192 hr., followed by 3x reflows at 260°C. The reliability tests results are summarized in **TABLE 4**.

SEM/EDS/FTIR analysis. The goal of the analysis is to evaluate the overall cleanliness under the chip component, as well as surface cleanliness of the Au pad. Post-cleaning, the substrate was cracked, and both the chip and test substrate (Au pad) were analyzed using SEM/EDS and FTIR.

SEM/EDS analysis. SEM/EDS analysis was performed using a Zeiss Sigma 300VP and Oxford X-max<sup>N</sup> 80. Over a period of 4.5 hr., the entire substrate surface was scanned at 200x magnification for a total of 667 individual pictures. These pictures were stitched together using Zeiss SmartStitch software. The BSE detector at 1.5kV was used in this study. The BSE detector is typically very sensitive to the presence of organic contaminations/residues (black = organics). It indicates the density of the material. Material with high density looks brighter (e.g., metals), and material with lower density looks darker (e.g., organics like flux residues).

**FIGURE 11** is an example of stitched area of unclean copper pillar substrate (chip backside). The image consists of 300 individual pictures that were stitched together. The dark areas observed indicate the presence of organic flux residues.

**SEM/EDS overall results.** Substrates cleaned with DI water showed the presence of organic residues on both the chip and the Au pad at 2.0 FPM. At an increased belt speed of 3.0 FPM, a significant amount of residues on both the chip and the Au pad were observed. In the case of the cleaning agent, 2.0 FPM did not exhibit any residues, whereas a minor amount of residues was seen on the Au pad at increased belt speed of 3.0 FPM. Overall, substrates cleaned with the cleaning agent showed a minimal amount of residues compared to "unclean" substrates and substrates cleaned with deionized water.

**FTIR analysis.** FTIR analysis was performed using Bruker LUMOS equipment. The spectrometer is equipped with a liquid-nitrogen-cooled detector. The measurements were performed in attenuated total reflection (ATR) mode.

The Au pad surface was scanned with 20 measurement spots (each 125 x 125 $\mu$ m) in ATR mode. Via integration, it was determined the organic signal was in the range of 2980.9 - 2817.2cm<sup>-1</sup>. All the obtained 20 spots were converted into a heat map. The FTIR heat map indicates the intensity of carbon/flux contamination. As a reference, a flux spectrum was used. Red areas indicate high organic contamination, and blue areas indicate low to zero organic contamination. All spectras were corrected for CO<sub>2</sub> (at around 2,400 to 2,200 cm<sup>-1</sup>).

FTIR overall results. Substrates cleaned with DI water at



FIGURE 11. SEM imaging of unclean chip showing presence of organic flux residues.

	Total No.	Reliability/ Analytical Test	Description/		Cleaning Proc	ess - Acceptance	
	of Substrates Tested		Reference Document	DI Water at 2.0 FPM	Cleaning Agent at 2.0 FPM	DI Water at 3.0 FPM	Cleaning Agent at 3.0 FPM
	15	Thermal cycling with event detection (1,000 cycles at -40° to 125°C)	JESD22-A104E	Pass electrical test	Pass electrical test	Fail electrical test	Pass electrical test
	15	HTSL (1,000 hr. at 150°C)	JESD-22-A-103C	Pass electrical/visual	Pass electrical/visual	Failed electrical/visual	Pass electrical/visual
	15	MSL-3	IPC test per J-STD-020E	No delamination observed; no external crack visible under 40x magnification	No delamination observed; no external crack visible under 40x magnification	Delamination observed between underfill/die and underfill/laminate	No delamination observed; no electrical test failure; no external crack visible under 40x magnification
	2	SEM/EDS	SEM for electron imaging and EDS for elemental analysis	Organic residues visible on chip and Au pad	No residues visible on the chip and Au pad	Significant amount of organic residues visible on chip and Au pad	No residues visible on chip; very minor amount observed on Au pad
	2	FTIR	FTIR mapping and spot measurements	Carbon/flux signals visible around bumps and Au pad	No carbon/flux signals visble on bumps and Au pad	Significant amount of carbon/flux signals visible around bumps and Au pad	No carbon/flux signals visible on bumps; very minor residues visible on the Au pad
	5	lon Chromatography	IPC TM-650 Method 2.3.28	Above pass/fail limits	Below pass/fail limits	Above pass/fail limits	Below pass/fail limits

#### TABLE 4. Reliability Test Results

#### IC CLEANING

2.0 FPM exhibited a significant amount of residues on both bumps and Au pad. On the other hand, substrates subjected to the cleaning agent at 3.0 FPM did not exhibit any carbon/ flux signals on the bumps. Very minor residues were observed on the Au pad in the upper right corner.

Overall, substrates cleaned with the cleaning agent showed a significant improvement compared to DI-water-cleaned substrates, even at faster belt speed.

 TABLE 5. SEM Images for Unclean, DI Water and Cleaning Agent

 at 2.0 FPM



 TABLE 6. SEM Images for Unclean, DI Water and Cleaning Agent

 at 3.0 FPM



**Ion chromatography results.** All the test coupons were subjected to ion chromatography analysis per IPC-TM-650, Method 2.3.28. IC analysis used an extraction solution of 10/90 v/v IPA/deionized water.

- All the bare substrates passed, exhibiting low levels of ionic species.
- Uncleaned substrates having Pb-free, water-soluble tacky flux residues showed significantly high levels of cations, anions and weak organic acids.
- DI-water-cleaned packages failed the IC test, exhibiting high levels of formate and chloride ions. At 2.0 FPM, even though substrate #4 passed the IC test, the values for formate ions were very close to pass/fail limits. At 3.0 FPM, significant failures were observed for acetate, formate and chloride ions.

**TABLE 7.** EDS Images for Unclean, DI Water (at 2.0 FPM) and Cleaning Agent (at 3.0 FPM)



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Substrates cleaned with the cleaning agent passed the IC test at both 2.0 and 3.0 FPM, with a majority of the ionic species below the pass/fail limits.

#### Conclusions

This comparative study confirmed the deionized water inline cleaning system is challenged to consistently and effectively clean flux residues underneath low-stand-off components, especially when it comes to cleaning under copper pillar packages with  $150\mu m$  bump pitch and  $30\mu m$  Cu pillar height.

The DI-water-cleaned substrates at 3.0 FPM failed the thermal cycling, HTSL and MSL-3 test. Moreover, substrates cleaned with DI water exhibited the presence of carbon contamination on the chip backside and the Au pad via SEM/EDS/FTIR analysis, as well as high levels of ionic species when subjected to IC testing.

In comparison, substrates subjected to the cleaning agent passed the thermal cycling, HTSL and MSL-3 test. These packages showed better cleaning performance under chip



FIGURE 12. Example of FTIR heat map generation.

TABLE 8. FTIR Results for Unclean, DI Water (at 2.0 FPM) and Cleaning Agent (at 3.0 FPM)



#### TABLE 9. Ion Chromatography Results - Bare Substrates

		Pass/	Bare Substrates					
	Ionic Species	Limit	#1	#2	#3	#4	#5	
	Fluoride (F <sup>-</sup> )	1	0.242	0.332	0.271	0.032	0.032	
	Acetate ( $C_2H_3O_2^{-}$ )	3	ND	ND	ND	ND	ND	
	Formate (CHO <sub>2</sub> <sup>-</sup> )	1	0	0.226	ND	0.109	0.153	
	Chloride (Cl-)	1	0	0.104	0	0.104	0.104	
su	Nitrite (NO <sub>2</sub> -)	2	0.332	0.052	0.219	0.187	0.154	
Anio	Bromide (Br <sup>-</sup> )	6	0	0	0	0	0	
	Nitrate (NO3-)	2	ND	0.106	0.009	ND	0.06	
	Phosphate (PO42-)	2	ND	ND	ND	ND	ND	
	Sulfate (SO <sub>4</sub> <sup>2-</sup> )	1	0	0	0	0	0	
	WOA (Weak Organic Acid)	25	1.554	1.58	1.215	0.98	1.754	
	Lithium (Li+)	1	ND	ND	ND	ND	ND	
	Sodium (Na+)	2	0.082	0.05	0.065	0.05	0.046	
suo	Ammonium (NH <sub>4</sub> <sup>+</sup> )	2.5	0	0	0	0	0	
Cati	Potassium (K <sup>+</sup> )	2	0.018	0.0009	0.0008	0.0012	0.0007	
	Magnesium (Mg <sup>2+</sup> )	n/a	0	0	0	0	0	
	Calcium (Ca <sup>2+</sup> )	n/a	0	0	0	0	0	
lo	n Chromatography Test F	Results	Pass	Pass	Pass	Pass	Pass	
NE	ND – Not detected. 0 – Blank value is higher than sample value. All values in µg/in <sup>2</sup> .							

TABLE 11. Ion Chromatography Results - Substrates Cleaned with DI Water at 2.0 FPM

	Pass/ DI-Water Cleaned Substrates (at 2.0 FPM)							
	Ionic Species	Fail Limit	#1	#2	#3	#4	#5	
	Fluoride (F <sup>-</sup> )	3	ND	ND	ND	ND	ND	
	Acetate ( $C_2H_3O_2^{-}$ )	3	2.6703	2.459	2.7654	2.8431	2.3789	
	Formate (CHO <sub>2</sub> <sup>-</sup> )	3	3.9452	3.821	3.206	2.985	3.532	
	Chloride (Cl <sup>-</sup> )	3	3.2659	3.1456	2.9591	2.8831	3.1456	
su	Nitrite (NO <sub>2</sub> <sup>-</sup> )	3	ND	ND	ND	ND	ND	
Anic	Bromide (Br)	6	2.1469	2.5631	2.6701	2.1478	2.1097	
	Nitrate (NO3-)	3	1.156	1.243	1.742	1.291	1.295	
	Phosphate (PO42-)	3	ND	ND	ND	ND	ND	
	Sulfate (SO <sub>4</sub> <sup>2-</sup> )	3	ND	ND	ND	ND	ND	
	WOA (Weak Organic Acid)	25	6.5421	6.7439	5.7612	5.9863	5.1874	
	Lithium (Li+)	3	ND	ND	ND	ND	ND	
	Sodium (Na+)	3	1.3464	1.2984	1.9754	1.1321	1.0743	
suo	Ammonium (NH <sub>4</sub> +)	3	2.9865	2.0972	2.5632	2.6821	2.1876	
Cati	Potassium (K <sup>+</sup> )	3	ND	ND	0.1987	ND	ND	
	Magnesium (Mg <sup>2+</sup> )	n/a	0.5421	0.6784	0.7543	0.5312	0.6409	
	Calcium (Ca <sup>2+</sup> )	n/a	ND	0.1324	0.1679	0.1954	0.1076	
lo	n Chromatography Test F	Results	Fail	Fail	Fail	Pass	Fail	
NE	ND – Not detected. 0 – Blank value is higher than sample value. All values in µg/in <sup>2</sup> .							

TABLE 10. Ion Chromatography Results – Unclean Substrates Having LF Water-soluble Tacky Flux Residues

	Ionic Species	Unclean substrates having lead-free water-soluble tacky flux							
		#1	#2	#3	#4	#5			
	Fluoride (F <sup>-</sup> )	ND	ND	ND	ND	ND			
	Acetate ( $C_2H_3O_2^{-}$ )	ND	ND	ND	ND	ND			
	Formate (CHO <sub>2</sub> <sup>-</sup> )	55.6747	47.549	49.0945	43.2678	41.6709			
	Chloride (Cl <sup>-</sup> )	51.514	46.3214	48.439	42.478	48.321			
SU	Nitrite (NO <sub>2</sub> <sup>-</sup> )	ND	ND	ND	ND	ND			
Anio	Bromide (Br)	7.746	6.431	7.236	6.8903	7.7835			
	Nitrate (NO <sub>3</sub> <sup>-</sup> )	9.3004	8.6709	9.321	8.459	8.539			
	Phosphate (PO <sub>4</sub> <sup>2-</sup> )	ND	ND	ND	ND	ND			
	Sulfate (SO <sub>4</sub> <sup>2-</sup> )	6.5516	5.551	5.987	6.231	6.451			
	WOA (Weak Organic Acid)	37.5647	41.891	30.235	30.456	35.467			
	Lithium (Li <sup>+</sup> )	ND	ND	ND	ND	ND			
	Sodium (Na+)	8.3673	8.41	8.561	8.341	8.465			
suo	Ammonium (NH <sub>4</sub> <sup>+</sup> )	6.7807	5.234	6.412	5.124	5.987			
Cati	Potassium (K <sup>+</sup> )	4.4984	3.973	4.245	4.219	4.875			
	Magnesium (Mg <sup>2+</sup> )	7.2435	7.2435	7.2435	7.2435	7.2435			
	Calcium (Ca <sup>2+</sup> )	6.1741	6.1741	6.1741	6.1741	6.1741			

ND – Not detected. 0 – Blank value is higher than sample value. All values in  $\mu$ g/in<sup>2</sup>.

TABLE 12. Ion Chromatography Results – Substrates Cleane	d with
DI Water at 3.0 FPM	

	Devid and a second s									
	ates (at 3.0	D FPM)								
	ionio openico	Limit	#1	#2	#3	#4	#5			
	Fluoride (F <sup>-</sup> )	3	ND	ND	ND	ND	ND			
	Acetate $(C_2H_3O_2^{-})$	3	2.872	2.946	3.21	2.976	3.147			
	Formate (CHO <sub>2</sub> <sup>-</sup> )	3	4.762	5.132	4.8762	4.952	5.184			
	Chloride (Cl <sup>-</sup> )	3	5.487	5.943	6.726	5.743	6.871			
suo	Nitrite (NO <sub>2</sub> <sup>-</sup> )	3	ND	ND	ND	ND	ND			
Anio	Bromide (Br <sup>-</sup> )	6	4.3298	4.5048	4.6254	5.3728	4.974			
	Nitrate (NO <sub>3</sub> -)	3	1.8663	1.6735	1.5463	1.7934	1.972			
	Phosphate (PO <sub>4</sub> <sup>2-</sup> )	3	ND	ND	ND	ND	ND			
	Sulfate (SO <sub>4</sub> <sup>2-</sup> )	3	ND	ND	ND	ND	ND			
	WOA (Weak Organic Acid)	25	13.834	16.621	15.419	16.423	15.854			
	Lithium (Li+)	3	ND	ND	ND	ND	ND			
	Sodium (Na+)	3	1.7542	1.542	1.873	1.851	1.914			
ons	Ammonium (NH <sub>4</sub> <sup>+</sup> )	3	2.103	1.963	2.864	2.5492	2.365			
Cati	Potassium (K <sup>+</sup> )	3	ND	0.354	ND	ND	ND			
	Magnesium (Mg <sup>2+</sup> )	n/a	0.8508	0.6273	0.6904	1.8144	0.942			
	Calcium (Ca <sup>2+</sup> )	n/a	ND	0.1333	0.1342	0.2016	0.1754			
lor	n Chromatography Test R	esults	Fail	Fail	Fail	Fail	Fail			
ND	ND – Not detected $\Omega$ – Riank value is higher than sample value. All values in $\mu \sigma lin^2$									

component, as well as on the investigated Au pad. Very minor residue was visible when subjected to SEM/EDS/FTIR analysis. IC testing also showed very low levels of ionic species.

Based on the overall study conducted, it is observed the cleaning agent at low concentration (5%) may completely remove the Pb-free, water-soluble tacky flux residues at faster belt speed (3.0 FPM) compared to straight DI water at 2.0 FPM, which would also enable an increase in throughput of 50%.

It should be noted the copper pillar flip-chip substrates were cleaned 24 hr. after the assembly and soldering process. Generally, its recommended to clean the water-soluble tacky flux as soon as possible (preferably within an hour post-soldering).

#### Acknowledgments

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 TABLE 13. Ion Chromatography Results – Substrates Cleaned with

 Cleaning Agent at 2.0 FPM

Pass/ Substrates Cleaned with Ionic Species Fail Cleaning Agent at 2.0 FPM								
		Limit	#1	#2	#3	#4	#5	
	Fluoride (F <sup>-</sup> )	3	ND	ND	ND	0	0	
	Acetate ( $C_2H_3O_2^{-}$ )	3	ND	ND	ND	ND	ND	
	Formate (CHO <sub>2</sub> <sup>-</sup> )	3	ND	ND	ND	0.284	0.158	
	Chloride (Cl <sup>-</sup> )	3	0.4297	0.0222	0.2653	0.766	0.11	
suo	Nitrite (NO <sub>2</sub> -)	3	ND	ND	ND	0.044	0.04	
Anic	Bromide (Br <sup>-</sup> )	6	0	0.3709	0.2745	0.142	0.162	
	Nitrate (NO3-)	3	0.2172	0	0	0	0	
	Phosphate (P0 <sub>4</sub> <sup>2-</sup> )	3	ND	ND	ND	ND	ND	
	Sulfate (SO <sub>4</sub> <sup>2-</sup> )	3	ND	ND	ND	ND	ND	
	WOA (Weak Organic Acid)	25	ND	ND	ND	0.768	0.788	
	Lithium (Li+)	3	ND	ND	ND	0	0.002	
	Sodium (Na <sup>+</sup> )	3	0	0	0	1.216	0.32	
SUO	Ammonium (NH <sub>4</sub> +)	3	ND	ND	ND	ND	ND	
Cati	Potassium (K+)	3	2.406	0.0033	0.002	0.028	0	
	Magnesium (Mg <sup>2+</sup> )	n/a	0	0	0	0.114	0.016	
	Calcium (Ca <sup>2+</sup> )	n/a	0	0	0	0.568	0.688	
loi	Ion Chromatography Test Results Pass Pass Pass Pass Pass							
NE	$ND-Not$ detected. 0 – Blank value is higher than sample value. All values in $\mu g/in^2\!.$							

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	Ionic Species	Pass/ Fail	Substrates Cleaned with Cleaning Agent at 3.0 FPM						
		Limit	#1	#2	#3	#4	#5		
	Fluoride (F <sup>-</sup> )	3	ND	ND	ND	ND	ND		
	Acetate ( $C_2H_3O_2^{-}$ )	3	0.9643	0.659	0.5612	0.6214	0.7215		
	Formate (CHO <sub>2</sub> <sup>-</sup> )	3	ND	ND	ND	ND	ND		
	Chloride (Cl <sup>-</sup> )	3	0.4678	0.3901	0.6109	0.6213	0.4931		
SU	Nitrite (NO <sub>2</sub> -)	3	ND	ND	ND	ND	ND		
Anio	Bromide (Br <sup>-</sup> )	6	0.2643	0.3387	0.239	0.2104	0.1612		
	Nitrate (NO <sub>3</sub> -)	3	ND	ND	ND	ND	ND		
	Phosphate (PO4 <sup>2-</sup> )	3	ND	ND	ND	ND	ND		
	Sulfate (SO <sub>4</sub> <sup>2-</sup> )	3	ND	ND	ND	ND	ND		
	WOA (Weak Organic Acid)	25	0.54	0.964	0.684	0.556	0.398		
	Lithium (Li+)	3	ND	ND	ND	ND	ND		
	Sodium (Na <sup>+</sup> )	3	0.2807	0.3134	0.2964	0.2607	0.2176		
SUO	Ammonium $(NH_4^+)$	3	0.1284	0.0875	0.1119	0	0.024		
Cati	Potassium (K+)	3	ND	ND	ND	ND	ND		
	Magnesium (Mg <sup>2+</sup> )	n/a	ND	0.1908	ND	ND	ND		
	Calcium (Ca <sup>2+</sup> )	n/a	ND	ND	ND	ND	ND		
lor	n Chromatography Test F	lesults	Pass	Pass	Pass	Pass	Pass		
ND	ND – Not detected. 0 – Blank value is higher than sample value. All values in $\mu$ g/in <sup>2</sup> .								

### TABLE 14. Ion Chromatography Results – Substrates Cleaned with Cleaning Agent at 3.0 FPM

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### State-of-the-Art Technology Flashes

Updates in silicon and electronics technology.

Ed.: This is a special feature courtesy of Binghamton University.

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The INTEGRATED **ELECTRONICS** ENGINEERING **CENTER (IEEC)** at Binghamton University is a New York Center of Advanced Technology (CAT) responsible for the advancement of electronics packaging. Its mission is to provide research into electronics packaging to enhance our partners' products, improve reliability and understand why parts fail. Research thrusts are in 2.5/3-D packaging, automotive and harsh environments. bioelectronics, flexible and additive electronics. materials for packaging and energy storage, MEMS, photonics, power electronics. sensors, embedded electronics, and thermal challenges in electronic packaging. More information is available at binghamton.edu/ieec.

This ink is alive and made entirely of microbes. Northeastern University researchers have created a bacterial ink that reproduces itself and can be 3-D-printed into living architecture. The microbial ink flows like toothpaste under pressure and can be 3-D-printed into various tiny shapes, a circle, a square and a cone, all of which hold their form and glisten like Jell-O. This new substance is not the first-ever living ink. Scientists have previously created printable gels that were cocktails of bacteria and polymers that helped provide structure when printed. One such ink contained hyaluronic acid, a seaweed extract and fumed silica. (*IEEC file #12578, The NY Times, 11/24/21*)



Nanowires under tension create the basis for ultrafast transistors. Smaller chips, faster computers, less energy consumption. The faster electrons can accelerate in these tiny wires, the faster a transistor can switch and the less energy it requires. Dresden researchers have succeeded in experimentally demonstrating electron mobility in nanowires is remarkably enhanced when the shell places the wire core under tensile strain. They produced nanowires consisting of a gallium arsenide core and an indium aluminum arsenide shell. This phenomenon offers novel opportunities for the development of ultrafast transistors. Nanowires have a unique property: These ultra-thin wires can sustain very high elastic strains without damaging the crystal structure of the material. (IEEC file #12664, Science Daily, 2/7/22)

Rechargeable battery is one long filament, and you can cut it as needed. MIT researchers have developed a rechargeable Li-ion battery that's fabricated as a continuous fiber using a standard fiberdrawing system and novel battery gels. A key attribute is the battery can be cut anywhere along its length and still function without leakage of contents. As tangible demonstration of the absence of limitation on length, they drew a battery filament over 140 meters long; this fiber battery had discharge capacity of about 123mAh and discharge energy of 217mWh. Incorporating a filament power source into the structure of end products could lower their overall weight, enable new packaging arrangements, and permit customization of the battery's physical features. *(IEEC file #12659, Electronic Design, 1/21/22)* 



New efficiency record for solar cell technology. National University of Singapore researchers have set a record of 23.6% in the power conversion efficiency of solar cells made using perovskite and organic materials. This technological breakthrough paves the way for flexible, lightweight, low-cost and ultrathin photovoltaic cells, which are ideal for powering vehicles, boats, blinds and other applications. To raise the power conversion efficiency of solar cells to go beyond 30%, stacks of two or more absorber layers are required. Tandem solar cells, which are made using two different types of photovoltaic materials, are a hot area of research. Their discovery opens the door to thin-film tandem solar cells that are light and bendable, which has wide-ranging applications for solarpowered blinds, vehicles, boats and other devices. (IEEC file #12643, Science Daily 12/21/21)

A transistor for sound points toward whole new electronics. Potential future transistors that consume far less energy than current devices may rely on exotic materials called "topological insulators," in which electricity flows across only surfaces and edges with virtually no dissipation of energy. Harvard University researchers have invented and simulated the first acoustic topological transistors, which operate with sound waves instead of electrons. Topology is the branch of mathematics that explores the nature of shapes independent of deformation. By using acoustic topological insulators, in which sound waves can experience topological protection, scientists were able to sidestep this complexity to create *acoustic* topological transistors. *(IEEC file #12661, IEEE Spectrum, 1/31/22)* 



Groundbreaking research produces record levels of strain in single-crystal silicon. University of Surrey researchers have developed a single-step procedure to put single-crystal silicon under more strain than ever achieved. The discovery could be crucial to the future development of silicon photonics, which underpins the technologies behind the internet of things, and is currently constrained by the lack of cheap, efficient, and easily integrated optical emitters. The researchers are transferring the same procedure to germanium. If successful, they will open the door to creating germanium lasers, which are compatible with silicon-based computers, and could revolutionize communications systems by means of new optoelectronic devices. This would address the problem of overheating and would eliminate the need to develop expensive and difficult-to-integrate III-V devices, a popular area of research to try to overcome overheating. (IEEC file #12641, Nanowerk, 12/8/21)

Samsung claims first with in-memory MRAM. Samsung announced an MRAM innovation, claiming the world's first in-memory computing based on MRAM capable of performing both data storage and data computing within a single memory network. The MRAR array chip is the next step to realizing low-power AI chips. Use of in-memory computing architectures has increased over the years because of its abil-



ity to crunch data at the edge, which can in turn reduce the amount of data movement and network latency. Samsung's focus on in-memory computing stems from MRAR's low-resistant nature, which ordinarily limits its ability to reduce power consumption. The MRAR array chip eliminates this issue with what it calls "resistance sum" in-memory computing architecture. *(IEEC file #12638, EE Times, 1/13/22)* 

Harnessing noise in optical computing for Al. University of Washington researchers have developed new optical computing hardware for AI and machine learning that is faster and much more energy-efficient than conventional electronics. The research also addresses another challenge: the "noise" inherent to optical computing that can interfere with computing precision. The team demonstrated an optical computing system for AI and machine learning that not only mitigates this noise but uses some of it as input to help enhance the creative output of the artificial neural network within the system. They built an optical computer that is faster than a conventional digital computer. Also, this optical computer can create new things based on random inputs generated from the optical noise that most researchers tried to evade. (*IEEC file #12645, Semiconductor Digest, 12/24/21*)

Sensor could make 3-D holograms a feature in mobile devices. Korea Institute of Science and Technology (KIST) and Yonsei University researchers are laying the groundwork for 3-D digital holography on mobile devices. The group designed a photodiode that detects the polarization of light in the near-infrared region without the need for additional filters. Using this device, the researchers demonstrated miniaturized holographic image sensors for 3-D digital holograms. (*IEEC file #12644, Photonics Media, 12/20/21*)



'Intelligent sensor processing unit' integrates brains into sensors. STMicroelectronics announced the launch of the intelligent sensor processing unit (ISPU) that combines a digital signal processor (DSP) suited to run AI algorithms and a MEMS sensor on the same silicon. In addition to reducing size over system-in-package devices and cutting power by up to 80%, merging sensor and AI puts electronic decisionmaking in the application Edge. In the Onlife Era, innovative products enabled by smart sensors are able to sense, process and take actions, bringing the fusion of technology and the physical world. The proprietary ultra-low-power DSP can be programmed in C. It also permits quantized AI sensors to support full- to single-bit precision neural networks. This ensures superior accuracy and efficiency in tasks such as activity recognition and anomaly detection by analyzing inertial data. (*IEEC file* #12681, *Semiconductor Digest*, 2/18/22)

#### Market Trends

Alice all-electric aircraft prepares to fly. The world's first all-electric passenger aircraft is preparing to take flight. The Alice, a plane developed by Israeli company Eviation, went through engine testing. A prototype of the aircraft has been going through low-speed taxi tests since December and will attempt a high-speed taxi test next. Eviation is working with Honeywell (flight-by-wire systems), Siemens (EPUs), Hartzell (propellers), and magniX (EPUs). The aircraft is targeting "middle mile" commuter routes. Eviation claims the airplane can fly up to nine passengers at 240 knots at a range of up to 650 miles. (*IEEC file #12672, Military & Aerospace Electronics, 2/1/22*)



Automotive sensors market to reach \$55 billion by 2030. Global Market Insights predicts the automotive sensors market size will exceed \$55 billion by 2030. Sensors of various types, including LiDAR, pressure, temperature and image, play a key role in these safety solutions, owing to their ability to offer higher accuracy and faster response rates in the event of accidents or crashes. Additionally, many regulatory bodies are issuing mandates that require auto manufacturers to equip their new vehicle models with passive safety systems, which could augment demand for automotive sensor technology. The automotive sensors market from the radar sensor segment is likely to depict a CAGR of 10% through 2030, owing to burgeoning autonomy and the use of ADAS in modern vehicles. *(IEEC file #12674, Semiconductor Digest, 2/3/22)* 

**Quantum update: a \$490 million market.** The global quantum computing market was worth \$490 million last year and is expected to expand 21.9% annually through 2024, according to a new study from Hyperion Research. The report also notes software, middleware and applications are growing to account for a bigger share of the market value than hardware. In the few years after 2024, several companies are expecting to be able to demonstrate quantum advantage: the ability for a quantum computer to process a real-world problem faster

than a classical computer. (IEEC file #12675, Fierce Electronics, 2/7/22)



Integrated Roadways sees a smart pavement future for infrastructure backlog. Integrated Roadways sees the future of infrastructure in precast concrete roadway panels that incorporate digital tech and fiberoptics. The panels will be used to support wireless charging for electric vehicles and fast wireless data communications for autonomous vehicles, among other capabilities. These panels can incorporate sensors and networking gear to support connected and autonomous EVs but also to support networks for municipal use in traffic control and other functions. They are designed to be softwareupgradeable panels, similar to how modern vehicles and smartphones can be upgraded over the air. (*IEEC file #12676, Fierce Electronics, 2/8/22*)



Four important Wi-Fi design trends worth watching in 2022. The number of Wi-Fi devices in use will reach nearly 18 billion in 2022. The network of companies that manages the Wi-Fi design ecosystem also forecasts 4.4 billion devices to be shipped this year. Wi-Fi, now widely acknowledged as a foundation technology for the IoT applications, is reinforcing its position with Wi-Fi 6 and Wi-Fi 6E, which employ orthogonal frequency division multiple access (OFDMA) to improve performance in dense environments. Then, there is target wake time (TWT) technology, which reduces battery consumption and makes Wi-Fi a suitable choice for sensor-based devices. Wi-Fi Alliance has listed four major trends as Wi-Fi: an IoT

building block; Wi-Fi 6 and Wi-Fi 6E in homes and enterprises; automated frequency coordination (AFC); and Wi-Fi network optimization. *(IEEC file #12655, EDN, 1/24/22)* 

New Panasonic battery extends Tesla S range to 750km. Next year Panasonic plans to start mass production of a battery that will give a Tesla Model S a range of 750km, up from 650km at the moment. The new battery will have five times the capacity of the previous battery and will be twice as big and, costed on a capacity basis, will be 10-20% cheaper. Mercedes' EQS currently has a range of 770km but is planning a car with a range of 1000km using a battery from CATL of China. (*IEEC file #12656, Electronics Weekly, 1/25/22*)



Electrically conductive adhesives: the new solders. Electrically conductive adhesives (ECAs) claim to possess many superior properties than traditional solders. With an increasing demand for electronic goods, this decade may see ECAs gradually establish themselves as the new solder. Proper placement of electronic components such as ICs and LEDs on substrates is the crux of developing an operational circuit board for an electronic device. While conventional lead-free solder excels at its task for rigid PCBs, it is not well suited for emerging applications that require components to be attached to flexible substrates or conformal surfaces. The alternative ECA not only has high strength but is quite safe as well. ECA comes in two types: isotropic conductive adhesive (ICA) and anisotropic conductive adhesives (ACA), which correspond to different ways of conducting electricity across a joint. ACA is further divided into anisotropic conductive paste (ACP) and anisotropic conductive film (ACF). (IEEC file #12651, Electronics for You, 1/12/22)



#### **Recent Patents**

Novel 3-D NAND memory device (assignee: Yangtze Memory) pub. no. EP3915147. A semiconductor device is provided. The semiconductor device includes a first substrate that has a first side for forming memory cells and a second side that is opposite of the first side. The semiconductor device also includes a doped region and a first connection structure. The doped region is formed in the first side of the first substrate and is electrically coupled to at least a source terminal of a transistor (e.g., a source terminal of an end transistor of multiple transistors that are connected in a series). The first substrate and coupled to the doped region through a first via. The first via extends from the second side of the first substrate to the doped region.

Semiconductor package having a spacer with a junction cooling pipe (assignee: Semiconductor Components Ind.) patent no. 16/790,933. Implementations of semiconductor packages may include a first substrate coupled to a first die, a second substrate coupled to a second die, and a spacer included within a perimeter of the first substrate and within a perimeter of a second substrate, the spacer coupled between the first die and the second die. The spacer includes a junction cooling pipe therethrough.

Fabrication of a microfluidic chip package or assembly with separable chips (assignee: IBM Corp.) patent no. 11,198,119. The present invention is notably directed to methods of fabrication of a microfluidic chip package or assembly, comprising a substrate having at least one block comprising one or more microfluidic structures on a face of the substrate; partially cutting into the substrate to obtain partial cuts, such that a residual thickness of the substrate at the level of the partial cuts enables singulation of said at least one block; cleaning and applying a cover film to cover said at least one block, whereby at least one covered block is obtained, the applied cover film still enabling singulation of each covered block, where each block corresponds to a microfluidic chip after singulation.

Packaged die for bumpless buildup layer (BBUL) packages (assignee: Intel Corp.) pub. no. US11201128. A packaged semiconductor die with a bumpless die package interface and methods of fabrication are described. A semiconductor package includes a substrate having a land side with a lowermost layer of conductive vias. A die is embedded in the substrate and has an uppermost layer of conductive lines, one of which is coupled directly to a conductive via of the lowermost layer of conductive vias of the substrate. In another example, a semiconductor package includes a substrate having a land side with a lowermost layer of conductive vias. A semiconductor die is embedded in the substrate and has an uppermost layer of conductive lines with a layer of conductive vias disposed thereon. At least one of the conductive lines is coupled directly to a conductive via of the semiconductor die. Chip-on-film package (assignee: Novatek Microelectronics Corp.) patent no. 11189597. A chip-on-film package, including a flexible film, a first patterned circuit layer, one or more first chips, a second patterned circuit layer, and one or more second chips. The flexible film includes a first surface and a second surface opposite to the first surface. The first patterned circuit layer is disposed on the first surface. The one or more first chips are mounted on the first surface and electrically connected to the first patterned circuit layer. The second patterned circuit layer is disposed on the second surface. The one or more second chips are mounted on the second surface and electrically connected to the second patterned circuit layer.

PCB mesh routing to reduce solder ball joint failure during reflow (assignee: Microsoft Technology Licensing) patent no. 11,212,912. Voids are introduced in a copper shape to reduce warpage experienced by a printed circuit board during a reflow process. Copper shapes on an outer layer of a PCB may be used to connect large packages that include ball grid arrays to the board. The copper shapes may induce warpage in the board during reflow. Routing a mesh pattern of voids in the copper shapes may reduce solder ball joint cracking and pad cratering during reflow and make solder joints more reliable. The voids may make the copper shapes less ridged and change the copper heat dissipation profile to remove sharp warpage forces that cause solder joints to experience pad cratering. The voids may be 8-mil times 8-mil cuts or indentations in the copper shape.

Adaptive vertical wiring method and stacked semiconductor package (assignee: Powertech Technology) patent no. TW202044434. The present invention relates to an adaptive vertical wiring method, a stacked semiconductor packaging method and a stacked semiconductor package. In the adaptive vertical wiring method, the end point of each vertical wire is determined according to a plurality of position patterns on a carrier, and a real position of each pad on a chip is obtained to determine the start point of the vertical wire. A wiring path of the vertical wire is calculated according to the end point and the start point. Therefore, even if any chip is displaced during stacking, and the pads thereon are shifted, the vertical wire is accurately connected to the shifted pad and corresponding inner pad on an outer wiring layer.



**PRINTED CIRCUIT DESIGN & FAB / CIRCUITS ASSEMBLY** 

MACHINES

MATERIALS

TOOLS SYSTEMS

SOFTWARE

# **SHELF**

#### ALTAIR SIMULATION 2022 SOFTWARE

Simulation 2022 software helps simulate antennas and broadens toolset for advanced driver-assistance systems applications. Supports automation of 5G envelope beam patterns and includes hybrid ray-tracing patterns and rotating doppler effects for ray-based solvers. Can better simulate full-wave antenna and array characterizations to analyze wireless systems. Improved ADAS tools consider sensor types like ultrasound. Has frequency-modulated continuouswave radar simulations that target ADAS applications. Includes updates for AEC. Altair Units-accessible capabilities include S-FRAME software, as well as SimSolid rapid analysis, HyperWorks advanced meshing, and computational fluid dynamics wind load simulations. S-CONCRETE, S-FRAME and S-FOUN-DATION include built-in design codes for different American, Canadian, European and Asian/Oceanian nations. S-TIMBER addresses sustainable buildings and structures; includes analysis capabilities and can simulate structural response to seismic loading according to NBCC, ASCE and IB codes. Provides enhanced control over panel modeling to design CLT, Glulam and Sawn lumber elements for code compliance. PollEx features expanded design verification, signal integrity and PCB modeling functionalities. Includes cross-probe verification like DFx Excel results and direct ECAD link to Pulsonix and Altium Designer. Altair SimLab includes application functionalities like drop test, multiphysics analysis for PCBs, and thermal management simulation that can cover entire systems. Introduces PSIM, which can handle simulation and design for power supplies, motor drives, control systems and microgrids.

#### Altair

#### altair.com/simulation-2022

#### ELECTRONINKS CIRCUITSEED FILM

CircuitSeed thin, dense film is used as 3-D, finely patterned seed layers for subsequent metallization by plating. Reduces 20-plus-step process to a few steps. Reportedly uses at least 40x less water and substantially less energy. Supports multiple chemistries that can be printed via variety of techniques as dense, finely patterned seed layers on surfaces ranging from rigid to flexible plastics and 3-D.

#### Electroninks

electroninks.com

#### ELECTRONINKS CIRCUITSHIELD INK

CircuitShield ink is for EMI shielding and backend semiconductor metallization. Powers technology that produces smartphones with 5G capabilities. Reportedly eliminates spray nozzle clogging and residue in silver film, and provides high shielding effectiveness. Has long shelflife and excellent printing stability at room conditions. Is used for five-sided SiP shielding with aspect ratio from top to side wall close to one. Other use cases involve wafer metallization and conformal via coating.

#### Electroninks



#### HERAEUS CONDURA.ULTRA AMB SUBSTRATE

Condura.ultra Ag-free AMB substrate enables bonding silicon-nitride-based ceramics with copper foils. Enables highperformance Si3N4 substrates using Ag-free active metal brazing bonding technology. Designed to offer outstanding reliability and processing for sintering, bonding and soldering. Comes with standard and thick Cu layers. Thermal conductivity is ≥60W/m.K and ≥80W/m.K.

#### Heraeus Electronics

heraeus-electronics.com



#### HITACHI FT230 XRF ANALYZER

FT230 XRF analyzer speeds up analysis to help achieve 100% inspection and meet tightening specifications. Includes intelligent part recognition feature Find My Part; automatically selects features that need to be measured, analytical routines and reporting rules. On-board, user-built library handles new parts and routines as work changes. Runs on FT Connect software, with aspects of Smart-Link and X-ray Station software. FT Connect focuses interface on important aspects of XRF. Results are displayed on main measurement screen. Results can be exported in spreadsheet or JSON format for integration with SCADA, QMS, MES or ERP systems. Customized reports can be created. Has functions to confirm instrument stability, including routine instrument checks and calibration validation tools. On-board diagnostics provide information about instrument health. Data can be shared via ExTOPE Connect. High-res SDD screens parts for conformity to restricted materials legislations such as RoHS and analyzes composition of materials, including plating bath solutions and metal alloys, useful for validating incoming substrates and confirming chemistry.

Hitachi High-Tech Analytical Science hitachi-hightech.com/hha

#### EXPRESSPCB PLUS V. 3.1 LAYOUT SOFTWARE

ExpressPCB Plus v. 3.1 layout software creates multipage schematics and validates PCB layout. Schematic Link and Netlist Validation tools support use of symbols in ExpressCSH Plus. Reportedly has improved speed, stability and quality of results in Schematic Link and Netlist Validation tools. Includes updates to SnapEDA API.

#### ExpressPCB

expresspcb.com

#### ADVANTEST DUT SCALE DUO INTERFACE

DUT Scale Duo Interface for V93000 EXA Scale SoC test systems tests advanced semiconductors. Usable space on DUT boards and probe cards is reportedly increased 50% or more; wafer probe and final test setups can accommodate component heights more than 3x taller. Can adapt to existing standard DUT board or probe card size or switch to new larger size. Using sliding mechanism, users can switch back and forth between both formats to adapt to specific applica-

# **SHELF**

tion requirements. Stiff extended bridge achieves deflection performance in direct probing setups. Supports applications including digital and RF device testing.

#### Advantest Corp. advantest.com

#### NOVACENTRIX METALON JG JETTABLE GOLD INKS

Metalon JG jettable gold inks have electrical and physical performance properties. Are for applications requiring biocompatibility or high levels of corrosion resistance. Cure with traditional thermal processes or with PulseForge tools, featuring digital thermal processing to dry, sinter and solder at industrial scale on low-temp. heat-sensitive substrates without damage.

#### NovaCentrix

NovaCentrix.com

#### AEGIS FACTORYLOGIX 2022.1, 2022.2 MES

FactoryLogix 2022.1 and 2022.2 MES feature smart, dynamic visualization. Powers visual work instructions with smart pictures that change depending on context of what is being inspected or worked. Creates one template and is for use in infinite scenarios. Tracks units of measurement (volume, length, etc.) beyond unit level during production process. Expanded support for more process types and product types. Establishes common assembly operation to occur simultaneously across different assembly lines and different products. Can balance approaches, equipment, materials and resources based on similar operations common among products, regardless of assembly line. Supports cost-related parameters and threshold approval workflows when assessing path of action for nonconformance. Sees problems occurring most frequently and those imposing greatest cost. Compares CAD/CAM BoM to externally resident BoM (e.g., ERP) and accelerate BoM compare process.

#### Aegis Software aiscorp.com

#### **AIM SOLDER V9 SOLDER PASTE**

V9 low-voiding, no-clean solder paste is formulated to reduce voiding to as low as 1% on BGA and <5% on BTC com-

### popopta while exhibit

MACHINES

ponents, while exhibiting stable print performance on fine-feature devices over 12 hr. Post-process residue is probed and possesses high SIR values required for high-reliability applications. Is REACH and RoHS compliant. Comes in SAC 305 type 4.

MATERIALS



#### ASC VISIONPRO MERLIN BENCHTOP AOI

VisionPro Merlin benchtop API system is optimized for remote support. Uses 5mp camera with sub 8µm X-Y resolution. Has laser sensor for coplanarity height measurements of components and leads. Flexible universal carrier system inserts PCB up to 460mm x 360mm, clamps it and inspects with press of a button. Once complete, PCB is returned to load point ready for next PCB to be loaded. Includes 1-D and 2-D barcode reading as standard. Can be combined with Prey rework suite. Combines excellent mechanical stability with 64bit software and Windows 10/11 OS.

#### ASC International

ascinternational.com



#### EMIL OTTO ETIMOL SEM 12 RAA Soldering system cleaner

Etimol SEM 12 RAA is non-labeled medium for cleaning reflow ovens, wave and selective soldering systems, and vapor phases. Impurities and flux residues can be removed. Water-based, alkaline cleaning system removes outgassing from PCBs from soldering systems used in electronics manufacturing. Can be used on residually warm soldering machines. Has mild odor. Is sprayed onto surfaces to be cleaned at room temp. and removed after a few min. of exposure time. Reportedly no residues of cleaner remain in soldering equipment when soldering temp. >200° are reached. Is label-free and not hazardous.

SOFTWARE

SYSTEMS

#### Emil Otto

TOOLS

emilotto.de

#### HELLER 1911MK5-VR NITROGEN VACUUM REFLOW OVEN

1911MK5-VR Nitrogen vacuum reflow oven has 11 zones, a vacuum chamber, closed-loop nitrogen atmosphere control and Cool-Pipe flux management system, trapping flux so it can be removed and replaced while oven is running. Targets voiding ratios of less than 2% and cycle times of 40 sec. for single-lane implementation and 20 sec. for dual-lane systems. Maintains solder paste reflow specification, including liquidous times of under 60 sec. Is suitable for hightemp. applications up to 450°C. In-Zone IR heating.

Heller Industries

hellerindustries.com



#### ITW EAE CAMALOT PRODIGY ADVANCED TILT AND ROTATE OPTION

Advanced tilt and rotate dispensing system is available for Camalot Prodigy. Reduces wet-out areas and improves capillary flow for underfill. Provides access to dispense on side walls, underneath, or around tall components. Rotary actuators reportedly provide zero backlash mechanism that allows articulation of dispense pump in sub-degree increments in both axes as many times as needed. Setup and calibration are automated functions that run after machine has been initialized or if pump has been removed and replaced; ensures camera needle offsets at different angles, and rotations are known.

ITW EAE

itweae.com



SOFTWARE

#### MACDERMID ALPHA HRL3 SOLDER SPHERE

Alpha HRL3 solder sphere is a leadfree, high-reliability, low-temp. alloy for ball-mount applications. Designed to exhibit improved drop shock and thermal cycling performance versus existing low-temp. alloys. Offers wide operating window and reduced warpage. Capable of soldering at temp. lower than standard tin-silver copper alloys.

MacDermid Alpha Electronics Solutions MacDermidAlpha.com

#### MASTER BOND MASTERSIL 323 BONDING SILICONE

MasterSil 323 two-component, additioncured silicone for bonding, sealing and potting applications has 1:1 mix ratio and can be packaged in double barrel cartridges for dispensing from a gun applicator. Applicable in thin and thick sections. Elongation of 150-250% at room temp., Shore A hardness of 35-45 and tensile modulus of 100-175psi at 75°F for stress relief. Withstands thermal cycling and shock without cracking or exerting stress on components. Dielectric constant is 2.8 at 75°F, 1 MHz.

#### Master Bond masterbond.com

#### NORDSON ELECTRONICS HELIOS SD-960 DISPENSER

Asymtek Helios SD-960 series fluid dispenser comes with FS-EP1 fluid supply/feeding system 1-gal. pail pump for single-component TIMs. Pushes material to dispense valve using closed hydraulic system. Low shearing of material ensures conductive thermal gap fillers do not separate, and material properties remain unaffected. No moving parts come in contact with gap filler; no moving parts are outside pump enclosure. Pump enclosure securely holds 1-gal. pail at operator's waist-level, so it is simple to load and remove. When it's time to change out pail, semi-automated airbleed routine with priming valve ensures

air is removed from the system, operating behind the closed, safety-interlocked doors. Other features include durable hydraulic pump, intuitive operator interface, and tool-free seal changeover.



#### TRI TR7500QE PLUS 3-D AOI

TR7500QE Plus multi-camera 3-D sideview AOI performs at speeds up to 57 cm<sup>2</sup>/sec. Is equipped with AI-powered algorithms and increased mechanical capabilities. Includes four sideview cameras for front, rear, left and right viewing angles – and views from top camera. Detects concealed defects from top camera view. Sideview cameras inspect innerlayer bridges, hidden lifted leads and other out-of-sight defects.

#### Test Research Inc.

tri.com.tw/en/index.html



#### VISICONSULT QUADCOUNT LIVE SMART BARCODE READER

VCcount now includes QuadCount Live smart barcode reader. Data are automatically scanned as SMD reels are placed into drawer, autoloading real-time information into system without clicking or confirmation required. Includes updated software. Detects position and barcode as SMD reel is placed over loading drawer; enables tracking of reel positioning and automatic label printing after reel removal. Camera provides live feedback prior to counting. Detects changes of reel position. Directly controls labeling printer after each reel removal. Camera is available with 2.3MP or 5MP. XRHCount customers can add QuadCount Live.

VisiConsult



#### WELLER ZERO SMOG 4V REPLACEMENT FILTER

Replacement main filter for Zero Smog 4V is for soldering, laser and gluing applications. Is comprised of HEPA class H13 particle filter and granulated media. Contains 2.2kg of granular media composed of 50% activated carbon, 50% KMnO<sub>4</sub> (potassium permanganate). This 50/50 mixed media is reportedly versatile and effective with more gases than activated carbon on its own. Includes small silicone hose and connector used by Zero Smog 4V to measure differential pressure through filter to indicate when filter is full. Also fits Zero Smog EL and TL filtration units. Life of main filter is extended by using it in conjunction with prefilters.

Weller Tools

apextoolgroup.com

#### 1 CLICK SMT INTRODUCES UNIT-I1 SELECTIVE SOLDERING MACHINE

Unit-i1 compact inline selective soldering machine is less than 55" in length. Combines drop jet fluxer nozzle, bottom IR preheating, selective solder pot and AOI function. Is for fluxing/preheating/soldering inspection. After soldering is complete, built-in AOI inspects all soldered joints for bridging, less solder, excessive solder, solder particles, etc. Auto repairing function can be activated to solder defect position again automatically. Is reportedly ideal for smart factories. Can be used as standalone or as module with high flexibility. For volume production, customers can place unlimited boards one after another. For production of different boards, customers can separate each machine.

1 Click SMT Technology

1clicksmt.com
#### In Case You Missed It

#### Additive Manufacturing

"A Review on Printed Electronics with Digital 3D Printing: Fabrication Techniques, Materials, Challenges and Future Opportunities"

Authors: C. Hanumanth Rao, et al.

Abstract: The introduction of 3-D printing technology has revolutionized the manufacturing and electronics product design in the past few years, where it is used to produce printed circuit boards. Printed electronics is one of the fastest growing additive manufacturing technologies and is becoming invaluable to various industries. The evolution of several contact and noncontact types of fabrication techniques has been reported in the recent past. Leveraging these technologies, various types of printed electronic components have been realized. One method is inkjet printing technology, which has been widely accepted for printed electronics manufacturing. As 3-D printing uses only those materials essential to create the product, it eliminates waste production, with a smaller equipment cost and minimizes the number of process steps, resulting in lower manufacturing costs with reduced turnaround time. Various kinds of conductive and nonconductive materials have emerged in the recent past in conjunction with many manufacturing techniques for printed electronics. Herein, the authors review the most commonly used substrates, electronic printing materials, and the widespread printing techniques employed at the industrial level, giving an overall vision for a better understanding and evaluation of their different features. The technical challenges of several contact and noncontact techniques with corresponding solutions are also presented. Finally, status on advances in the production of various kinds of materials employed in 3-D printed electronics and the methods for producing them, shortcomings, technical challenges, applications, benefits, and the future opportunities pertaining to printed electronics are discussed in detail. (Journal of Electronic Materials, Apr. 1, 2022, link.springer.com/ article/10.1007/s11664-022-09579-7)

#### IC Reliability

"Artificial Intelligence Deep Learning for 3D IC Reliability Prediction"

Authors: Po-Ning Hsu, et al.

*Abstract:* Three-dimensional integrated circuit (3-D IC) technologies have been receiving much attention recently due to the near-ending of Moore's law of minimization in 2-D ICs. However, the reliability of 3-D ICs, which is greatly influenced by voids and failure in interconnects during the fabrication processes,

typically requires slow testing and relies on human judgment. Thus, the growing demand for 3-D ICs has generated considerable attention on the importance of reliability analysis and failure prediction. This research conducts 3-D x-ray tomographic images, combined with AI deep-learning based on a convolutional neural network (CNN) for non-destructive analysis of solder interconnects. By training the AI machine using a reliable database of collected images, the AI can quickly detect and predict the interconnect operational faults of solder joints with an accuracy of up to 89.9% based on non-destructive 3-D x-ray tomographic images. The important features that determine the "good" or "failure" condition for a reflowed microbump, such as area loss percentage at the middle cross-section, are also revealed. (Scientific Reports, Apr. 25, 2022, nature.com/articles/s41598-022-08179-z)

#### Sensors

"Thin Film Magnetoelectric Sensors Toward Biomagnetism: Materials, Devices, and Applications"

Authors: Cunzheng Dong, et al.

Abstract: Since the discovery of strong magnetoelectric (ME) coupling in two-phase ME laminate composites, strain-mediated ME heterostructures have found practical applications in magnetic sensors, tunable inductors, tunable filters, miniaturized antennas, magnetic memories and nanoscale motors. Thin-film ME sensors, in particular, have become promising candidates in biomagnetic sensing, due to their high sensitivity, CMOS compatibility, room-temperature operation and high spatial resolution. In this article, an overview is presented on different types of thinfilm ME sensors and their applications in biomagnetic measurement. First, the coupling structures, materials selection and fabrication processes are introduced. Three different mechanisms of recently emerged ME sensors, including the magnetic modulation, electrical modulation and delta-E effect are presented. Their performance and noise analysis are also compared and discussed. Finally, real-time applications of ME sensors in the detection of magnetic fields from different parts of the human body are presented and discussed. The review concludes with an outlook on future perspectives and challenges of thin-film ME sensors for biomagnetic applications. (Advanced Electronic Materials, May 4, 2022, onlinelibrary.wiley. com/doi/10.1002/aelm.202200013)

This column provides abstracts from recent industry conferences and company white papers. Our goal is to provide an added opportunity for readers to keep abreast of technology and business trends.



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