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PRINTED CIRCUIT DESIGN & FAB/CIRCUITS ASSEMBLY is published monthly by Printed Circuit Engineering Association, Inc., PO Box 807 Amesbury, MA 01913. ISSN 1939-5442. GST 124513185/ Agreement #1419617.

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Recent Meetings Revive Future Possibilities

ND WE'RE BACK!

After a (too long) break, PCEA meetups have restarted with a bang, with two local chapter meetings, plus the first national event in PCEA history.

Professional development was the focus of both chapter meetings. This can be looked at two ways: one in terms of technology advancements and the other tied to learning the basics of placement and routing.

The pandemic is driving change, not just to the way we work, but what we work on. Per John Watson of Altium, who spoke at both meetings, "Advancements in technology are partially a result of the pandemic." The industry "forced us into redoing the way we do things."

As reported by PCEA chief content officer Chelsey Drysdale, Watson says designs for IoT, drones and nanotechnology, among others, were "science fiction" just a decade ago. Today, they are commonplace, and others (additive manufacturing?) are right behind them.

Yet, while today's designs are typified by higher frequencies, smaller boards, and bigger, heavier stackups, the industry is losing experience. A survey shared by Watson suggests more than half of designers plan to retire in the next 12 months.

While I don't buy that, there's no question the profession is in transition. EEs are taking over more PCB design responsibilities, but when layout is only a small component of their overall job, developing proficiency is challenging. "A lot of EEs don't want to do PCB layout. They think it's someone else's responsibility," said Watson.

Let it be said colleges aren't trade schools. We could debate the role of higher education for months, but changing the current model is not going to happen overnight, if ever. PCEA, of course, supports the efforts of companies like EMA Design Automation, which has partnered with Rochester Institute of Technology to develop a college course on PCB design (and has plans to expand that to other universities).

Meanwhile, collaborations between community colleges like Palomar in San Diego and high schools offer the infrastructure to rebuild the entry-level segment of the profession from the ground up, "starting," as Watson says, "at step one for new designers with no experience." Palomar also has two advanced courses for seasoned designers and plans to offer degree programs. Ultimately, the college plans to scale its program statewide.

These are the types of programs that will set the

stage for replacing drafting in vocational schools, from which generations of PCB designers matriculated, with targeted college classes that prepare tomorrow's engineers.

Supplementing this is the PCE-EDU program. We can't say enough about this curriculum. There are, at my count, three privately developed curricula available for PCB design. Only one, however, is both current and written by a group of experienced design professionals. PCE-EDU was developed by Mike Creeden, Susy Webb, Rick Hartley, Gary Ferrari and Steph Chavez. That's more than 180 years of design engineering experience right there. Creeden, Ferrari and Hartley have chaired IPC standards task groups for board design and high-speed, and Ferrari was coauthor of the original IPC CID program. Among them, they have trained thousands of design engineers worldwide. No one knows more about training designers than this group.

Launched last year, PCE-EDU has now certified 100 designers. Explains Creeden, who also spoke at both chapter meetings, "CPCD is crafted to create a layout engineer/designer. The curriculum is technically up to date. I need to know why I push a button before I know which button to push." Learn more at pcea.net/pce-edu-design-engineer-curriculum.

Supplementing the chapter meetings, PCB East proved a successful return to the East coast of the US after a 13-year absence. More than 600 industry professionals registered for the event. Highlights included Gene Weiner's keynote, which traversed a host of new technologies ranging from laminates to algorithmic engineering, which converts labor-intensive engineering processes into algorithms, permitting physical objects and entire machinery to be designed automatically. He cited Continuous Laser Assisted Deposition Technology (CLAD), a nozzle-free laser-jetting technology said to deposit material of any viscosity. The materials that can be jetted range from solder masks and pastes (Types 5 to 7), polyimides, epoxy and silicone, Weiner said.

Weiner also noted the gains made in additive manufacturing. Nano Dimension supplemented that with a special AME Academy presentation, revealing the vast potential for printed electronics. While not a panacea, AM gives every engineer the potential for quick design proof of concept. That alone makes it worth further investigation.



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PCDF People

Amazon Lab126 named Faisal

Ahmed ECAD application engineer. He has more than 20 years' experience in PCB design, most recently at Cadence.

Anirudh Devgan, Ph.D., president and CEO, Cadence Design Systems, will be honored with the 2021 Phil Kaufman Award for Distinguished Contributions to Electronic System Design during a ceremony May 12.

NXP Semiconductor promoted **Dan Beeker** to technical director. He has more than 40 years' experience in engineering with Freescale and NXP.

PCDF Briefs

NextFlex announced \$17 million in funding for 18 new projects as part of its Project Call 6.0 to further promote FHE development and adoption throughout the US advanced manufacturing sector.

Prototron Circuits installed a Maskless model 5600 LED direct imager.

Yokogawa Electric selected Zuken's CR-8000 electronic systems design software for all Japanese, Chinese and Korean subsidiary locations.

CA People

AIM Solder's **Andres Lozoya** has been awarded a Lean Six Sigma Black Belt.



Apex Tool Group named **Rich Mathews** chief marketing officer. He has over 30 years' experience modernizing and growing consumer brands.

ARC Technology Solutions named **Rich Flynn** supply chain manager.

Arch Systems appointed **Cameron Sobie**, **Ph.D.**, senior staff factory data scientist.



Arch Systems also appointed Georg Fuerlinger (left) senior account manager. Based in Vienna, Austria, Fuerlinger will work with Arch Systems' clients and strategic partners throughout Europe.



Emerald EMS named Uma Patravali president of the Bestronics manufacturing division. Patravali has a master's in industrial engineering from Western Michigan and has

worked for GE, Creation Technologies and Sanmina.

Private Equity Firm Acquires Elvia PCB Group

NORMANDY, FRANCE – Private equity firm Tikehau Ace Capital has finalized the acquisition of 100% of the capital of Elvia PCB Group. Terms were not disclosed.

Alain Dietsch has been appointed CEO of Elvia PCB. He was previously CEO of Cobham Electrical and Electronic Equipment.

Bruno Cassin will leave his operational duties to join the supervisory board.

Elvia PCB had consolidated revenue of €60 million in 2019. The group manufactures PCBs for defense, aeronautics, space, industrial, telecom, automotive and medical.

BH to Acquire LG's In-Car Handset Wireless Charging Business

SEOUL – Printed circuit board fabricator BH said it will acquire LG Electronics' in-car handset wireless charging business unit for 136.7 billion won (US\$111.5 million), according to reports. BH will form a new subsidiary called BH EVS, and the acquisition is expected to be completed in August.

BH said demand for in-car handset wireless charging units is some 20 million units per year. The firm expects orders worth US\$2 billion in the next decade.

BH CEO Lee Kyung-hwan will be CEO of BH EVS, and BH will own a 56% stake. DKT, another subsidiary of BH, will own a 44% stake.

CCL Maker NexFlex Receives Buyout Bids

SEOUL – Six investors have submitted bids in a preliminary tender for 100% stake in NexFlex, according to reports. The sale price is estimated around 700 billion won (US\$574 million).

NexFlex manufactures flexible copper-clad laminates for smartphone and TV flex substrates. The firm supplies FCCLs to companies such as Samsung Electronics and Apple.

The company is currently held by private equity firm SkyLake Equity Partners. A final candidate was expected to be shortlisted in April.

Its annual revenue expanded to 150 billion won in 2021 from 69 billion won in 2019.

Nano Dimension Opens HQ Near Boston

WALTHAM, **MA** – Nano Dimension opened a new US headquarters in the Boston suburbs. The move to Waltham, MA, enables the additive manufacturing OEM to work closer to academic and research institutions, early adopters of its solutions for AME, printed electronics and Micro-AM.

The new headquarters will house expanded sales operations, customer support and fabrication facilities that will be used for customer open houses and continued support for AME Academy events and local organizations.

Veteran Gene Weiner has been retained as a consultant through his firm Weiner International Associates. In addition, Dana Korf, principal consultant, Korf Consultancy, has signed on as Nano Dimension's new AME standards manager.

Nano Dimension retains its presence in Sunrise, FL, as a marketing, sales support and NaNoS printing services and logistics center.

KLA Moves Frontline DfM to Cloud

MILPITAS, CA – KLA launched Frontline Cloud Services, a software solution that accelerates design-for-manufacturability analysis and time-to-market for printed circuit boards. The new cloud-based SaaS offering moves DfM analysis to the cloud, which, according to the company, significantly reduces IT bottlenecks and the amount of time needed to run analyses.

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Escatec appointed **Ernest Sebak** chief executive officer. Sebak was formerly vice president of Jabil's Global Business Unit. He succeeds CEO **Patrick Macdonald**, who is stepping down.

Incap Group appointed **Miroslav Michalik** director of operations Slovakia. He will continue as managing director of Incap Slovakia.



Kurtz Ersa hired **Ian Orpwood** as North American director of sales-soldering tools and equipment. Orpwood previously served as global director of sales at OK International.



Libra Industries promoted Matt Tringhese to vice president of global operations. Tringhese's career at Libra Industries began in 2012 as a second shift production supervisor.



Sanmina named **Shawn Brady** Northeast business development manager. He has more than 35 years' experience in EMS sales, most recently with Virtex.



ViTrox Technologies appointed Guilherme Pereira as sales and support manager for the Brazil region. Pereira has more than 15 years' experience in AOI, AXI and ICT in assembly

manufacturing.

CA Briefs

CGI Americas announced orders for more than \$1.5 million for WOL-7 and WOL-8 cleanroom ovens.

Dynetics selected **Benchmark Electronics** to manufacture electronic components for the company's Enduring Shield mobile ground-based weapon system.

EVS International appointed as manufacturers' representatives **Ark Manufacturing Solutions** in Arizona, New Mexico and Southern Nevada, **Competitive Edge Solutions** in the New England US, and **Wittco Sales** in Southern California.

LTKM Berhad, a leading chicken egg producer, announced a composite proposal under which the company will divest its existing business and venture into electronics manufacturing services.

Pillarhouse appointed **Wittco Sales** sales representative in Southern California, Southern Nevada and Baja Mexico. Asserting on-premises DfM analysis can take hours or days, KLA proposes a cloud-based solution to tap greater compute power.

"As a leader in PCB CAM, engineering and Industry 4.0 solutions, our customers share with us the bottlenecks that slow down their PCB manufacturing process," said Eran Lazar, general manager, Frontline division, and vice president at KLA. "We decided to tackle the challenges of DfM analysis by taking advantage of the unlimited computational power of the cloud, while keeping the proven application intact. For PCB manufacturers eager to make the most of cloud-based efficiencies while maintaining exacting security protocols, we continually ensure Frontline Cloud Services meets the highest security standards."

Per the company, customers running comparative tests on complex PCBs saw Frontline Cloud Services enable up to 90% faster DfM analysis speeds. For example, one customer producing high-density interconnect PCBs saw analysis time shorten to 30 minutes from 75 hours when running the same DfM analysis on premises versus with Frontline Cloud Services. Another customer producing PCBs for miniLED ran a similar test, and analysis time was reduced to 20 minutes from nine hours.

Altium Launches Electronic Design Program for College Students

SAN DIEGO – Altium launched Altium Education, a free online curriculum and certification program for college and university students interested in engineering and electronics design. This hands-on course takes college students from the basics of electronics to designing their first printed circuit board.

Altium Education is for university and college students studying engineering and computer science. Designed for virtual, hybrid and physical classrooms, the curriculum supplements engineering classes, and professors can incorporate it into their current lesson plans.

The program features hands-on lessons focused on schematics, design layout and manufacturing. Students will receive guided instruction that culminates in the completion of their own manufacturable PCB. An educator's guide is provided for the course. A free license of Altium Designer ECAD software is included for any student enrolled in the course.

Upon course completion, students will obtain a certificate signifying they have successfully completed Altium's course covering the fundamentals of PCB design.

ISU Petasys to Construct 4th Fab Shop in South Korea

DAEGU, SOUTH KOREA – Printed circuit board fabricator ISU Petasys plans to spend 54 billion won (US\$44 million) to build a fourth factory here, according to reports. The site will manufacture multilayer boards.

ISU Petasys currently makes boards for Nokia, Cisco, Juniper, Arista and others. The firm reportedly is looking to add Google to its client list.

The company said multilayer board demand is high because of 5G.

Simmtech to Open Factory in Penang

PENANG – Simmtech Holdings will invest more than S\$120 million to establish its first large-scale factory in Malaysia to address the global chip shortage, according to reports.

Once fully operational, the production facility is expected to employ more than 1,000 staff and contribute more than 20% to the company's global capacity.

Simmtech provides printed circuit boards and packaging substrates for the semiconductor industry.

TTM Breaks Ground at 1st Factory in Penang

PENANG, MALAYSIA – TTM Technologies in April broke ground at a new \$130 million manufacturing plant here.

TTM's expansion here is in direct response to customer requirements for advanced technology PCB supply chain resiliency and diversification in regions beyond China, the firm says. The new plant will serve TTM's global commercial markets, including networking communications, data center computing, and medical, industrial, and instrumentation.

The automated plant will be built on approximately 27 acres of industrial land at Penang Science Park. Construction is expected to take 12 to 15 months, followed by equipment installations in the middle of 2023. Pilot production is targeted to begin in the second half of 2023, with volume production commencing in 2024, gradually ramping to full phase 1 capacity in 2025.

TTM expects the new plant to achieve run-rate revenue of approximately \$180 million in 2025. The factory has also been planned to support a 25% upside phase 2 expansion.

Katek to Buy SigmaPoint, Expand to North America

MUNICH – Katek has signed a comprehensive, exclusive term sheet to acquire Canadian electronics manufacturing services provider SigmaPoint Technologies. Financial terms were not disclosed. Closing is planned for the end of the second quarter, subject to official approvals.

The move expands Katek's presence to include homeland security and defense and strengthens the offering for Katek's European customers in North America.

SigmaPoint is one of Canada's leading EMS providers, with annual sales over \$100 million and 280 employees. Its largest customer in North America is one of Katek's top five customers in Europe.

SigmaPoint CEO Dan Bergeron and the full management team will continue to lead SigmaPoint after the acquisition.

The investment is part of Katek's strategy of opening additional markets for high-value electronics.

Rainer Koppitz, CEO, Katek, said, "As the number three electronics service provider in Europe, we are making good on the promise to our European customers of a presence on the North American continent."

Katek also is opening its first Asian plant in Malaysia.

Neways to Construct EMS Factory in Slovakia

NOVA DUBNICA, SLOVAKIA – Neways said it plans to replace its two electronics manufacturing sites in Slovakia with one new 16,000 sq. m. factory, according to reports. The new site will focus on PCB, cable harnesses and cabinet production.

The company says the facility will potentially grow to

800 staff, and the location will provide the option for further expansion.

Construction is set to begin in October, and the site will be fully operational by the end of next year.

SEMI Wins \$1M Grant to Create Microelectronics Apprenticeship

MILPITAS, CA – SEMI, in partnership with Ignited Education, Foothill College and Krause Center for Innovation, has won a \$1 million California Apprenticeship Initiative New and Innovative Grant for the development of a semiconductor pre-apprenticeship and apprenticeship program to expand the pathway to careers in the microelectronics industry.

The SEMI Foundation and its partners will develop the industry career training program to be offered by California community colleges and ultimately schools in other states. The program will connect CAI partners with SEMI member companies to define job competencies that shape the coursework.

The CAI funding will support the SEMI Foundation's work to build the SEMI Career and Apprenticeship Network (SCAN) aimed at helping overcome the US microelectronics industry's talent shortage as the federal government continues to invest in apprenticeships. The grant also supports the foundation's efforts to promote a more inclusive workforce. SCAN will offer training that equips workers with the technical skills needed to enter highdemand, entry-level jobs in the microelectronics industry. It will also expand the pool of skilled workers for hiring companies.

"Securing the CAI funding is a key step in building out SCAN as we work to develop a national apprenticeship network, recruit more people of color and women to the industry, and create industry credentials recognized nationwide," said Shari Liss, executive director, SEMI Foundation. "We look forward to continuing the vital work with our partners to expand access to jobs across the semiconductor industry and enable more people to enter rewarding careers."

Foothill College will develop coursework covering the competencies for high-need positions in the microelectronics industry. Complementing the work of Foothill College, Ignited and the Krause Center for Innovation will create middle school foundations and high school pre-apprenticeship programs featuring engaging student experiences and teacher-training workshops.

VTech Mexico EMS Plant Nears Production Readiness

TECATE, **MEXICO** – VTech's first EMS facility outside Asia is making progress toward establishing production. The proaudio focus supports wood and non-wood (semi-EMS) production.

The Mexico facility is able to fully leverage the Top 50 EMS company's supply chain in China and Malaysia. Its NPI team supports Mexico through all stages from concept to mass production.

VTech acquired the plant in 2021 from QSC, where it manufactured wood enclosure loudspeakers.



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COMPONENTS CREEP UP				
Trends in the US electronics equipment market (shipments only)	DEC.	% CH/ Jan.	ANGE Feb.	YTD%
Computers and electronics products	1.2	1.9	1.2	5.9
Computers	-2.1	2.5	3.8	-0.9
Storage devices	1.9	6.8	2.0	10.8
Other peripheral equipment	7.1	-3.7	6.5	-3.6
Nondefense communications equipment	-0.3	8.0	0.9	14.3
Defense communications equipment	1.3	6.0	-1.6	8.5
A/V equipment	-7.3	34.5	-8.2	50.3
Components ¹	0.9	2.8	2.4	14.2
Nondefense search and navigation equipment	0.3	1.0	-1.0	1.7
Defense search and navigation equipment	-0.1	0.8	1.2	1.6
Medical, measurement and control	1.9	-0.3	0.8	2.8
^r Revised. *Preliminary. ¹ Includes semiconductors. Seasonally adjus Source: U.S. Department of Commerce Census Bureau, Apr. 4, 2022	ted. 2			

PCB Design Software Sales Leap 14% YoY in Q4

MILPITAS, CA - Sales of printed circuit board and multichip module design software increased 13.9% to \$333.7 million in the period ended Dec. 31, the ESD Alliance announced in April.

The four-quarter moving average for PCB and MCM, which compares the most recent four quarters to the prior four, rose 15.1%.

Overall electronic system design (ESD) revenue increased 14.4% to \$3.47 billion. The four-quarter moving average rose 15.8%.

Companies tracked in the report employed 51,236 people globally in the quarter, up 5.7% year-over-year and 0.1% sequentially.

Computer-aided engineering revenue increased 11.2% to \$1.06 billion, IC physical design and verification revenue decreased 2% to \$625 million, semiconductor intellectual property revenue jumped 25% to \$1.3 billion, and services revenue increased 43% to \$131 million.

The Americas was the largest reporting region by revenue, up 21% to \$1.58 billion. Europe, Middle East and Africa (EMEA) rose 5.5% to \$482.5 million, Japan fell 2.4% to \$223 million, and Asia Pacific rose 14% to \$1.19 billion.

Global Semi Equipment Sales Surge 44% in 2021

MILPITAS, CA - Worldwide sales of semiconductor manufacturing equipment in 2021 surged 44% year-over-year to an all-time record of \$102.6 billion, says SEMI.

China claimed the largest market for semiconductor equipment for the second time with sales expanding 58% to \$29.6 billion to mark the fourth consecutive year of growth. Korea, the second-largest equipment market, registered a sales increase of 55% to \$25 billion, after showing strong growth in 2020. Taiwan logged 45% growth to \$24.9 billion to claim

Hot Takes

- Global semiconductor materials revenue grew 15.9% to \$64.3 billion in 2021. (SEMI)
- Total semiconductor sales will rise 11% in 2022, following a 25% increase in 2021 and an 11% increase in 2020. (IC Insights)
- Worldwide semiconductor revenue totaled \$595 billion in 2021, an increase of 26.3% from 2020. (Gartner)
- The worldwide market for augmented reality and virtual reality (AR/VR) headsets grew 92% year-over-year in 2021, with shipments reaching 11.2 million units. (IDC)
- Global fab equipment spending for frontend facilities is expected to jump 18% year-over-year to an all-time high of \$107 billion in 2022. (SEMI)
- Spending on compute and storage infrastructure products for cloud infrastructure, including dedicated and shared environments, increased 13.5% year-over-year in the fourth quarter of 2021 to \$21.1 billion. (IDC)
- The global PC monitor market continued its quarterly decline in the fourth quarter, with unit shipments shrinking 5.2% compared to the same guarter in 2020. (IDC)
- By 2025, the market share of smartphones supporting Wi-Fi 6 and 6E is estimated to surpass 80%. (TrendForce)
- Worldwide IC unit shipments will increase 9.2% this year to 427.7 billion units. (IC Insights)
- Worldwide sales of semiconductor manufacturing equipment in 2021 surged 44% year-over-year to an all-time record of \$102.6 billion. (SEMI)
- Global shipments of smart home devices grew 11.7% in 2021 to more than 895 million. (IDC)

US MANUFACTURING IN	IDICES				
	NOV.	DEC.	JAN.	FEB.	MAR.
PMI	61.1	58.8	57.6	58.6	57.1
New orders	61.5	61.0	57.9	61.7	53.8
Production	61.5	59.4	57.8	58.5	54.5
Inventories	56.8	54.6	53.2	53.6	55.5
Customer inventories	25.1	31.7	33.0	31.8	34.1
Backlogs	61.9	62.8	56.4	65.0	60.0
Source: Institute for Supply Management	, Apr. 1, 2022				

KEY COMPONENTS						
	NOV.	DEC.	JAN.	FEB.	MAR.	
EMS (North America) ¹	1.43	1.55	1.58	1.52	1.44	
Semiconductors ²	24.5%	28.3%	26.8% r	32.4% ^p	TBD	
PCBs ³ (North America)	1.10	1.17	1.18	1.16	1.05	
Computers/electronic products ⁴	5.34	5.32	5.24 ^r	5.17 ^p	TBD	
Sources: ¹ IPC ² SIA (3-month moving average gro	wth) ³ IPC	⁴ Census Bi	ireau ^p ore	liminary ^r re	vised	

the third position. Annual semiconductor equipment spending increased 23% in Europe and 17% in North America, which continues to recover from a contraction in 2020. Rest of world sales jumped 79% in 2021.

Support For Flex, Rigid Flex and Embedded Component Designs Now Available.



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A rigid-flex design in 3D. Shown with layers spread to improve visualization of the layer stackup. Use Rigid-Flex and Inter-layer DFM analysis to analyze flex and rigid-flex designs.



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Here Comes Supply Chain 4.0!

Will it be able to handle unforeseen events better than its predecessor?

MANY ARE EXCITED and working diligently toward enabling Factory (Industry or Tech) 4.0 to dramatically change their manufacturing and business environment, but maybe we should focus instead on Supply Chain 4.0, as that may change the manufacturing and business environment more – and not in a good way!

Businesses are currently operating within Supply Chain 3.0. Supply Chain 3.0 has taken decades to refine into a highly efficient, cost-effective, global supply chain. We know how we got here. Companies sought lower-cost skilled labor and a cost-friendly operating environment in which to build manufacturing facilities. As manufacturing shifted to these lowercost areas, governments invested in infrastructure and education to attract ancillary businesses to invest there as well. Shipping and logistics improved thanks to the advent of containerships, larger aircraft, better roads and rail, and countries opening their borders to trade. The result was a global supply chain in which components and parts are made almost everywhere and transported "just in time" to assembly sites, before finished products are shipped to customers.

As impressive is how product development now occurs globally with teams from different countries collaborating 24/7 to develop the next great product. This efficient, cost-effective collaboration is again made possible thanks to the development and refinement of communication. Supply Chain 3.0 is robust – a winner for all companies and countries involved. After decades making Supply Chain 3.0 nearly perfect, what could go wrong?

As it turns out, a lot.

It started with tariffs. Government economic saber rattling in the form of tariffs levied on certain goods incented manufacturers to reallocate resources to reduce the financial impact. A single tariff levied on a single item, in a single place, ricochets across the globe, negatively impacting the entire supply chain. No one saw these coming. Tariffs were viewed as highly improbable in the contemporary world, where all economies are connected through a global supply chain. Supply Chain 3.0 suddenly caused considerable stress, especially on logistics and transportation.

The next unforeseen event was a pandemic. Covid put a tremendous burden on all aspects of society. Daily disruptions have been roiling global economies for over two years. The result has been component and product shortages. Some of these shortages have been local. Others have impacted entire industries. Some governments have resorted to shutting down entire cities, leaving manufacturing facilities idle. Working remotely became the norm. Too many were infected with Covid, were too sick to work, or decided to retire early to avoid contracting the virus at their workplace. With everyone hunkered down, travel ground to a halt, further disrupting global transportation and logistics, compounding the problem. The pandemic suckerpunched Supply Chain 3.0, and it is still reeling.

A third unforeseen event was war. Wars have taken place during the evolution of Supply Chain 3.0. Most, however, have been in relatively obscure locations or between countries whose only strategic export is oil. This time the battles are on the border of Europe and between two countries with significant minerals and natural resources, which are - or were - exported globally. With 90% of the world's helium exported by one of the countries and a significant percentage of palladium from the other, the impact on our industry in particular could be dramatic. A lack of helium negatively affects the already stressed chip manufacturing sector. Palladium shortages will further drive up the cost of some surface finishes used in electronics. The war is affecting scores of items. Equally, air and sea transportation have been impacted with no-fly zones in place. "Risk" of a cascading effect on other materials, minerals and resources used in the global supply chain is real. As recently as six months ago, most could not have predicted such an event taking place so close to Western Europe. Once again, an unforeseen event is challenging the robustness of Supply Chain 3.0.

Which brings us to Supply Chain 4.0. What will it look like? While many believe recent events mark the end of a global supply chain undoing, something so complex and bedded in so much infrastructure most likely will not happen, at least not anytime soon. Rather, Supply Chain 4.0 may be a much more bloated, much less efficient, and less cost-effective version of Supply Chain 3.0.

"Just in time" parts distribution may now be a thing of the past. Expect increased inventories and expense at all levels. Geographic investment in factories will shift. All players regardless of nationality will likely diversify and build facilities, probably smaller ones, in a variety of countries to hedge geopolitical and logistics risk. All this will take time, especially as all involved will look at "risk" very differently in a world with less global economic dependency. We are entering a period when supply-chain disruptions will be more the norm than not, and prudent businesspeople will be forced to add cost and time within supply-chain calculations.

So, as we deal with unforeseen events of the past half-decade, we'll have to adapt to a "new" supply chain. Hopefully the next one will be more efficient for a world filled with unanticipated events.

PETER BIGELOW is president and CEO of IMI Inc.; pbigelow@imipcb. com. His column appears monthly.



In PCB Procurement, Negotiate All Over

Review pricing with current and outside suppliers to confirm you are paying the going rate.

"We don't have the bandwidth to move business."

THAT'S WHAT A printed circuit board buyer told me recently.

Let's unpack that because it could be a short-sighted attitude.

When an EMS firm puts a PCB supplier on its AVL, it often asks only for pricing on new projects. When it comes to existing work, the response is often, "We don't move boards once they are placed," or, "we don't have time to rebid those," or, "it takes too much effort to move to another vendor."

Even in the face of rising board costs, many buyers and procurement managers resist moving production away from suppliers they've used for years.

What about your company? Do the people responsible for overseeing your supply chain and ensuring the most cost-effective operation make buying decisions based on lack of "bandwidth?"

If so, it's business malpractice.

Because when that is the prevailing mindset, the PCB supplier is aware of it. They know your board buyer doesn't want to upset the apple cart, and they will take advantage of that. OEM and EMS companies that invest too much of their annual PCB spend with only one vendor are making a costly mistake.

I understand a buyer's concern for good quality and consistent delivery, but you can get that from more than one fabricator. And then it comes down to price. Complacency will cost you money. When EMS firms focus only on winning new business, they are putting their existing business at risk.

Many EMS companies are not being proactive to protect their existing assembly business from jumping to a competitor, especially when it comes to the cost of the bare board. Although the common wisdom is, once won, assembly programs will stay in place, in fact, over the last year several OEMs have asked me to suggest new homes for their assembly work. OEMs are taking a hard look at their assembly costs to remain competitive and maintain profit margins. PCB materials, metals and freight pricing are skyrocketing. It is good business to look at reducing costs wherever possible, especially on existing orders. It can be done successfully without sacrificing quality.

And it's not an excuse to say board buyers are overwhelmed with responsibilities. Keeping the vendor base on its toes is a core responsibility. More important, it's the job of upper management to ensure board buyers regularly seek offers from other vendors to compare with the prices they're getting. Business doesn't always have to be moved to get better pricing, however. The PCB is usually eight to 12% of the BoM, and any savings found can either add to your bottom line or be passed on to the OEM customer, making it less tempting for them to move business away from your company.

As a custom-made item, the printed circuit board's price is somewhat subjective, depending on technology required, volume needed, speed of delivery and location of manufacture.

PCB buyers should always review pricing with present suppliers *and* go outside the company AVL to confirm what they've been paying is in line with the going rate, especially on jobs that have been with the same vendor for a long time. With good industry knowledge, they'll be able to negotiate intelligently. EMS management should encourage buyers to make time to actively quote other qualified sources.

Are your board buyers leveraging their annual PCB spend, or are they being leveraged by a current vendor?

It is not hard to explore the PCB market. For additional PCB supplier leads, buyers need to attend industry trade shows, read trade magazines, search LinkedIn or ask their favorite component rep about good suppliers.

Once that information is accumulated, get an NDA and ask for several quotes. If the quotes are competitive, ask for and follow up on references. If all looks well, *then* get your quality and production departments involved by following your corporate procedure for a new vendor addition.

At the same time, let your existing vendor base know you are looking elsewhere, even if the reason only has to do with price and not performance. At a minimum, this exercise will keep your vendors on their toes when it comes to price, delivery and quality.

Supplier diversification is vital to your success.

Don't get complacent with your PCB purchasing practice. You may regret it.

GREG

PAPANDREW has more than 25 years' experience selling PCBs directly for various fabricators and as founder of a leading distributor. He is cofounder of Better Board Buying (boardbuying.com); greg@directpcb.com.



Selecting the Appropriate Through-Via Technology for a PCB Project

Component manufacturers continue to seek breakthroughs, adding functions and reducing size, while fan-out is left to the designer.

WHILE THE PRINTED circuit board is composed of sheets of dielectric and conductor layers, it's the vias that really bring a circuit to life and keep it going. Permitting signals to pass from one layer to another makes this a 3-D puzzle that can scale to a staggering number of layers.

You don't have to go back many decades to find a time when we called them printed wiring boards. (Officially, the standards still do.) Components were mounted to what looked like a pegboard: rows of evenly spaced holes where the leads of the part extended through two or more of the holes. You just added wire. As far as routing consistency, every board was a one-off, built up one wire at a time.

Give credit to government agencies for driving PCB technology toward higher reliability. Along the way, the "industrial complex" responded with the following electronics innovations:

- Individual transistors advanced to integrated circuits using dual-inline package technology.
- Axial- and radial-leaded passive through-hole components gave way to surface mount types with and without leads.
- Quad flat packages (QFP) and similar devices came along with a full perimeter of signal pins, plus a ground slug taking the central area inside the single ring of pins.
 - Ball grid array (BGA) packages now featured a partial or full field of pins.

Each of these general categories describe a watershed advancement in device packaging as we went from one transistor to billions of them. The PCB industry responded by transitioning to multiple layers of etch, which protected the more vulnerable circuits and permitted higher circuit density.



FIGURE 1. A typical mix of components found on a board that features through-hole vias.

Component manufacturers continually outdo themselves, adding functions while reducing size. The end game is a "marketing breakthrough," where the company can compare its chipset to the others and claim to take up the least amount of PCB real estate. While that claim may be technically true, the part where the fan-out is left to the designer is the unspoken cost of chip-scale packaging.

The standard plated through-hole via. The plated through-hole via still has a long runway. On plenty of devices, the pitch of the pins supports through vias in the go-to size of 8-mil drill with 18-mil capture pads on all layers. This is the usual size for Class 2 commercial applications and permits up to 90° of the drilled/ plated hole to break out from the 18-mil pad. Thicker boards want larger holes, as the fabricator doesn't want to deal with plating high aspect ratio holes. The common 0.062" board thickness is in the sweet spot.

(I will continue using mils for drill/pad sizes and metric units for device pitches. The two systems are blended in the real world, where there are CAM operators and SI/PI people who use mils, and they set the rules. Meanwhile, the chipmakers have settled into decreasing the pin pitch from one rounded metric number to another. I could call it 127 μ m or 5 mils. The point is to be comfortable with the common units of measure.)

Now, where was I?

Class 3 design rules for high reliability. On the high-reliability side, we still use the 8-mil drill but with a 23-mil pad on the outer layer and 21-mil innerlayer. These numbers are intended to ensure a minimum 2-mil annular ring of metal around the hole on every

layer. This must account for layer-tolayer registration, along with hole location and size tolerance.

The vias described above are useful for routing DIP and QFP packages, along with the roomy BGA devices where the pin pitch equals or exceeds 0.8mm. Be careful about managing the vias in the thermal pad that makes up the heart of the QFN/QFP package types. You might get away with adding a few regular vias between the paste stencil openings.

When the device is consuming a considerable amount of current, more vias must be placed in the thermal pad.

JOHN BURKHERT JR. is a career PCB designer experienced in military, telecom, consumer hardware and, lately, the automotive industry. Originally, he was an RF specialist but is compelled to flip the bit now and then to fill the need for high-speed digital design. He enjoys playing bass and racing bikes when he's not writing about or performing PCB layout. His column is produced by Cadence Design Systems and runs monthly



The vias may be filled with a nonconductive material and capped with metal plating so solder cannot migrate down the holes. Last, a conductive fill with little globs of copper mixed with strands of silver in an epoxy base is the plan for drawing out some serious heat.

Case study: Thermally conductive fill. The end of a fiberoptic cable has a transponder that converts light waves from the glass into electrical waves for copper and also generates the light waves going the other direction using a laser. These photo detectors and lasers get very warm as the units strobe along at 10 to 400Gb per second.

In one case, the mechanical engineer thought they had an answer that used a slot in the board and a pedestal in the housing to pass through the board and contact the bottom of the device. The engineer didn't want to believe the PCB could not have a +/-1-mil thickness tolerance. It was a 1mm board, so the standard tolerance was +/-4 mils. That didn't help the engineer's pedestal plan, but it's always good when

the fabricator confirms your statements.

They tried everything: thermal pad, grease and different heat sinks. Only one configuration had a measurable difference: the one where I changed the ground holes in the center pad from 10 mils to 13 and had them filled with the expensive twostep thermal epoxy fill. The measurable difference was it met the spec, and we could ship products to Cisco.

General-purpose PCBs continue to use plated through-hole vias. Plated through-hole vias are sufficient to fan out BGA packages with lower pincount and generous pin-to-pin spacing of 0.8mm or more. It may be possible to use PTH vias on a 0.65mm-pitch BGA, although it uses a 16-mil capture pad. It is likely you will hear from the fabricator if you go this way, even if the finished hole size is decreased to 6 mils. You need to use the 1mm- or 1.27mm-pitch devices to pull off a high-reliability (Class 3) fan-out. The number of layers required grows quickly as each via blocks the routing channel on every layer. We're lucky if we get two traces between the vias. Necking down traces to fit the geometry may not sit well with those signal integrity folks.

Rounding out the plated through-hole via discussion. Thankfully, some FPGA and ASIC vendors still deal in packages that can be used with a 10- to 12-layer board with through-hole technology. Back-drilling may be required for the thicker boards. Extra thin traces and spaces may be required in especially dense areas to allow the signals to escape from the inner part of the BGA devices.

In cases where the vias are incorporated with a heat-sink pin, plugging and capping prevents solder migration, while vias filled with thermally conductive material can dissipate a lot of energy.



FIGURE 3. Opening up the solder mask for the vias provides a convenient method of attaching a jumper wire.





FIGURE 2. A fan-out scheme for the FPGA shown in Figure 1.

and cut off right down the middle for what's called a castellated via. The ground net or even various signals can wrap around the edge or a slot somewhere within the board using castellated vias.

Other than components targeted for mobile applications, many possibilities exist to build a PCB using through-hole technology. Power consumption may be higher while edge rates are lower than their miniaturized counterparts. Some of these more robust parts may only be available in the high-temperature version.

If these things aren't concerning, then perhaps basic PCB technology can be used for simpler projects in a way that extends the expected lifespan. You have to hope they keep on building those components.



Printed Circuit Engineering Professional

The comprehensive curriculum specifically for the layout of printed circuit boards

The **Printed Circuit Engineering Professional** curriculum teaches a knowledge base and develops a competency for the profession of printed circuit engineering layout, based on current technology trends. It also provides ongoing reference material for continued development in the profession. The 40-hour course was developed by leading experts in printed circuit design with a combined 250 years of industry experience and covers approximately 67 major topics under the following headings: Basics of the profession, materials, manufacturing methods and processes; circuit definition and capture; board layout data and placement; circuit routing and interconnection; signal-integrity and EMI applications; flex PCBs; documentation and manufacturing preparation; and advanced electronics (energy movement in circuits, transmission lines, etc.). Class flow: Books sent to students prior to an instructor lead review. This is followed by an optional exam with a lifetime certification that is recognized by the PCEA Trade Association.

The course references general CAD tool practices and is vendor-agnostic. Instructors include Mike Creeden, CID+, who has over 44 years of industry experience as an educator, PCB designer, applications engineer and business owner; and Tomas Chester, P.Eng., CPCD, who has designed over 100 circuit boards through all phases of the product lifecycle, and managed a variety of multifaceted, interdisciplinary projects, from simple interconnect designs to complex microprocessors. For Information or Registration: https://pcea.net/pce-edu-design-engineer-curriculum/

Upcoming Class Openings: More added each month! May 9-13 July 11-15



AUTHORS











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Printed Circuit Engineering Professional

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Build Back Better – and Smarter

As the pandemic becomes endemic, restoring order to the world's prices and supply chains will take time and won't be easy.

AS WE ALL adjust to the reality that Covid and its derivatives are here to stay, communities around the world are beginning to rebuild economically: returning to work, reviving businesses where possible and making new plans if not.

It is no surprise materials, inventory and shipping are in short supply and are often stuck in the wrong places. In some cases, services that companies used to rely on are no longer available because the suppliers have gone out of business. Workforces are depleted, and some knowhow, skills and experience have been lost. Rebuilding is not as straightforward as opening the factory doors, picking up the tools that were put down at the beginning of 2020 and getting on with it. Even now governments are still mandating measures such as the sudden full lockdown of Shanghai, which has severely impacted road and air transport. We must still expect the unexpected!

There certainly is the opportunity to build back better, but let's not be simplistic. The world we built was highly sophisticated and interconnected – an ecosystem of ecosystems. It won't be easy. It will take time. New leaders and innovators need to acquire the skills required to replace those we've lost. And we have other challenges too, like protecting the environment and transitioning to more sustainable ways of living. As if that wasn't enough, further new tensions are adding to the pressure on resources and, as a result, prices.

As we work to restore order, established supply chains remain disrupted or broken. Even without material shortages, the shortage of transportation creates the same effect. Companies are struggling to arrange the supplies they need to fulfill orders received from their own customers. The disruption is transmitted through the entire chain, changing the balance of supply and demand.

The effect on the automotive industry is a highly visible case. It affects everyone making, selling and buying cars. Over the past three decades or so, the electrification of mobility has provided many growth opportunities for our industry and has delivered increasingly efficient and intelligent vehicles that are more satisfying to drive, safer, more comfortable and more economical. The electrification of the drivetrain is the ultimate stage of evolution when passenger cars become, in essence, consumer electronic products.

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Today's latest models are full of chips controlling everything from mirror dimming and mood lighting to internet connectivity, high-voltage battery management and autonomous driving. Except they are not. Supply shortages mean carmakers are struggling to fulfill orders for new cars. Major manufacturers are producing fewer vehicles and prioritizing their most in-demand models because they cannot source all the electronic components needed.

On the other hand, pressures such as increasing fuel prices, legislation on emissions, and the prospects for restrictions on new combustion-engine vehicles should buoy demand for the latest most efficient vehicles. And, while customers wait, demand for used cars is increasing, driving market prices upward.

In the longer-term, semiconductor makers are working to increase capacity to service the demand. However, that takes time, and semiconductor demand will continue to grow as the leading markets reach government-imposed deadlines outlawing sales of combustion-engine vehicles.

Some of the worldwide supply problems resulting from the pandemic are short-term issues. As acceptable prices are negotiated (or alternative solutions are imagined and enacted), output resumes, and shipping returns to more normal routines, problems will subside; inflationary pressure should ease, and availability of goods and services should improve. Other changes to the established order are here to stay, some part of the new post-pandemic reality and others due to strengthening environmental protection, including an emphasis on carbon offsetting and the switch to green energy.

I've commented on the dynamics of supply-chain management before, and there is an even clearer justification and more urgent demand for closer collaboration between suppliers and customers to ensure the greatest possible efficiency. Sharing production plans enables partners to guarantee materials arrive in the right places at the right time. While "too little, too late" is as disastrous as always, "too much, too soon" is a luxury that, in the current economic climate, adds to costs considerably. Saving these costs through better plan and data sharing is one of the many changes we need to make as we adjust to the situation we find ourselves in. It is worth remembering the highest cost a manufacturer can experience is that of having no materials to process.

It will be difficult to definitively declare the pandemic "over." That may be best left to the World Health Organization. We cannot beat Covid. It's in the world, and we must live with it, but we can be encouraged we are finding ways to do this, and, as we restart economic activities, we can only be bullish, adopt the spirit of "build back better," and strive to realize the cleaner world we want to inhabit, make use of the experiences we have gained and continue to work to make all our lives healthier, more secure, safer and happier. □

This Indium Corporation webinar series addresses a range of topics beneficial to anyone with technical involvement or interest in electric vehicles and the automotive industry.

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JOIN our discussion!











Bandwidth for MODELING AND MEASURING PCB Interconnects

Numerical analysis of defects in single bit and single symbol response. by YURIY SHLEPNEV, PH.D.

Modeling and measuring digital serial interconnects is usually done in the frequency domain. That means the minimal and maximal frequencies (or bandwidth) should be defined before analysis or measurement begins. The data rate and rise time define the signal bandwidth, and the usual practice is to define the maximal frequency as either the inverse of the rise/fall time (or fraction of it) or as a multiple of the fundamental or Nyquist frequency.¹ Such a simple bandwidth definition may work for some structures, but it may fail for others. Ultimately, an SI engineer must make the decision for a particular signal type and interconnect structure.¹

Here we introduce a simple, practical way to identify the bandwidth with a numerical analysis of defects in a single bit (SBR) or single symbol response (SSR). It begins with a brief introduction into structure and spectrum for 6Gbps and 112Gbps signals. Then, it proceeds with analysis of defects in SBR and SSR introduced by the bandwidth deficiency for two practical cases. The bandwidth is defined by a model with an acceptable level of defects in either SBR or SSR.

High-Speed Serial Data Signals

A digital signal in a serial link is a sequence of bits transmitted through the PCB or packaging interconnects as a sequence of pulses modulated by amplitude. The digital interconnect modeling problem is actually the analog problem of modeling the propagation of pulses in the time domain.

Most often a simple two-level pulse amplitude modulation (PAM2) is used. A lower voltage level corresponds to 0 and a higher level to 1. Also, because the pulse amplitude does not return to zero, PAM2 is often called non-return-to-zero (NRZ). To transmit data with a speed of 6Gbps with NRZ or PAM2 modulation, one bit time is 166.6667ps. In space, it spreads over about 2.5cm (about 1") in PCB type dielectric (Dk=4).

Four-level pulse amplitude modulation (PAM4) is becoming more popular as the data rates increase, and the required link bandwidth for PAM4 is smaller.² It uses four voltage levels to encode sequences of two bits: 00, 01, 10 and 11 (also called symbols). To transmit 112Gbps or 56GBd (GigaBaud)



FIGURE 1. PCB and packaging interconnect scale in bits for 6Gbps NRZ signal (top) and in symbols for 112Gbps PAM4 signal (bottom).

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with PAM4 modulation, one symbol time is 17.8571ps. In a PCB dielectric with Dk=4, one symbol spreads in space over 2.677mm (about 105 mil). To understand the scale of PCB and packaging interconnects, we can use the number of bits for PAM2 or symbols for PAM4 signal spreading over the length of the ideal link in the space domain (FIGURE 1).

The ruler in Figure 1 provides a scale in centimeters. A slowdown factor of two is used for the illustration of the spatial spread in a typical PCB dielectric with Dk=4. We can see at 6Gbps NRZ only a couple bits are simultaneously in the packaging part of interconnects (about 5cm or 2"), and about 10 bits are in the PCB part (about 25cm or 10") at the same time.

With the data rate increased to 112Gbps and PAM4 modulation used, we can observe about 20 symbols (40 bits for NRZ) over the package section of interconnects and about 100 symbols (200 bits for NRZ) in the PCB interconnects. The illustration in Figure 1 is for the ideal link, one without any kind of signal degradation. In real interconnects, the signals degrade. The degradation can be predicted with modeling or analysis or measured with scopes or vector network analyzers (VNAs).

Mathematically, it is easier to model the digital signal degradation in the frequency domain, assuming the time domain signal is a superpo-

Spectra and Bandwidth of High-Speed Data Signals

Let's look closer at the power spectral density (PSD) of 6Gbps NRZ signal with 50ps rise time for a pseudo-random bit stream PRBS7 (computed with Simbeor SDK) (FIGURE 2).

The signal in the frequency domain is a superposition of harmonics with rapidly decreasing magnitudes. Starting from about 5GHz, harmonic amplitudes are below -18dB. The contribution of such harmonics cannot be ignored. The spectrum has a minimum at 1/Tbit (the time for one bit or the unit interval) of 6GHz, but rises up to -18dB again.

The minimum bandwidth of a link to pass such a signal



FIGURE 2. A fragment of 6Gbps NRZ signal in time domain (left plot) and in frequency domain as the power spectral density in dB vs. frequency (right plot).



FIGURE 3. The insertion loss of the sample link (left). The power spectral density (PSD) of the incident signal shown in blue (stimulus). The PSD of the transmitted signal (response) shown in red (middle). The eye diagram (overlap of the pulses) shows the degradation of the ideal trapezoidal pulses (right).

sition of harmonics. (Harmonics are sinusoidal signals in time domain.) At this point, the analog problem in the time domain becomes the problem of harmonics in the frequency domain.

The first question is always what is the bandwidth of the signal in the frequency domain, and over what bandwidth should we have to model or measure it? To answer this question, we investigate what we would lose by neglecting the harmonics above the maximal bandwidth frequency. stop the frequency sweep? Should it be 0.5/Trise or 1/Trise? At this point, we do not have enough data to answer that.

The real signal does not have a linear rise time as used for the spectrum evaluation above. It is not generated like that, and even at the chip IO level, the lossy and dispersive interconnects smooth or filter the signal. The package may be very destructive too. So, for illustrative purposes, let's look at the spectrum of the same signal after it passes through 50cm

is defined by the Nyquist frequency (0.5/Tbit or 3GHz in this case).3 As demonstrated,1 accurate models or measurements must include the harmonics above the fundamental or Nyquist frequency. Otherwise, the observed or computed signal in the time domain would be significantly distorted. This is because the power in the signal harmonics above the Nyquist frequency is significant, and it will define the signal shape or distortion if not properly accounted for.

Notice most of the spectrum above the Nyquist frequency is in the microwave band. So, what should the bandwidth for the modeling or measurement for such signals be? Where should you (about 20") of PCB stripline interconnect. The insertion loss of such a link is shown on the left graph in **FIGURE 3**, and corresponding response spectrum is shown in the middle graph below (40GHz bandwidth).

Figure 3 shows the rise time increases, and there is deterministic (predictable) jitter due to the dispersion. (It is not jitter, but it is usually called that.) From the PSD plot, we can see considerable attenuation of the high-frequency harmonics. If the analysis must be done only for the transmission through the interconnect, it can be done with high accuracy over the same or smaller bandwidth. Although, to define the bandwidth we need to quantify the errors introduced by the bandwidth deficiency. As shown next, this can be done with the analysis of single-bit response.

The important point from this example is an interconnect reduces the magnitude of the signal high-frequency harmonics for better or worse, and it should be accounted for in the bandwidth identification.

PAM4 Signal Analysis

Next, let's look at the spectrum of a 112Gbps PAM4 signal. The TX, with 4ps rise time – a little optimistic – is computed







FIGURE 5. The insertion loss of the sample link (left). The power spectral density (PSD) of the incident signal shown in blue (stimulus). The PSD of the transmitted signal (response) shown in red (middle). The eye diagram (overlap of the pulses) shows the degradation of the ideal trapezoidal pulses (right).

up to 500GHz with Simbeor SDK (FIGURE 4).

If the upper frequency estimate, 1/Trise, looked reasonable in the case of 6Gbps (relatively easy to make models and measurements), it is completely unrealistic here. The Nyquist frequency = 0.5/Tsymb; it is 28GHz in this case. The analysis or measurement up to this frequency will be highly insufficient, as most of the signal power above this frequency will be unaccounted for. Notice the signal spectrum above the Nyquist frequency is in the mm-wave band (over 30GHz).

Fortunately, the spectrum changes dramatically when the PRBS signal shown in Figure 4 on the left passes through 25cm (about 10") stripline interconnect, as shown in **FIGURE 5** (500GHz bandwidth).

It is rather unfortunate. If you look at the eye diagram on the right, this is how a 112Gbps PAM4 looks when it passes through the 25cm of stripline on a typically designed PCB. It does not look good and requires additional signal conditioning to restore it.

So, what is the bandwidth for a 112Gbps PAM4 signal? Should it be a multiple of Nyquist or fraction of the inverse rise time? We still need to evaluate the consequences of the bandwidth restriction. Technically, we must evaluate the time

> domain signal distortion introduced by the spectrum harmonics above the bandwidth maximal frequency for a particular interconnect structure. As shown next, this can be done with the single-symbol response.

Complications to the Spectral Analysis of Ultra-High-Speed Signals

Here is what we have learned so far: The signal source spectrum (computed or measured) should define the bandwidth required for modeling or measurements, considering the expected channel insertion loss, including all kinds of losses: absorption, reflections and leaks. The signal

> degradation reduces the power in high-frequency harmonics and may reduce the required bandwidth as well. Though, such signal degradation and possible bandwidth reduction is unfortunate because it may degrade the signal up to the point of a complete link failure.

> One more thing contributes to the bandwidth. We have not discussed possible coupling or crosstalk. The model bandwidth must be adjusted to account for the spectrum of the coupled signals that

are not attenuated much at the near side (near-end crosstalk or NEXT, for instance).

Single Bit Response Numerical Experiments

There is a universal way to estimate the bandwidth with numerical experiments. First, compute the single bit response (SBR) of a 6Gbps NRZ signal passing through a 50cm stripline link. We use a 40GHz bandwidth as the benchmark and artificially restrict the modeling bandwidth to 3, 6 and 12 GHz and compare the SBRs (FIGURE 6).

The left plot in Figure 6 shows SBRs computed in Simbeor software with rational compact model (RCM) without the delay extraction. The RCMs are causal, but they approximate the original transmission parameter with high accuracy only up to the bandwidth maximal frequency (BW number on the plots above). The RCM does not delay or attenuate the signal harmonics above that frequency. The high-frequency harmonics appear as non-causal oscillations on the SBR. (Response comes before the expected time.) If we restrict the bandwidth to the Nyquist frequency 3GHz, the SBR will show noncausality with peak-to-peak voltage noise of about 40mV. That is over 10% of the benchmark SBR magnitude, computed with the sufficient bandwidth 40GHz. That value may be considered as the error measure due to the insufficient bandwidth. In fact, the insufficient bandwidth usually shows up in time domain as oscillations or other defects caused by a mishandling of the high-frequency harmonics. With the extension of the bandwidth up to 6GHz (1/Tbit), the error is reduced to 7mV, or about 2%, and the error is negligible with the bandwidth 12GHz. That is what the model or measurement bandwidth should be for this case, ideally.

Obviously, one can reduce the noncausality by the delay extraction procedure. If the RCM is built with the frontal delay extraction, the error due to insufficient bandwidth drops, as shown on the right of Figure 6. For the bandwidth 3GHz, the delay in RCM corresponds to the signal frontal delay at 3GHz. However, as we can see from the red curve on the right plot, the model delay is smaller than expected, and we can still see the oscillations caused by the high-frequency harmonics. Even if we somehow adjust the delay exactly to the value of the SBR delay, that will not save the day. The harmonics above 3GHz will distort the SBR in some way. One possibility to avoid it is to predict the signal attenuation above 3GHz. It may work for a simple transmission line segment, but it will not work for a link with discontinuities, as discussed in the next example. So, the answer for the bandwidth evaluated with the model with the delay is still about 12GHz. Further increase of the bandwidth does not significantly change the SBR.

Will it work for another type of interconnect? Unfortunately, no. The numerical experiment should be repeated. Also, the result of such a numerical experiment will depend on the software used to compute the SBR. It is important to validate the software first. Capabilities of a particular software can be evaluated with a similar numerical experiment. Compute SBR for a set of models with different bandwidths to see if the response converges with the increase of bandwidth. If software uses DFFT, increase the number of frequency samples to see if the SBR converges when the number of samples increases. Also, compare the result to SBR computed with a different tool.

Single Symbol Response Numerical Experiments

Single symbol responses (SSR) for the 112Gbps PAM4 signal discussed earlier and computed from S-parameters (left) measured for a 5cm (about 2") link are shown in **FIGURE 7**.

In this case, a 67GHz bandwidth is considered sufficient for SSR computation and used as the benchmark. It does not produce significant error (no visible noncausality in the SSR).



FIGURE 6. Single bit response (SBR) of a 50cm stripline link for the 6Gbps signal computed with different model bandwidths (BW) without the delay extraction (left plots) and with the delay extraction (right plots). dV is the error in SBR caused by the bandwidth deficiency.



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FIGURE 7. Magnitude and phase delay of transmission parameter of a 5cm stripline link (left). Single symbol responses (SSR) of the link computed with two different bandwidths (BW) and with and without the delay extraction. dV is the error in SSR caused by the bandwidth deficiency (middle). Eye diagrams computed with two different bandwidths (BW) and with and without the delay extraction (right).

That means the power in the high-frequency harmonics above 67GHz is not significant for this structure. If the bandwidth is reduced to 30GHz (a little over the Nyquist frequency), the error is about 40mV out of 420mV, or about 10%, for the model constructed with RCM and no delay extraction, and about 20mV (about 5%) with the frontal delay extraction.

The SSR pulse magnitude is closer to the expected magnitude with the delay extraction, but it is a coincidence. The rest of the SSR is different from the benchmark case. The stub effect appears on all three SSRs because the stub degrades not only the frequencies around the resonance at about 55GHz, but also at the lower frequencies (visible as oscillations of the insertion loss on the left plot). The stub is a capacitive discontinuity at the frequencies below the first resonance. Though, the stub effect looks smaller on the SSR with the insufficient bandwidth.

The eye diagrams for all three cases may look similar. (They are shown on the right of Figure 7, with the eye measurements computed with a Simbeor eye analyzer tool.) The eye diagram may not be suitable for a bandwidth-deficiency evaluation. We cannot reduce the bandwidth below 67GHz for this structure. Most likely, we have to increase the bandwidth for interconnects with smaller reflections (no stubs) and a smaller insertion loss. A numerical experiment should be the next step for a more definite answer.

Numerical experiments are important when deciding the bandwidth for PCB or packaging interconnect modeling and measurements. By building models with an excessive bandwidth, which requires only realistic transmission line models, and observing the effect of the bandwidth reduction on the simulated response, we can identify the minimum bandwidth for the system investigation before the signal is excessively distorted.

REFERENCES

- C.R. Paul, "Bandwidth of Digital Waveforms," EMC Society Newsletter, #223, 2009.
- R. Stephens, "PAM4: For Better or Worse Is PAM4 Worth the Hassle," SI Journal, Feb. 26, 2019.
- H. Nyquist, "Certain Topics in Telegraph Transmission Theory," *Transac*tions of the American Institute of Electrical Engineers, vol. 47, no. 2, April 1928.

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EMBEDDED RESISTOR Copper Foil for mmWave Applications

Embedded passives are being deployed for commercial market applications. by THOMAS SLEASMAN

Recent advancements in mobile technologies have exponentially increased demand for radio spectrum bandwidth. The rush of equipment for more RF applications is being deployed across the world, with 5G and millimeter wave (mmWave) communications expanding into the commercial space to take advantage of the wider bandwidth, higher data rates and low latency that these frequency bands offer. Cellular 5G and 6G, low Earth orbit (LEO), mid Earth orbit (MEO), geosynchronous communications networks, interconnected devices (internet of things), autonomous driving vehicles, defense and environmental monitoring are all driving these needs. The antenna and sensors necessary to manage the signals for these applications are similarly changing, becoming more sophisticated.

To ensure high-data-rate wireless connectivity, the broadband high-gain antennas necessary to manage high-frequency but lower-power signals are increasingly moving from dish and horn to flat-panel active electronically steered antennas (AESA) for beam forming and massive MIMO designs. In response, the RF industry has developed new integrated circuits, materials, processes and equipment to build devices to manage these mission-critical sensor applications.

Much of the development and understanding of how to engineer and build reliable and accurate transmit-and-receive sensors for today's environment were derived from phased array antennas and Ka/Ku-band radar engineering typically used in defense applications. The AESA products being developed can shape azimuth, elevation and antenna pattern as desired to generate beams that target specific communications devices.

Embedded resistor copper foils have a long history of applications in military/defense antenna systems and remain well positioned to support the design and manufacture of the flat-panel, PCB-based AESA antennas necessary to handle this expanded antenna paradigm.

As AESA technologies used in the defense and space sectors are deployed for commercial applications, designers who may not have broad experience in implementing systems with this technology are faced with a must-have list of printed wiring board concerns, including tighter routing, higher layer counts, maximum surface area for components, the lowest possible insertion loss and system-acceptable attenuation characteristics.

As 5G and mmWave communication are leveraged by the commercial marketplace, system architects and designers envision thousands of flat-panel AESAs discreetly mounted across the landscape. As frequency rises, so do the limits of the RF waves to travel through space, objects and variable environmental conditions. As a result, more antennas, repeaters and base stations are necessary to mitigate signal attenuation, coupled with lower power and shorter propagation distances at these short wavelength frequencies.

One antenna technology design option is using thin-film copper foil technology incorporating embedded passive materials. Embedded passives can be slimmed-down SMT components built and mounted into the inner copper and dielectric layers of the PWB laminate substrates. Embedding components allows designers to create smaller PCB/package sizes with better signal integrity and gain increased board surface space for active component mounting because of a more efficient wiring design. While components and mounting technologies are evolving to meet the challenges of discrete devices within PWBs, embedding thin-film-based resistors etched and formed within the copper foil traces leverages decades of effectiveness and robustness, no additional component buying and stocking, no extra handling and placement of components, elimination of wire bonding or solder processes within the depths of the PCB during the processes of multilayer build, and no cavity or added space requirements and potential component waste should the subsequent multilayer laminations go awry. Embedded thin-film resistors further enhance reliability of PWBs in part due to the aggressive sealing measures employed during the PCB's lamination processes.

Thin-film embedded resistors address many of the needs of SMT passive resistors, while providing additional value that can be factored into the overall completed PCB cost model. Given the PCB layers must have copper routing lines and spaces to move signals to and from active components, the resistor materials residing beneath those traces, while not free, are already in place to be used to lower PCB costs.

Due to the thin nature of embedded resistors (200-10000Å, 0.02-1.0 μ m), the resistors can be buried in innerlayers of printed circuit boards without increasing the overall thickness of the board. To do so, they employ internal cavities or occupy surface space for discrete SMT resistors (FIGURE 1). These resistor networks become part of the etched and printed circuitry on the standard PCB layers, thereby eliminating the need for passive SMT resistors and the many solder connections, bonding issues

> and routing vias servicing those components. Resistor foils are alternatives to traditional termination and pullup/

> down SMT resistors

and widely utilized for

balancing resistors in Wilkinson power divid-

ers. By removing discrete

SMTs from PCBs, inter-

connecting traces and

vias claim less room, so engineers can add other



FIGURE 1. Embedded passives can be placed in cavities and become part of the circuitry.

functions and reduce the PCB size for smaller, higher frequency applications and systems.

Millimeter and higher frequencies mean smaller and more tightly routed microstrip and stripline circuit designs and reliance on stable Dk and Df high-frequency PCB dielectrics, smoother, thinner copper foils, and other advanced technologies to limit signal degradation. Thin-film embedded resistive material technology offers a solution for many high-speed, low-loss, high-frequency applications where absolute performance and reliability are essential.

Designing with Embedded Resistors

Among the myriad design decisions that must be made – function, size, interconnection with other boards, laminate materials, thermal issues and components used – designers need to decide if they intend to use buried resistors at the frontend of the process.

The basic design concept for embedded resistors can be seen in the following equation:



EQ. 1.

where R_s is the sheet resistance of the resistor material designated as ohms per square (OPS).

The resistance value can be determined by material resistance and geometry of the resistor according to the formula above.



EQ. 2.

where *N* is the ratio of length to width or number of squares (N = L/W).

For a given sheet resistivity:

- Resistance of a square area equals the bulk sheet resistivity of the material.
- One square of $25\Omega/\Box$ material will equal 25Ω regardless of the size of the square.
- To create different resistor values with a given sheet resistivity, adjust the length-to-width ratio or number of squares.
 - For example, to create a 50Ω resistor using Rs of 25Ω/□ material, adjust the length to twice the width:



FIGURE 2. Resistance value is established in part by resistor geometry.

$$R = R_{s} \left(\frac{L}{W}\right) = R_{s} \left(\frac{2W}{W}\right) = 2 R_{s}$$

EQ. 3.

Resistors can be patterned as bar type using multiple squares and further arranged in a serpentine type of multiple squares. They can also be designed circular or form an arc.



FIGURE 3. Resistor patterns include a bar type with one (3a) or more squares (3b), as well as a serpentine pattern (3c).

Embedded resistor suppliers provide design tools in which the engineer can select resistance, power handling and tolerance to suggest the appropriate resistor dimensions.

Power dissipation, temperature rise and laminate substrate used all have an effect of the working life and long-term stability of the resistor. In general, the larger the resistor area the better, especially in designs where power and reliability are critical.

Manufacturing embedded resistors with resistive copper foil involves two print/image and develop steps and two or three etch steps, depending on the resistor alloys being used. Standard resistor alloys are nickel chromium (NiCr), nickel phosphor (NiP), silicon (Si), aluminum (NCAS) and chromium silicon monoxide (CrSiO). Considerations include the equipment setup for the photoresist application and subsequent exposure and development, as well as process control for selective copper removal to define resistor length. These processes can impact individual resistor tolerances. The inclusion of the resistive foil layer between the substrate and copper layer and the print and etch process steps result in resistors having customized ohmic values embedded inside PCBs after the PCB lamination process.

The OPS sheet resistance for sputtered and plated copper foils in roll form are controlled to a plus or minus 5% coefficient of variance value. The manufacturing process is calibrated using precise measurement and SPC guidelines. The roll-to-roll sputter and/or plated manufacturing produce a thin, continuous, conformal resistor alloy coating that mirrors the profile of the matte side of the copper foil. Trace width, conductor spacing and etch rates are predictable to maintain consistency with most modeling and design software. This eliminates the need for excessive iterative engineering to move from design to realized products.



FIGURE 4. The resistor in the ground plane requires an isolation area between the ground plane and the resistor. (Source: Ticer Technologies)

Embedded resistor foil products are available in roll form and customer-specified sheet sizes. Foils are produced at a 51" or 40" width cross-web standard, and production rolls are hundreds of LF in the down-web direction. This allows users to work with various combinations of dielectric laminate cores or PCB innerlayer layup processes. This flexibility allows users to scale to their preferred and most economical unit size. Foils come in a range of standard resistor options from 10 to 1000Ω per square bulk sheet resistance.



FIGURE 5. Processes for defining resistor elements. (Source: Ticer Technologies and Coretec)

As signal speed increases, so does the skin effect causing the electrical energy to move nearer to the surface of the copper traces in a PCB. At these higher speeds, roughness profiles and etching quality of embedded resistor foils are critical to achieve the best possible insertion loss characteristics. Furthermore, line, space and etched microwave structures like Wilkinson power dividers must become smaller to manage the wavelengths.

The final resistance tolerance is a function of delivered tolerance, the relative movement up and down in value during dielectric lamination (annealing effect) and the precision of the copper and resistive material etch processes of the PCB fabricator. Precise etching process controls repeatedly produce resistors with good tolerance.

Thermal Dissipation Factors

All aspects of the system's thermal dissipation must be considered in the PCB design. Factors that affect thermal dissipation in the system are circuit configuration; circuit thickness and material type; thermal conductivity of the dielectric; proximity of power or ground planes to resistors; ambient temperature; additional system cooling or heat sinking; and resistor size (total resistor area).

All electronic systems need to consider cost. This is particularly important as technologies developed for defense applications are adopted for commercial applications. Understanding the total system cost drives designers to consider options, including embedded passives. Designers need to consider tradeoffs, such as using thin-film embedded resistor foils to place most or all of the resistor networks on a layer or two inside the board in place of SMT components. They need to decide if reserving more surface real estate, simplified packaging and improved signal integrity by using embedded resistor foils would lower the overall cost of the system vs. standard SMT devices. □

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Revamping the SMTA MINIATURIZATION TEST VEHICLE

Rev. 3.0 will incorporate user input. What should be on the next layout? **by CHRYS SHEA**

The current SMTA Miniaturization Test Vehicle was released in 2018 and is projected to have an effective lifespan of three to five years. Its design has served the SMT community well – and will continue to do so with an updated layout, bill of materials (BoM) and associated programming and analysis files slated for release in late 2022.

The board is used for standard tests, such as solder paste selection, wipe frequency and pad or aperture design, which will remain the same in the new revision, albeit with some components removed and others added. FIGURES 1 AND 2 show the top and bottom sides of the board with the footprints that *will* be removed outlined in orange, and ones that *may* be removed outlined in blue:

- The 1206 and 0603 components will be completely eliminated, opening up several square inches of real estate on the populated side of the board.
- The QFN layout will avoid copper pads on the opposite side to make x-ray analysis easier.
- The SIR coupon will be removed, thereby eliminating the need for the gold fingers on the short edge of the board, which in turn will eliminate the notch that requires machine board stop adjustments for the unpopulated side. It will also free up about 6 sq. in. of real estate for print or reflow tests.
- At least one set of the fine resolution spread tests will be removed, freeing up even more space on the unpopulated side. With all the newly available real estate, what will we add



FIGURE 1. SMTA Miniaturization Test Vehicle populated side.

to the board? That's up to the SMTA community. What do users want on the next layout? Here are some ideas we've received so far:

- More pad and aperture sizes for 01005s; built-in DoEs.
- More pad and aperture sizes for 008004s; mask-define some 008004s and build in DoEs.
- D-paks for voiding tests.
- 0.4mm TSSOPs.
- More BTCs of different sizes; thermal vias in center pads.
- Stagger BGA layouts to mitigate "leading-edge effect."
- More 0.3 BGA pad configurations.
- Rotational placements at various angles.
- LED footprints.
- Areas to dispense and measure adhesives or other additive materials.
- Cu pillar flip chips.

Should the 0402s stay or go? What about the wet bridge test patterns? I'm asking for user input through the month of May, and layout efforts will begin this summer. SMTA Rev 3.0 is planned to make its debut Oct. 31 - Nov. 3 at SMTA International 2022 in Minneapolis.

Have some ideas? Email me at chrys@sheaengineering. com. I look forward to hearing from you. □

CHRYS SHEA is president at Shea Engineering Services (sheaengineering.com); chrys@sheaengineering.com.



FIGURE 2. SMTA Miniaturization Test Vehicle unpopulated side.

The Risks of Electronic Hardware Exposure to DISINFECTANTS

Case studies show cleaning the workplace can harm materials and equipment. by TERRY MUNSON and PHIL ISAACS

During the pandemic, cleaning and disinfecting common areas and surfaces to protect and remove the Covid-19 virus and all other viruses and bacteria has become urgent. During this time manufacturers have turned to professional cleaning services or have assigned facilities departments the responsibility of properly disinfecting areas. Adding corrosive chemicals to the working environment is a new condition. While the CDC issued guidelines for human exposure and documented the timing and conditions when workers can return to a work area after fogging, spraying and disinfecting, it missed the under-

standing and risk of contamination these corrosive chemicals can cause to exposed electronic hardware, components, material in production and production equipment. Below are case studies showing the chemical effects and residue patterns negatively impacting hardware and operating conditions.

As the pandemic altered our world, we learned and isolated in ways we never expected. As the SARS-CoV-2 virus spread, manufacturing facilities closed worldwide to help slow the spread of the disease. Scientists and engineers sought methods to safely reopen factories, prioritizing the effectiveness of disinfecting methods for the health and safety of the employees. Possible reliability impacts to electronic products and equipment were typically not of highest consideration. The initial unknown nature of the virus, its mode of spread, and length of time it lives on surfaces resulted in a need to apply disinfecting agents to the environments where people are exposed to other people.

Wearing masks and isolating proved effective at reducing the spread, but there's another side to disinfecting the areas where people work, live and play to allow the store, diner, office and manufacturing centers to return to normal operations. Many professional services offer disinfecting and cleaning for virus reduction, and they are easy to find and schedule (FIGURE 1). It is an important health and safety issue that all areas are cleaned and disinfected – all common spaces and working surfaces that put people at risk for exposure to



FIGURE 1. Aerosolized disinfecting surface treatment of workstation.



FIGURE 2. CFD airflow and heating of PC controller.

the virus, but the risks should be understood.

Those who professionally disinfect areas wear protective clothing and respirators designed to eliminate the risk of exposure, and they disinfect when people are not present. Again, they are following the chemical/equipment manufacturing requirements for broadcasting disinfectants, many of which are corrosive chemicals.

There are sprayers, foggers, application spray bottles and wipes for surfaces. Each method permits deposition and volatilization of chemicals over time. Most disinfectant applications are not applied directly on electronic hardware, but because of the complexity of these operating electronic systems, they may have draw-fans pulling air across the system to cool operational components (FIGURE 2). This air intake path allows airborne contaminants to be deposited on electronics.

When electronics manufactur-

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FIGURE 3. Aerosolized disinfecting surfaces. The lack of specific control over the fog ...



FIGURE 4. ... means surface residues are deposited randomly ...



FIGURE 5. ... and sit until the units are powered up.



FIGURE 6. Ultra-low-volume fogging.



migration (shorting) and corrosion issues.

the area is disinfected (FIGURE 4).

FIGURE 7. Ultra-low-volume fogging machine.¹

Case Study #1: Field Failures

ing facilities are fogged to cover large areas where electronic hardware is being produced, these pre-functional systems are exposed, and these surface residues are deposited and sit on surfaces until the units are powered up in the field (FIGURE 3). The effects of these residues pose a great risk of parasitic leakage, electrochemical

When fogging large production areas and office locations, airborne disinfectants not only travel to the general locations but are drawn into the HVAC air handling systems, redepositing this contamination throughout the system. (Air filters will capture the initial microdroplets, but as they dry the chemicals outgas and are delivered to working areas as gases onto electronics.) Even when hardware is tented or covered during fogging, the risk of contamination to hardware and systems grows every time

> In the first case study, medical areas with tented equipment in surgical suites fogged with disinfectant to remove bacterial, viral and biological contamination created a sterile environment for patient and staff protection (FIGURES 5, 6 AND 7). The use of an aerosolized disinfectant is an effective, fast method of applying the disinfectant (typically a corrosive residue) to large areas, but each professional person is well protected by personal protective equipment (PPE).

> In this case, we show data on equipment in the tented suites in standby and ready-for-use states. The electronic equipment was tented with surgical draping cloths and was not exposed directly to the disinfectant fog (stationary units to fog the entire room), which ran for 15 minutes, then was allowed to sit for 15 minutes before people could reenter the room. The functional prob-



FIGURE 8. PCBA 1: four fogging cycles, exposure on the bottom side of the PCBA.



FIGURE 9. PCBA 1: two fogging cycles, exposure on the bottom side of the PCBA.

lems in this case appeared after one or two fogging exposures created by the moisture-laden disinfectant floating throughout the space.

Exposed hardware from the surgical suite – 30 days in the field with four exposures and two exposures of fogging – was compared to current production samples (FIGURES 8 AND 9). Hardware failed in a critical respiratory control system (TABLE 1).



FIGURE 10. PCBA 1: four fogging cycles, disinfectant exposure on the bottom side of the PCBA with cooling fans showing high chlorine residues from debris on top of resistors (not from process residue) (no-clean = WOA)).



FIGURE 11. PCBA 1: two fogging cycles, disinfectant exposure on the bottom side of the PCBA with cooling fans showing high chlorine residues from debris on top of resistors (not from process residue) (no-clean = WOA)).



FIGURE 12. Hardware exposed to fogging ...



FIGURE 13. ... experi-



FIGURE 14. ... up to five days later.

Upon review of the localized extraction results and electrical test, new hardware exhibited acceptable residue levels and good, "clean" C3 results. The two field samples with different exposure (fogging) cycles experienced catastrophic failures and were returned for failure analysis. (These are real field applications, not experiments.) The resulting failed hardware in the field led to corrosion due to external contamination caused by

the exposure from fogging with an aerosolized disinfectant.

Case Study #2: ICT Failures

Hardware in production and engineering areas was exposed to fogging. The samples experienced ICT and functional testing failures two to five days after fogging the production area (FIGURES 12, 13 AND 14). Each of the areas was inside a 50,000 sq. ft. production facility and selected in relation to the main aisle fogging areas.

Inspection of the areas showed no visible signs of fluid on the floors and rack surfaces, but small droplets appeared on box surfaces three days after fogging. The ESD plastic trays and tops of components showed tiny dry spots on the surfaces that were open, but not on the samples below the top layer. The residues of the disinfectant chemically matched the residues on the trays and top layer of the PCBA surfaces (TABLE 2). These residues are corrosive and moisture-absorbing after they dry.

Case Study #3: RF Product Corrosivity

For high-reliability and RF products, even small amounts of parasitic leakage can cause a change in impedance of the circuit, causing undesirable results. Exposure of the work area to fogging while the PCBAs were a work-in-progress prior to potting in silicone for ruggedization caused long-term impedance changes in the circuit that were only brought about through temperature cycling in end-use after several months.

Board inspection showed no visible residues from the fogging, and resistivity of solvent extract (ROSE) testing at a full board level showed an acceptable amount of ionic contamination as a result of the large surface area being measured. The contamination was at a level in which the corrosivity was not enough to be detrimental to the PCBA in the short term. Therefore, the issue was not caught during ICT or functional testing.

Although tenting WIP trays was done at the manufacturing site, only the top and most of the sides were covered, leaving some

TABLE 1. Ion Chromatography – Case Study #1

			lo	n Chro	matogra	phy (C)ionex l	CS 300	0 at Fore	site) n/	a = not	appli	cable						C3	Tester
	Sample Description	Fluoride	Acetate	Formate	Chloride	Nitrite	Bromide	Nitrate	Phosphate	Sulfate	W0A	MSA	Lithium	Sodium	Ammonium	Potassium	Magnesium	Calcium	Results	Time (Sec)
Fores for Pl	ite Recommended Limits CBA (No-Clean - SMT)	1	3	3	6	3	6	3	3	3	25	1	3	3	3	3	n/a	n/a	Clean	>120
ID	PCBA from Production, Not in	the Fie	eld																	
1	Area 1 Microprocessor Leads	0	0.52	0	0.45	0	0.34	0.05	0	0.98	18.65	0	0	1.51	0	0	0	0	Clean	180
2	Area 2 Capacitor SMT	0	0.35	0	0.69	0	0.54	0.03	0	1.34	15.36	0	0	1.69	0	0	0	0	Clean	180
3	Area 3 Open Solder Mask area	0	0.11	0	0.54	0	4.65	1.74	0	0.32	1.05	0	0	1.36	1.63	0	0	0	Clean	180
4	Area 4 DIMM Memory Module	0	0.29	0	1.25	0	3.88	1.24	0	0.24	12.33	0	0	1.41	2.26	0	0	0	Clean	180
	PCBA #1 from Field 30 Days (e	xpose	d to 4 fo	gging	cycles)															
5	Area 1 Microprocessor Leads	0	15.24	0	28.98	0	8.65	12.34	0	21.31	15.65	0	0	11.58	14.24	0	0	0	Dirty	1
6	Area 2 Capacitor SMT	0	9.24	0	91.24	0	9.65	10.25	0	41.25	14.24	0	0	17.10	16.69	0	0	0	Dirty	1
7	Area 3 Open Solder Mask Area	0	10.27	0	15.64	0	1.24	5.68	0	9.54	0.52	0	0	11.58	21.24	0	0	0	Dirty	1
8	Area 4 DIMM Memory Module	0	16.35	0	21.41	0	6.35	9.98	0	15.66	10.14	0	0	17.10	18.92	0	0	0	Dirty	1
	PCBA #2 from Field 30 Days (e	xpose	d to 2 fo	gging	cycles)															
9	Area 1 Microprocessor Leads	0	8.54	0	13.65	0	4.65	4.62	0	12.35	12.35	0	0	7.98	8.54	0	0	0	Dirty	1
10	Area 2 Capacitor SMT	0	6.98	0	41.21	0	3.88	3.21	0	24.68	9.98	0	0	13.32	14.68	0	0	0	Dirty	1
11	Area 3 Open Solder Mask Area	0	8.57	0	8.22	0	4.65	2.69	0	5.10	0.44	0	0	10.21	12.24	0	0	0	Dirty	1
12	Area 4 DIMM Memory Module	0	6.44	0	11.72	0	3.88	3.21	0	7.17	10.65	0	0	9.98	13.36	0	0	0	Dirty	1
13	Liquid Disinfectant Dried on Foil for Shipping	0	121.41	0	231.54	0	0.22	11.24	0	148.54	10.65	0	0	81.35	101.27	0	0	0	Dirty	1
All Val	ues in ug/in ²																			

units much more exposed and prone to future failure compared with other units processed at the same time. The photos show the cart tops were tented, but ESD work surfaces were not, creating a transfer point. Disinfectants do not negatively impact ESD but are easily transferred with direct board contact to the ESD mats or tools.



Samples tested by localized (sitespecific) extraction showed poor, "dirty" C3 performance, and three

stages of new build production.

samples from a cycle within three days of fogging showed the same chemical signature as the disinfectant that was fogged. The samples with high levels of contamination were field return samples, while the others were from different

Case Study #4: Design of Experiment

Since disinfecting near or around electronics has become a common periodic event to prevent normal workers from virus exposure, it is time to understand the environmental effect on electronic performance caused by these methods of disinfecting. This case study analyzes the deleterious effects of common chemicals used on and near electronic systems when delivered with ultra-low-volume (ULV) fogging systems. The analysis includes surface insulation resistance (SIR) of test boards with four test locations per board with no-clean flux residue on the assembly and local ionics testing the mobility of the ions present.

Chemicals for fogging included hypochlorite; hydrogen peroxide; IPA; ben-



FIGURE 16. Workbenches not covered, and open racks exposed on lower shelves.



FIGURE 17. SIR test board, pre-test.



FIGURE 18. SIR test board in draw box.



FIGURE 19. SIR test board with ULV fogger.

TABLE 2. Ion Chromatography – Case Study #2

zalkonium chloride 13%; thymol oil (botanical disinfectant and fungicide); control (not exposed).

Findings. The samples exposed to fogging with a draw-fan permitted residues from the disinfectant to create deposits on the surface of the test coupons, which failed SIR testing for the hypochlorite, hydrogen perox-



FIGURE 20. PCBAs 1 (top left); 2 (top right); 3 (middle left); 4 (middle right); 5 (bottom left); 6 (bottom right).

ide, benzalkonium chloride and thymol oil. All disinfectants were diluted with tap water, which is the recommended dilution material for the ULV foggers. The IPA and control with no exposure both showed good, passing SIR results. When this location was assessed by localized extraction and tested by ion chromatography, it showed corrosive effects as well on the four chemicals that failed SIR. The resi-

	Ion Chromatography (Dionex ICS 3000 at Foresite) n/a = not applicable														Localized Test					
	Sample Description	Fluoride	Acetate	Formate	Chloride	Nitrite	Bromide	Nitrate	Phosphate	Sulfate	W0A	MSA	Lithium	Sodium	Ammonium	Potassium	Magnesium	Calcium	Results	Time (Sec)
Fores for P	ite Recommended Limits CBA (No-Clean - SMT)	1	3	3	6	3	6	3	3	3	25	1	3	3	3	3	n/a	n/a	Clean	>120
ID	Hardware Inside a Box Seale	d																		
1	Area 1 Outside of Box on Plastic Label	8.65	12.54	0	125.88	0	0	13.28	0	104.24	0	0	0	241.19	0	0	0	0	Dirty	1
2	Area 2 Inside Box on ESD Bag	0	0.15	0	2.34	0	0	0.41	0	1.55	0	0	0	2.71	0	0	0	0	Clean	180
3	Area 3 Inside Box on PCBA Capacitor SMT	0	2.14	0	1.71	0	1.54	0.16	0	2.41	12.39	0	0	1.04	0.35	0	0	0	Clean	180
4	Area 4 Inside Box on PCBA #2 Capacitor SMT	0	1.87	0	1.46	0	1.27	0.22	0	1.97	10.41	0	0	1.71	0.27	0	0	0	Clean	180
	Hardware on Production Rac	k 3 Day	s after	Foggin	g															
5	Area 1 Empty Tray	10.21	21.35	0	74.21	0	2.14	10.88	0	26.98	0	0	0	184.65	0	0	0	0	Dirty	1
6	PCBA #1 Capacitor SMT	15.24	18.64	0	82.14	0	1.81	11.24	0	31.24	10.24	0	0	163.25	0.65	0	0	0	Dirty	1
7	PCBA #2 Capacitor SMT	19.65	21.41	0	74.61	0	1.24	10.21	0	29.11	12.15	0	0	174.24	0.36	0	0	0	Dirty	1
8	PCBA #3 Capacitor SMT	12.35	14.24	0	63.26	0	1.07	8.55	0	24.65	9.98	0	0	144.27	0.31	0	0	0	Dirty	1
9	Area 2 Empty Tray	3.65	5.24	0	21.35	0	0	3.29	0	10.24	0	0	0	64.25	0	0	0	0	Dirty	1
10	Area 3 Empty Tray	7.19	8.51	0	41.78	0	0	3.21	0	16.88	0	0	0	101.24	0	0	0	0	Dirty	1
11	PCBA #4 in Tray Area 3 Capacitor SMT	9.74	9.74	0	63.54	0	1.25	7.94	0	10.27	12.32	0	0	94.65	0	0	0	0	Dirty	1
12	PCBA #5 in Tray Area 3 Capacitor SMT	8.81	6.44	0	54.21	0	1.11	8.11	0	12.04	15.34	0	0	102.41	0	0	0	0	Dirty	1
13	Liquid Disinfectant Dried on Foil for Shipping	121.41	85.65	0	541.57	0	0	121.65	0	265.54	0	0	0	1184.30	0	0	0	0	Dirty	1
All	/alues in ug/in ²																			

TABLE 3. Ion Chromatography – Case Study #3

				lon (Chromat	ograpl	hy (Dion	ex ICS	3000 at F	oresite	e) n/a =	= not a	pplica	ble					C3 Teste	er
	Sample Description	Fluoride	Acetate	Formate	Chloride	Nitrite	Bromide	Nitrate	Phosphate	Sulfate	W0A	MSA	Lithium	Sodium	Ammonium	Potassium	Magnesium	Calcium	Results	Time (Sec)
Fores for B	ite Recommended Limits are Boards	3	2.5	2.5	2	2.5	2.5	2.5	2.5	3	n/a	0.5	2	2	2.5	2	n/a	n/a	Clean	>120
Fores for Pl	ite Recommended Limits CBA (Clean)	1	3	3	6	3	6	3	3	3	25	1	3	3	3	3	n/a	n/a	Clean	>120
Fores for Pl	ite Recommended Limits CBA (No Clean)	1	3	3	3	3	6	3	3	3	150	1	3	3	3	3	n/a	n/a	Clean	>120
ID																				
1	Vial C5038	0	0	0	0.12	0	0	0.84	0	0.12	2.18	0	0	0.21	0	0.01	0	0.09	Clean	180
2	Vial C6F05	0	0.16	0	0.40	0	0	0.11	0	0	0	0	0	0.23	0	0.02	0	0	Clean	180
3	Vial C781B	0	1.05	0	0	0	0	0.01	0	0	0.55	0	0	0	0	0.01	0	0	Clean	180
4	Vial C9E34	0	14.79	5.42	10.99	0	161.27	0.03	0.44	3.30	21.47	0	0	0.76	3.02	9.04	1.32	1.64	Dirty	51
5	Vial C9235	0	0.11	0.69	0.11	0	0	0.04	0	0	0	0	0	0	0.28	0.01	0	0	Clean	180
6	Vial C4519	0	1.32	0	0.42	0	0.19	0.65	0	2.17	2.54	0	0	1.18	1.27	1.30	0.92	0.42	Clean	180
7	Vial CAD1A	0	1.53	0	0.71	0	1.51	0.20	0	0.65	1.64	0	0	0.13	0	0.31	0.02	0.38	Clean	180
8	Vial CAC06	0	2.25	0	0.95	0	1.24	0.13	0	1.09	1.59	0	0	0	0	2.21	0	0.02	Clean	180
9	Vial CABC8	0	1.31	0	0.83	0	4.68	0.10	0	0.42	0	0	0	0.22	0	0.25	0	0.50	Dirty	92
10	Vial CACF8	0	2.11	0	1.83	0	15.24	0.04	0	1.01	1.16	0	0	0	0	1.41	0.05	0.66	Dirty	8
11	Vial CADA6-X1	0	13.48	4.90	15.84	0	132.97	1.02	0.81	15.37	286.06	0	0	7.06	1.69	5.31	6.91	11.38	Dirty	29
12	Vial CADA9-D2	0	8.35	2.55	3.56	0	68.06	0.52	0.03	3.94	12.28	0	0	2.05	1.19	4.40	0.23	3.37	Dirty	53
Adde	ndum Samples - Disinfect	lant																		
13	Sample A - Undiluted	0	136.81	71.42	13.332	0	0	5.07	0	27.64	0	0	0	5.523	0	62.11	8.80	13.35	Not Tested w/C3	
14	Sample B - Diluted 128:1	0	0.89	0.43	83.11	0	0	0.17	0	0.75	0	0	0	41.40	0	0.04	0.80	2.99	Not Tested w/C3	
All V	/alues in ug/in ²																			

due levels of these chemicals showed a large deposit of contamination from the tap water, as well as the disinfectant chemicals. The IPA showed a good, clean, localized test and passing SIR, as did the control. These corrosive residues collect on surfaces and set up corrosion cells, causing intermittent performance and failing hardware in the areas where fogging occurs.

Conclusions

Surface disinfecting to reduce the presence of viral and bacterial contamination is a critical process to create safe workplaces, but as hospitals have consistently proved, when a broadcast aerosol method is used indoors, the risk of contamination vs. disinfecting becomes a long-term problem. Aerosolized appli-



FIGURE 21. PCBA 1, case study #3: as received, not powered.



FIGURE 22. PCBA 1, case study #3: exposed to fogging.

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Stable operation of equipment and improvement of productivity

Elimination of teaching deviation between operators and reduction of human error



TABLE 4. Ion Chromatography – Case Study #4

		lon C	hromate	ography	(Dione	CICS 3	3000 at F	oresit	e) n/a = r	not app	icable	!				Locali	zed Test	SIR Testing Results
	Sample Description	Fluoride	Acetate	Formate	Chloride	Nitrite	Bromide	Nitrate	Phosphate	Sulfate	W0A	MSA	Lithium	Sodium	Ammonium	Results	Time (Sec)	168 hr. 40°C/90%RH
Fore: for P	site Recommended Limits CBA (No-Clean - SMT)	1	3	3	3	3	6	3	3	3	25	1	3	3	3	Clean	>120	Good Passing >1.0e8 ohms
ID	DOE Fog Exposure (All Di	lutions	were I	Made w	ith Tap	Wate	r)											
1	Sample 1 - Hypochlorite	3.91	15.65	0	81.24	0	6.65	0	0	23.65	0	0	0	28.65	0	Dirty	1	Failed - Limited at 1.0e6
2	Sample 2 - Hydrogen Peroxide	3.26	4.68	0	9.24	0	3.16	0	0	2.16	0	0	0	6.65	0	Dirty	104	Failed - Limited at 1.0e6
3	Sample 3 - IPA	2.51	2.11	0	4.21	0	1.64	0	0	2.09	0	0	0	2.11	0	Clean	165	Pass 2.1e9 ohms
4	Sample 4 - Benzalkonium Chloride (13%)	3.63	4.81	0	113.15	0	9.87	0	0	36.35	0	0	0	41.24	0.27	Dirty	1	Failed - Limited at 1.0e6
5	Sample 5 - Thymol oil	2.39	11.36	0	11.78	0	3.65	9.54	0	12.14	34.65	0	0	22.31	0	Dirty	57	Failed - 4.2e7 ohms
6	Sample 6 - Control (No Exposure)	0	0.74	0	0.51	0	0.41	0	0	1.41	0	0	0	1.17	0	Clean	180	Pass 8.9e10 ohms
All	Values in ug/in ²																	

cations cover a large area but contaminate racks, trays, bins, boxes and equipment used in and on production hardware. This method puts disinfectants in areas where few viruses or bacteria are present: shelf tops, boxes, pallets, inside electronic equipment and on production hardware.

HVAC systems also pull the disinfectants into the system, dispersing them back into the environment, impacting these areas, even when not directly sprayed. Manufacturing offices and common areas require good air purification to reduce microdroplet exhalation from coughing and sneezing using UVC and air-purification systems, along with face coverings that dramatically reduce these risks. Using approved sprays and wipes, such as hydrogen peroxide or alcohol-based materials, reduces the viral load and permits better ways to protect workers and electronic hardware.

Creating a safe workspace should include a clear plan for worker safety but not at the expense of the equipment, product or working systems. There are times and places for broadcast aerosol disinfecting, but with planning, organization and understanding the corrosive nature of many of the disinfectants, the workplace can be safe and fully functional without creating a corrosive air-quality environment.

These case studies show a direct correlation to the application of disinfectants in or around production hardware. We must understand and qualify the workplace environment during production and WIP for electronic hardware, equipment used in production and testing, and all surfaces with which hardware will come in contact. These performance issues are not related to the electronics assembly process but the exposure to corrosive contamination from the disinfecting environment.

REFERENCES

- K. Middleton, Ph.D., "Cleaning and Disinfecting: Whole Room Fogging," *Cleanroom Technology Online*, Jun. 1, 2020.
- Ed.: This article was first published at the SMTA Pan Pacific Microelectronics Symposium in January 2022 and is republished here with permission of the authors.

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FIGURE 23. Four fogging cycles. Exposure on the bottom side of the PCBA.



FIGURE 24. 4 ULV fogger.

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VANGUARD EMS: Manufacturing the Smarter Way

Integrated flying probe testers and in-house MES have the EMS firm leading the pack. by MICHAEL L. MARTEL

Vanguard EMS is one of the largest locally owned electronics manufacturers in the Pacific Northwest, with a 77,000 sq. ft. facility near Portland, OR. The company specializes in high-reliability electronics products for the medical, aerospace and defense, and infrastructure/industrial sectors. Some 70% of the firm's customers are Fortune 500 companies. Founded in 1988 by Tektronix alumni, the company grew steadily and was acquired in 2003 by Floyd Sutz, Vanguard's CEO and an employee since 1995.

"Basically, everything we build has a high cost of failure, especially out in the field," said Chris Smith, director of sales. "Defense and aerospace, for example, are about 55% of our business. Medical is probably about 25%, and for those industries, these are products that are in the top five or 10% as far as difficulty is concerned. That's a high level, and yet this year we will be marching up to about \$70 million annually." In addition to circuit boards, many products are high-level assembly and box-build. Indeed, Vanguard is the FDA manufacturer of record for two final devices the firm produces from component assembly to the system level. That means Vanguard is permitted to ship directly to its customer's customer."

Because Vanguard's origins lie with ex Tektronix engineers, test has been "part of our DNA" since the beginning, says Smith. "I don't think there's anybody on the West Coast who has test capability like we do. One of our primary goals is to limit defects for the customer. We want to dramatically reduce or eliminate time spent in the defect discovery and repair and retest cycle. There's a lot of waste around that."

"We evaluated several manufacturing execution systems and found they were targeted more toward OEMs or manufacturers with fewer products and fixed flows," said Joe Lariz, director of IT, and Anh Vu, director of manufacturing, via

> email. "We needed a system that was flexible vs. fixed, and we did not want to take time trying to fit a square peg into a round hole. In addition, we wanted a system where our employees could get everything they need, as opposed to having to go to an MRP system, document control system and a shop floor control system. We spent months interviewing our frontline employees, asking them, 'What do you need to do your job effectively?' This was the beginning of SMARTer Manufacturing.

"We did not find [off-the-shelf platforms] to be very adaptable for our ever-changing customer needs, and [we weren't able] to easily adjust to multiple quality standards and specific customer requirements. In addition, we needed to be able to make it impossible to err in meeting standards and



FIGURE 1. To meet stringent quality demands, Vanguard EMS seeks optimum flexibility in manufacturing capability and capacity.

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customer requirements."

Enter SMARTer Manufacturing. That's the name for Vanguard's proprietary process flow and MES. According to Smith, "SMARTer was designed from the ground up by our team members exclusively for electronics manufacturing. It's our no-compromise approach to building high-quality, reliable devices with comprehensive traceability."

The novel MES (FIGURE 2) began as a database that tracked every part, test and failure. Vanguard hired dedicated software engineers and programmers to develop the MES, and modeled its software validation program after AS9100 requirements. The initial rollout phase took around 12 months from start to production release, and the system has been in place since 2007. By incorporating feedback from engineers



FIGURE 2. A Vanguard EMS employee works within the novel SMARTer MES.



FIGURE 3. Vanguard staff use Takaya APT-1400F series flying probe testers.

and technicians who use it, Vanguard engineers continue to refine and improve it.

Today, the entire Vanguard EMS production facility is controlled through the novel MES. Beyond device records and tests, the MES governs who can work on a customer's devices; whether technicians have been appropriately trained; what tool, equipment or process has touched each device at every stage of manufacturing and more.

"Vanguard team members are unable to open customer documentation at their workstation, unless their ESD heel straps and wrist straps pass, and all their training records are up to date and support all quality standards and customer requirements. This is all managed in the barcode of their employee badge and through an extensive plantwide barcod-

ing system," said Lariz and Vu.

To complement its MES, Vanguard uses INFOR Fourth Shift MRP and Agile PLM, which links directly to SMARTer.

Passing the Test

Two Takaya APT-1400F series flying probe testers are key resources in the SMARTer system (FIGURE 3). These testers meet the company's requirements for accuracy, speed and flexibility better than ICT fixtured testing, Vanguard says. Flying probe testers are used when there isn't time to wait for an outside vendor to produce bedof-nails test fixtures, or the product isn't at the volume or maturity for ICT.

"Flying probe testing is the most flexible tool to perform verification of product build to specification," said Roy McKenzie, Takaya Group manager. "On average, you're creating a test program in one to two hours from CAD. You're going through a debug process that is six to 12 man-hours, depending on the board. If it's a very complex, very large board, it can take a week, but happily, there's no additional hardware required in your board testing.

"Generally, our flying probe tester customers are testing boards within one to three days once they get the first board off the line because they've already developed a program in advance. They are already prepared in that they have the CAD, the bill of materials and the schematics. The program is ready by the time they get that first board. At that point, they can debug the program. Once that's done, they're ready to proceed. Additionally, engineering change orders are very easy, unless there's been a major change in the actual board itself.

"Basically, you're going into software and saying, 'Okay, this capacitor is now X



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value instead of Y value.' Verification is quick. The interval is one to three days to testing, a comparatively short period of time and the shortest in test technology today. If you're going to do any kind of testing in an automatic test environment, flying probe testing is the fastest from zero to testing your lot. As an example, should an ECO come down before the build with fixtures, you'll have to modify that fixture before that build occurs. But conversely, with flying probe testers, you don't have to worry about that. You can make a change the day of the build because it's a simple software change."

"Timing is essential to the SMARTer system," Smith added, "because we're tracking defects throughout the entire process, and we can because we have test and inspection equipment throughout the entire assembly process. As a result, a defect with our SMARTer Manufacturing system is not allowed to make it to the next step without being taken care of at the step where the defect is found. A defect found at the surface is addressed at that point; it's taken care of, and that reduces the number of defects overall. When we get to final testing, I can go to our [MES], pull up an assembly and find all the defects related to that assembly, and I can even zero-in on the actual solder joint where that defect occurred. We then have a list of defects our employees can pick. They're all working from that list. 'What component is it? What pin is it?' We've got that information right at our fingertips, and the further upstream we can locate these defects and correct them, the better. Whenever the team launches a new kit to the floor, they look at all the defects that happened in the kit prior, and all those get flagged in the system for elimination as much as possible in the next run."

Many of the military products Vanguard builds are, by their nature, constantly evolving – changes in design or "WHEN A NEW KIT IS LAUNCHED TO THE FLOOR, THEY LOOK AT ALL THE DEFECTS THAT HAPPENED IN THE KIT PRIOR, AND THOSE GET FLAGGED FOR ELIMINATION IN THE NEXT RUN."

delivery and traceability of components, supplies, tools, people and recipes are non-negotiables in the world of high-risk electronics. At Vanguard EMS, their manufacturing tools and processes are designed to meet these high standards.

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engineering ordered by the customer, Smith says. As such, they are never stable enough to make economic sense for bed-of-nails testing. Engineering changes in bed-of-nails testing cost a lot of time and sometimes a reasonable amount of money - to change the software, fixture and any hardware requirements.

"If you've got a mature product, you're ready to go; if you don't, you generally don't do this because it's not practical," Smith said.

Device quality, reliability, on-time



FIGURE 4. Flying probes can test the top and bottom of a PCBA.



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'Why' Lean Six Sigma?

Lean Six Sigma training leads to effective, intrinsic problem-solving.

MUCH HAS BEEN written on the "how" of Lean Six Sigma. This column discusses the "why" behind Lean Six Sigma. SigmaTron's facility in Tijuana, Mexico, began implementing its Lean Six Sigma program in 2018 as a way to instill a focused process improvement methodology in its automotive and medical customer projects. A consultant was brought in for initial training, and I volunteered to be the internal champion after agreement that the necessary management support and resources would be put in place. The initial training sessions were designed to train the engineering team as Green Belts and select production personnel as Yellow Belts.

One challenge in an electronics manufacturing services company is each customer has control of their design. While some incorporate EMS-driven design for manufacturability (DfM) recommendations, others do not. Although SigmaTron's production personnel wanted to solve production problems as they arose, the root causes were often difficult to identify using basic quality tools such as pareto charts without a strong problem-solving methodology. With Lean Six Sigma training, the team evolved from engineers and technicians trying to fix problems to a cohesive team with the necessary tools to rapidly identify issues, brainstorm possible root causes, test hypotheses, and implement the best solution. Issues that had taken weeks to analyze with prior methods were addressed in days or hours.

Speed in problem resolution translates to better yields, better schedule adherence, less rework and less scrap. Cycle time through the factory also improves when minimal troubleshooting and debug is required in test. In short, the ability to rapidly identify and resolve issues saves money and time in many ways.

The key advantages we saw early in the process included:

- The ability to find and eliminate causes of defects and errors using the define, measure, analyze, implement, control (DMAIC)/rapid problem-solving methodology
- Reduction in cycle times and cost of operations using value stream mapping (VSM) and singleminute exchange of die (SMED) tools
- Improved productivity through adoption of Lean principles and Kaizen events
- The ability to better meet customer expectations through voice of the customer (VOC) focus and key performance indicator (KPI) measurements
- Return on investment (ROI) and improved profitability as improvements were implemented.

Implementation challenges needed to be addressed. Initially, there was not enough detail in customer requirements for meaningful VOC analysis. KPIs were based on yield rates rather than PPMs or DPMOs. The data process was not measured or measurement system analysis (MSA) appropriate. The team's lack of expertise resulted in use of unsuitable process improvement tools. However, the combination of training and hands-on experience gained as team members progressed through Six Sigma levels enabled them to identify the corrections needed to make the Lean Six Sigma process highly effective.

As a Six Sigma Black Belt, my perspective has changed from finding quick fixes to permanent solutions. It has also extended my use of Six Sigma processes and tools into my personal life. I even developed a *poka-yoke* at home after losing my keys multiple times.

The benefits of Lean Six Sigma have become visible to those outside the program. Projects in 2021 resulted in a nearly \$197,000 ROI, despite the disruption on team interactions caused by Covid restrictions. During recent audits for ISO 9000, IATF 16949 and VDA, the auditor said the Continuous Improvement department's deployment of the Six Sigma methodology was a strength that complemented other methodologies in place in the facility. Longer-term OEM customers have commented on the improvements they see in terms of the data-driven focus to problem solving and the positive impact it has had on operational excellence. In short, the benefits have more than justified the management support and resources provided to this program.

The "why" behind Lean Six Sigma is more than cost or time savings. This philosophy is also more than a collection of tools and techniques. Instead, it is a continuous learning process in which concepts change practitioners' abilities to problem solve in highly effective ways. Identifying ways to improve has become as much a subconscious activity as breathing, and the DMAIC process ensures root-cause assumptions and good ideas are thoroughly tested, reviewed and documented before any changes are implemented. □

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A self-proclaimed "visionary" doesn't always understand the true meaning of partnership.

IN A PERFECT world, there would be truth in advertising.

It would be jaw-dropping to hear a politician say:

"My statements yesterday regarding the ignorance of voters on the issues of the day were not taken out of context. I meant every word I said, down to the last comma, semicolon and exclamation point, and I stand by them. Many of you don't even know what a semicolon is, much less how to use it. What's more, exploiting that gift of voters' ignorance has propelled my political career and enhanced my electoral viability. Systems are meant for gaming, and I'm seizing the moment my schooling and ambition has set for me. Here in the land where preparation meets opportunity, mine eyes have seen the glory. God Bless America!"

Or to hear a certain classism laid bare with this frank preschool prospectus:

"Vanilla Bean Curd Country Daycare is obsessed with our Mission of empowering little ones to succeed in life, especially when they matriculate and become Big Ones with Influence. Fortunately for you, the aspiring parent of a Young Chancer, there's us. One must start early in the relentless pursuit, cultivation and maintenance of privilege through an awareness and employment of the baser survival and mobility instincts. We are unabashedly proud to be the proverbial first cobblestone on that Machiavellian road. Right Daycare begets Right Preschool begets Right Kindergarten begets Right Elementary School begets Right Prep School begets Right Ivy League School begets connections and prominence and money to support multiple couplings, families and schooling for children from those sources. Repeat the process with new children. (See our rankings.) Get real before you get squashed. It's a competitive world, and connections matter more than ever. Make them here. Skip the line. You're with Our Kind. Get the cash flowing. What will it be? Winner or loser? A lifetime beckons. With us, your little darlings have 'high' and 'worth,' as in 'High Net Worth,' emblazoned on their skulls like QR codes. You'll thank us with your donations."

This is not a perfect world. Agendas like those displayed above remain hidden. For a reason. We are left to figure out motivations on our own.

So it is with Partnership. The term has become elastic. Seller beware.

He pulled up one fine day in a Tesla. (It's always a man.) The indicative license plate proclaimed M3MYS3LF&1. *Sic transit gloria mundi*. So was his lack of spatial reasoning: The vanity-plated rolling declaration was parked at a 30° angle to parallel. Sartorially to match: No tie. No socks. No obvious laundering of his attire. Shabby chic. Nonconformity as conformity. Visionaries want to make a statement, and trivialities like rules are for Little People. So he declared to us, without prompting or an ounce of shame, with that subcontinental swagger typical of those who write code, hit the jackpot once, and thereby think they know everything and deserve admittance to elite circles. They want to share their enlightenment. They make their own rules. Thus, people need to be reminded of their place in the Silicon Valley caste system, pretensions to egalitarianism be damned. Be grateful Greatness has arrived to grant you time with His Presence. Keep your prejudices to yourself. Maybe, just maybe, you'll get in on the IPO.

He had a Great Idea. (Of course he did). He needed help refining his process. Things weren't quite fitting together. Parts were cracking - or breaking apart prematurely while in use and still under warranty. This was embarrassing. Certainly not befitting a Visionary. The nominal design software data weren't meshing with the actual part data. Heat maps were glowing red, not a good color. His additive manufacturing process was subtracting from his cashflow at an unplanned rate, and he needed to know why. The VCs were furrowing their brows and demanding answers. Where were the defects coming from? What was their extent? For answers to these mysteries, he needed his parts CT scanned. Colleagues pointed him to us. Thus, he came to be parked at an off-putting angle in front of our building. He needed help.

That's us: We're "The Help."

We had a CT scanner. He didn't. His problem was our solution. Thus, free exchange is born. Naturally, he wanted a Partnership, but first he had to dazzle.

He beckoned with warm, ingratiating buzzwords, or so he thought. Series A, B, C and D rounds of funding. Stanford pedigree. A-list board (gratefully lacking some of the same astute judges of character who recognized potential in Elizabeth Holmes). Tons of pending orders. Huge upside potential. Ad infinitum. The firehose analogy is accurate: Overwhelm the prey with details. Don't allow them to interject a doubt or a skeptical question. Never stop talking. Allow them to bask in the glow. Control the subject and drive the bandwagon. Cultivate greed and envy.

We sat through a condescending PowerPoint about his soon-to-be iconic company and its game-changing products, designed to make fluid flow faster downhill. (Relative to what?) He is in search of trusted, durable Partners who can help him make his product better and get it to market faster. (That flow thing again.) ROBERT BOGUSKI is president of Datest Corp. (datest.com); rboguski@datest. com. His column runs bimonthly.



Are we of like-minded ambition, enthused about joining him?

What does "joining" mean? Does it come with a number assigned to it, with multiple trailing zeroes?

Perhaps it's a function of age, growing irascibility, and a keener awareness of one's limited time on the planet, but these presentations, in their faux boosterism, blend together. All show. They're slick. Slick as in B*O*R*I*N*G. Enduring them means you won't recover the hours spent listening to them. At slide 42 one wants to stand up and scream, "What do you want?" A common tactic is to deluge the recipient with a stupefying torrent of information, hoping it will render the prey senseless, or at least more pliable, when negotiations begin.

That's why he considers us "The Help."

Often this is a moment of revelation in the test engineering and failure analysis world. The client's pattern of answers to specifics betrays technical ignorance. As in, "We were hoping you could devise a test plan for us," or, "We weren't which sure system x-ray approach was



Beware the tech "visionary" who inflates your "partnership."

best for our needs. We were hoping you could write down an inspection strategy for us to use for future statements of work."

You know, the kind good enough to go anywhere to any competitor to obtain a cheaper quote, otherwise known as Free Engineering. Often, like a good trial lawyer, the client knows the answer to his question when he asks it. He's merely fishing for commitment. How far will he open up? What will a Partnership entail?

But I digress. Slide 42 was the midpoint. The financial pitch was yet to come.

Often we attempt to disarm wary or scheming customers by employing blunt honesty. For many clients it is an invigorating break from their day-to-day to hear us tell them we have no experience with their business and no clue what a good part or system means to us. But we're willing to learn. We are circuit board people who operate a great big CT scanning machine. Inevitably, engineers find it advantageous to bring requests to scan items that are not printed circuit boards. Included among these are additive-manufactured parts, some with exotic materials of varying thicknesses and densities. Some will admit x-rays; some won't.

That's where honesty comes in. If it's an unfamiliar application, manufacturing technique, material, composite or coating, we sometimes admit to the customer its newness (to us). We're willing to learn, and for that we make a deal. We offer to attempt a few test images to see if we can capture the view the customer wishes to obtain, which is often vague due to lack of a statement of work or technical ignorance both feigned and actual – or both! (See above.) These test images are usually offered free of charge, as long as the customer isn't a jerk. If we succeed with those images, terrific. We can then discuss a program that is mutually acceptable and work out the cost

in collaboration with the project engineers. If we don't, then, as the saying goes, no harm, no foul. We tried, and it didn't cost the customer a thing. No risk for them. See you next project.

Historically this approach has worked well. It works really well with engineers from big-name companies that often have labs with our own capabilities and

more, but who lack the speed, flexibility and responsiveness we offer. Two-day turnaround often is a compelling alternative to six- or eight-week turnaround using internal corporate resources, especially if you don't need a glossy report and rely on the images to tell the tale, most especially in line-down situations. The economics of urgency sells itself.

Ease of use notwithstanding, this is a business proposition. The operating assumption remains that if we succeed – however success is agreed to and defined – *the customer will pay*. Free images are a means to an end, namely a successful working inspection program, the terms of which are defined as we go. That is understood. For most, it would seem obvious and not need an explanation.

Except to the Visionary with the parking problem.

When I tell him he'll have to pay a sum for our services, he reacts with the facial features of one who has ingested something unpleasant, probably at the orders of his mother, bringing back unsavory childhood memories of folk medicine. Thus infused, he speaks indignantly of looming betrayal of the goodwill our Partnership is built on.

Built on? We only met an hour ago.

When All the Lights are Green

The time to squeeze out more efficiency is when everything is in spec.

WHAT KIND OF approach do you generally take? Do you follow the "if it ain't broke, don't fix it" mantra, or are you more the "it's good, but it could be better" type? In electronics manufacturing, continuous improvement is often discussed, but how much does your organization adhere to this philosophy when the shop floor is humming and everything is within spec? This is when process engineers should try to squeeze out even more efficiency.

Certainly, there is urgency around a process that is not running as it should. However, when all the lights on the line are green, there is likely opportunity for more improvement than you realize. Consider challenging the process through the lenses of incremental cost reduction and quality enhancement.

In the stencil printing process, there are several possible avenues for lowering cost and raising quality, even when everything is within spec:

Cost down. The first and most obvious area for resource optimization is understencil cleaning. This sub-process of stencil printing has several costs associated with its operation, including time (output reduction) and a fixed cost (fabric and solvent consumables) for every clean. A majority of print platform suppliers ship equipment with relatively liberal default settings for fabric advance (how much is used for each clean) and solvent volume. This is based on assumptions a manufacturer may be cleaning a very dirty stencil with numerous apertures across the entire length of the fabric, so high debris removal must be accommodated. In essence, the defaults are set for worst-case scenarios, as is fairly standard practice. Optimizing these settings based on specific process conditions has the potential to reduce waste through streamlined consumables delivery.

The other understencil cleaning analysis that should be conducted is cleaning frequency. In addition to elevated consumables use, there is an output cost: When you're not printing, you're not producing. Leveraging sophisticated software and SPI tools can deliver deep data analysis and a recommended cleaning frequency that allows the process to remain in control. Perhaps you're cleaning too often, and that is money wasted.

Second, solder paste management is an area a process engineer should examine to further reduce cost. Maximizing paste consumption can have a significant impact on overall process cost. While solder material prices have stabilized in recent years, the move toward Type 5 and even Type 6 pastes to handle miniaturization's challenges can elevate the solder budget. Leveraging sensor technology that monitors the paste roll height allows operators to take the "Goldilocks" approach: not too much, not too little – just the right amount of paste in front of the blade. On-target paste volume reduces both material expense and the environmental cost of waste.

Quality up. When it comes to improving quality, leveraging Six Sigma tools can further refine an inspecification process and move conditions on the very edge of acceptable to the center of the range. Data mining carried out through Excel or any other statistics correlation method – including my favorites XBar and Range – can provide a view into process centering and spread. Then, Cp and Cpk analysis will reveal the repeatability of the process. Perhaps there's a green tick in the box, but only on the border of the "within spec" range.

Using an SPI tool to data mine, one can pinpoint certain areas of the board that may be on the verge of moving from green to amber. Looking at elements like aperture design, processes and material sets (squeegees, tooling, etc.) and making slight changes may deliver more bandwidth to the process and quality to the product.

Last, using design of experiments (DoE) methodology offers continuous improvement opportunities. This is a bit of a forgotten tool, but for process engineers striving for quality utopia, it is essential. Many SPI software packages contain DoE functionality; some are more user-friendly and thorough than others. DoE is not something to undertake before the process is in control. Rather, DoE is about finding the best optimal solution for the centered process, pushing Cp/Cpk higher than where the process began. Engaging in DoE is also quite revealing and identifies the most and least important elements of the printing process. We often talk about stencil printing factors such as speeds and pressures as if they are all equally important; they're not. Some elements, like separation speeds, can have a massive amount of leeway in certain applications. And some, such as print pressure, simply do not. Contemporary DoE software tools are very slick, taking the areas you are interested in evaluating and running countless sequences to find the optimal conditions and inputs.

Extra time is a rarity these days, but when time is on your side, and the stencil printing operation is all systems go, use the opportunity to make the process even tighter and the output quality superior.

CLIVE ASHMORE

is global applied process engineering manager at ASM Assembly Systems, Printing Solutions Division (asmpt. com); clive. ashmore@asmpt. com. His column appears bimonthly.



SHELF



PULSONIX V. 12.0 PCB DESIGN TOOL Pulsonix v. 12.0 includes 3-D collision detection for multi-board designs and board folding. Visualizes boards in stacked or folded configuration and verifies boards and components fit together in intended space. Automated clash detection flags any space violations. Can ignore clashes intended for known connection points like plugs and sockets. 3-D capabilities are integrated into consolidated menu that organizes setup and operation. Has 64-bit implementation and additional multi-threading capabilities. Increased speed with large designs due to increased 64-bit address space and multi-threading for library access; 3-D rendering is now multi-threaded, meaning 3-D viewing and STEP output can be spread across multiple cores. Includes dark mode option, additional rules and DRC checking. New rules include stub routing length, loop antenna, return path, SMD to corner and SMD to plane rules. Has additional enhancements to edit differential pair traces.

Pulsonix

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TECHCON TS9800 SERIES JET VALVE

TS9800 series jet valve dispensing system is comprised of TS9800 Piezo-actuated iet valve and TS980 smart controller. Uses piezo, noncontact jetting technology for increased speed and accuracy during dispensing process. Is capable of dispensing dots and lines as small as 0.5nL at up to 1500Hz continuous and 2000Hz max bursts, jetting viscosities up to 2 million cps. Modular features include external power source. TS980 Smart Controller offers touch-screen interface, reportedly featuring fast setup and easy calibration. Includes standard internet port. Applications include edge sealing and end sealing of LCD and OLED displays; die bonding and frame bonding for camera module assembly; jetting silicone phosphor in LED assembly; dispensing underfill in microelectronic package applications on PCBAs; applying microdots of UV adhesive in medical device applications.

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TRI TR8100H SII ICT

TR8100H SII high-density pin count incircuit tester with vacuum fixture targets low-voltage testing market. Is also for large, complex PCBAs. Reportedly ensures full pin contact, with up to 11,088 pin digital MUX-free architecture. Has built-in auto-calibration and self-diagnostics.

Test Research, Inc.

tri.com.tw/en/index.html



VISCOM 3-D MXI SYSTEM X8011-III

X8011-III automated 3-D MXI resembles exterior of iX7059 systems. To inspect THTs or identify voids in surface soldering, analysis parameters can be selected and adjusted quickly during operation. Provides overview of tools required to create inspection plan for automatic x-ray inspection. 3-D reconstructions can be achieved with computed tomography. Options are available as part of XVR software. Individual layers of irradiated object provide nondestructive information on whether or not manufacturing defect is present. Smart networking is integrated into production line. Overlap between MXI and AXI properties. Inspection data from 3-D SPI and post-reflow systems can be compared at verification station with detailed 3-D MXI results. Manual x-ray system reads inspection plan from production line to automatically approach only positions on assembly that need to be verified. Reports with result and system data are generated automatically, including radiation dose information. Reportedly ideal for inspecting radiation-sensitive components.

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In Case You Missed It

Additive Manufacturing

"Improved Modeling of Kinematics-Induced Geometric Variations in Extrusion-Based Additive Manufacturing Through Between-Printer Transfer Learning"

Authors: Jie Ren, et al.

Abstract: The authors deal with the challenge by establishing a mathematical model that quantifies the printing width variations along the printing paths induced by printing speed and acceleration. The model provides vital information for predicting infill pattern nonuniformity and potentially enables using G-code adjustment to compensate for the infill errors in future research. In addition, since the model captures the mechanism of kinematics-induced variations, it provides a way of between-printer knowledge transfer on estimating printing errors. This article further proposes an informative-prior-based transfer learning algorithm to improve the quality prediction model for a printer with limited historical data by leveraging the shared data from interconnected 3-D printers. A case study based on experiments validated the effectiveness of the proposed methodology. (IEEE Transactions on Automation Science and Engineering, March 2021, https:// ieeexplore.ieee.org/document/9380390)

Nanosolder

"Molecular Dynamics Simulation on Wetting of Silver Nanosolder on a Diamond Surface"

Authors: Muhammad Saad Ali, et al.

Abstract: Analyzing the wetting behavior of silver on a diamond substrate is crucial prior to joining and printing diamond chips in electronics, bioimplants and cutting tool industries. The authors used molecular dynamics models to overcome the hydrophobic behavior. It was observed the hydrophilic character was well promoted when a nanosolder block of silver was collided at a certain velocity on a diamond substrate in a hydrodynamic state, rather than when it was stationary and then heated on diamond. Hydrodynamic wetting led to rapid spreading, which in turn elucidated a high rate of change in contact area to the highest 11 832 Å2 and a high rate of decrease in contact angle to the lowest 23° at the highest contact velocity of 19.7km/s in minimum time. Therefore, hydrodynamic wetting has a leading margin for silver coating on diamond surfaces over temperature, slab separation and hydrostatic wetting. This paper provides theoretical insights for effective thin-film development in the least possible time, with the lowest solder consumption. (Physical Properties of Materials and Interfaces, April 2022, pubs.acs.org/doi/10.1021/acs.jpcc.2c00124)

Solder Joint Reliability

"The Effect of Electric-Thermal-Vibration Stress Coupling on the Reliability of Sn-Ag-Cu Solder Joints"

Authors: Xinlan Hu, et al.

Abstract: The damage of the package structure, caused by the multi-stress coupling of various environmental factors, can lead to electronic device failure. Therefore, through the finite element method, the reliability analysis of three kinds of lead-free Sn-Ag-Cu solders (SAC 105, SAC 305, SAC 405) in ball grid array (BGA) packaging was conducted under the conditions of thermoelectric coupling and random vibration, respectively. The results, according to the modified Coffin-Mason model, indicate SAC 405 has the largest plastic strain range and the shortest fatigue lifetime under thermoelectric coupling. As a counterpart, SAC 105 has the smallest plastic strain range and the longest lifetime. However, under random vibration load, by addressing the Miner linear damage rule, the empirical formula of Manson high-cycle fatigue and Steinberg's three band theory, the fatigue lifetime of SAC 405 is the longest, which is twice as much as SAC 105 and SAC 305. Furthermore, based on the linear damage superposition approach, the fatigue lifetime is predicted as SAC 305<SAC 105<SAC 405 under multi-stress coupling of electric, thermal and random vibration conditions. These results will provide theoretical support for improving the application reliability of packaging in complex environments. (Journal of Electronic Materials, November 2021, https://link. springer.com/article/10.1007/s11664-021-09302-y)

Thin Films

"Perovskite Oxide Ferroelectric Thin Films"

Authors: Mingyue Tian, Lan Xu and Ya Yang

Abstract: How to prepare high-performance Perovskite oxide thin-films is the most difficult challenge for researchers. Multiple factors determine the application area of thin films and influence the performance of thin films. The preparation of the material determines its structure; the structure further influences the material's performance; and the performance decides the material's application, indicating these four factors are inextricably linked. This article reviews the preparation methods of perovskite oxide films and various factors that affect film properties, as well as basic physical properties. This paper lists methods to improve the physical properties of thin films and the latest applications in various fields in recent years. (Advanced Electronic Materials, March 2022, onlinelibrary.wiley.com/doi/10.1002/aelm.202101409)

This column provides abstracts from recent industry conferences and company white papers. Our goal is to provide an added opportunity for readers to keep abreast of technology and business trends.





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