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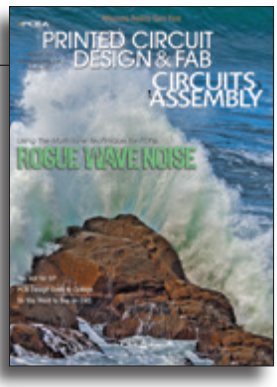




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with WILL KENDALL and OSCAR GONZALEZ

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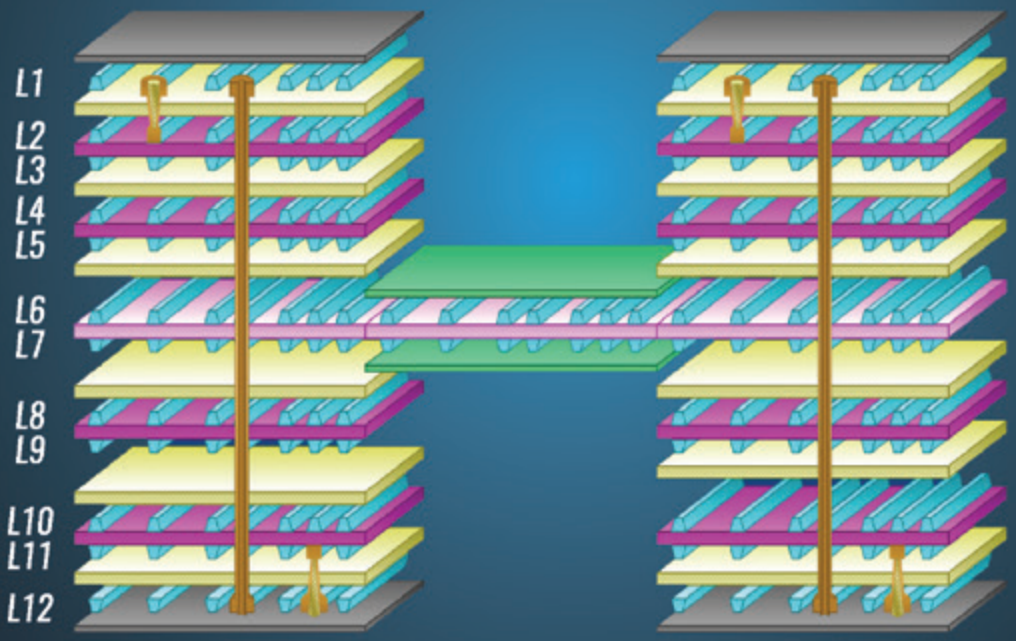


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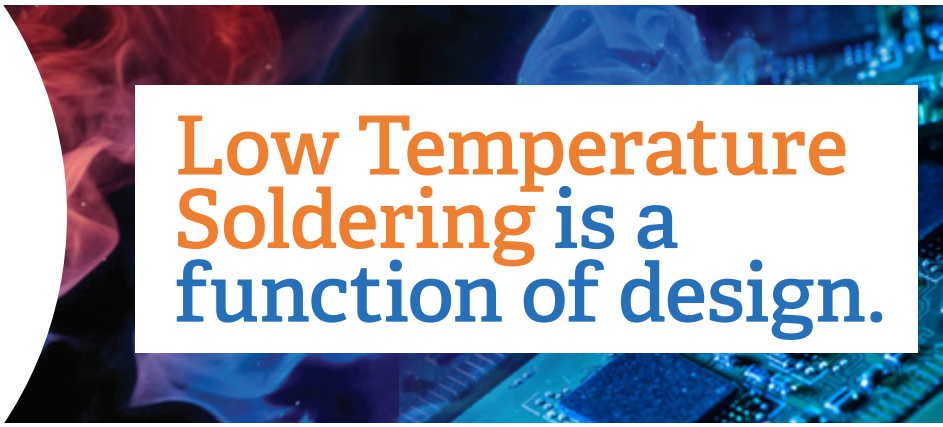

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# The Future of Space is No Longer Up in the Air

IT WASN'T LONG ago NASA administrators were lamenting ongoing cuts to the world's leading space agency's annual budget were putting the US at risk of falling behind its competitors.

No one remembers, but in the 1960s the line item for NASA made up more than 4% of the federal US budget. Once a few footprints were made in space, however, the shine was off the moon rock. A decade later, NASA's budget had been slashed by two-thirds in real dollars, and only briefly topped 1% of the federal budget again over the next 50 years.

Today it hovers around 0.5%, which still translates to more than $20 billion a year in funding. Indeed, the Biden administration proposed allocating nearly $25 billion to NASA in 2022 to support moon exploration and more.

As craft go up, costs come down. It can cost up to $400 million to lift some United Launch Alliance ships off the ground. That's one reason why NASA is so interested in its so-called Venture Class of launch vehicles, smaller vessels that carry smaller payloads but lower risks, especially to the bottom line if they end up cone down. These rockets are priced at a few million dollars apiece, chump change, especially for those, ahem, explorers named Branson or Bezos.

More than a dozen companies in the US alone have been launched to deliver humans and cargo above, and NASA has carved out a few hundred million dollars of its budget to support such efforts.

There's a lot going on over our heads. Russia, China, Israel, India, and Luxembourg (!) have joined the US in launching moon missions, and more than a dozen countries have at least 10 satellites now orbiting Earth. More than 4,500 satellites are currently traversing the skies, according to the Union of Concerned Scientists. (See their database here: https://bit.ly/3oQkv4i.) The skies, it seems, are the new Manhattan.

Jokes aside, space is serious stuff. So serious, in fact, NASA quietly warned one of those private launch providers that its non-geostationary (a fancy word for "moving") orbit satellite system is a risk to the NASA space missions, including manned operations such as the International Space Station. NASA was responding to SpaceX's plans to launch some 30,000 satellites to orbit later this year. For its part, the space agency is tracking about 25,000 objects in orbit (not all are manmade), of which more than 6,000 have a perigee – the point in the orbit of the moon or a satellite at which it is nearest to Earth – of less than 600km. Based on the letter, dated Feb. 8 (www.scribd.com/document/557924666/NTIA-NASA-NSF-letter-to-FCC-regarding-Starlink-Gen-2), NASA looks to be pushing back, citing possible risks to its ongoing missions and even human life.

"SpaceX's Gen2 expansion," the agency wrote, "would more than double the number of tracked objects in orbit and increase the number of objects below 600km over five-fold, without factoring in growth from other proposed constellations. An increase of this magnitude into these confined altitude bands inherently brings additional risk of debris-generating collision events based on the number of objects alone. NASA anticipates current and planned science missions, as well as human space flight operations, will see an increase in conjunctions [read: collusions]." Such an increase, NASA asserts, could also degrade the images captured by the Hubble telescope, while also obscuring ground-based telescopes that survey for Earth-bound asteroids. (Two days after the letter was submitted, SpaceX lost nearly an entire fleet of 49 satellites right after launch due to a solar storm. Don't look up, indeed.)

As retired astronaut Paul Lockhart notes, technology drives economics. NASA proposes SpaceX prove out its collision avoidance system as a condition of its launch. Such developments have obvious corollaries to terrestrial uses. Besides sensors, we can expect major advancements in robotics, communications, additive manufacturing (space travelers may need to print their own food), virtual reality, among other technologies, all of which need to be designed and engineered here on Earth.

The future of space is no longer up in the air, but making products – and profits – remains a high-risk venture. Organizations like the Printed Circuit Engineering Association offer the training and guidance from minds experienced in high-reliability electronics design and manufacturing. Join us at PCB East (pcbeast.com) in April in Marlborough, MA, or at one of our local chapter meetings, and take advantage of the printed circuit pioneers. □

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## PCDF People

**Bev Christian (left), Doug Pauls,** and **Jose Servin** were presented with Dieter Bergman IPC Fellowship awards.

Nano Dimension named **Sean Patterson** chief revenue officer. He joined in June 2021 as president of Americas after holding leadership roles in Amazon's transportation and healthcare groups.

Sunstone Circuits added **Debra Coburn** to its management team as human resources manager.

Zuken Vitech appointed **Enrique Krajmalnik** CEO. He joined Zuken USA in 2020 as vice president of business development and later moved into the Vitech organization as COO.

## PCDF Briefs

**Altium** and **MacroFab** announced Altimade, a "design with manufacturing" application, is now available to the Altium user community.

On Sept. 1, **Bowman** will formally open a new 20,000 sq. ft. global headquarters in Schaumburg, IL.

**DuPont Microcircuit** and **Components Materials** are collaborating with **Kuprion** to launch ActiveCopper thick film paste products to the electronics industry.

**DuPont Interconnect Solutions** completed a $250 million expansion at its manufacturing site in Circleville, OH, expanding production of Kapton polyimide film and Pyralux flexible circuit materials.

**Nano Dimension** is collaborating with **TTM Technologies** to open an AME NanoLab at TTM's advanced manufacturing center in Stafford Springs, CT.

**RBP Chemical Technology** announced an exclusive partnership with **Schlötter** in Geislingen, Germany.

**Ventec's** Fullerton, CA, facility is now certified according to AS9100D and ISO 9001:2015.

## It's Official: PCEA Acquires Key Assets of UP Media Group

**PEACHTREE CITY, GA** – The Printed Circuit Engineering Association (PCEA) has closed on its acquisition of the functional assets of UP Media Group Inc., including its industry leading publications and trade shows.

The deal, which was pre-announced during the PCB West conference and exhibition last October, includes the annual PCB West and PCB East trade shows; PRINTED CIRCUIT DESIGN & FAB (PCD&F) and CIRCUITS ASSEMBLY magazine; the PCB UPdate digital newsletter; the PCB Chat podcast series; the PCB2Day workshops and webinars; and Printed Circuit University, the dedicated online training platform.

The deal establishes PCEA as the leading association for printed circuit engineers worldwide, with over 2.5 million engagements annually to printed circuit engineers, designers, fabricators and assemblers.

Upon closing, Mike Buetow has been named president; Frances Stewart has been named vice president, sales and marketing; Chelsey Drysdale has been named chief content officer; and Brooke Anglin has been named senior sales executive.

The staff reports to the PCEA board of directors, which is made up of 10 industry professionals led by chairman Stephen Chavez and vice chairman Michael Creeden.

"We have been looking forward to this day since we entered negotiations with PCEA several months ago," said Mike Buetow, president, PCEA. "We are fired up and ready to engage with our members, starting with PCB East, our first live event as part of PCEA, which takes place in April in Marlborough, MA."

"I cannot believe we finally closed the deal," said Stephen Chavez, chairman, PCEA. "Simply amazing, but I'm more amazed at what we just accomplished from only being in existence for two years and starting from scratch.

"We are extremely excited and very eager to attack this great new adventure. We're even more tenacious and passionate in our eternal quest to collaborate, educate, and inspire for the betterment of the industry. The first upcoming PCEA conference is PCB East. We hope to see you there." (MB)

## Next-Generation Technologies to be Highlighted in PCB East Keynote

**PEACHTREE CITY, GA** – International electronics industry consultant Gene Weiner, fresh off a trip across the Atlantic where he visited several emerging companies, will keynote this year's PCB East conference. Weiner's talk, "From Possibility to Reality," will paint a picture of exciting possibilities in additive manufacturing, materials, equipment, components and other developments that may be in full swing in the next few years.

Gene Weiner

The PCB East conference and exhibition (pcbeast.com) will return Apr. 11-13, to Marlborough, MA. Weiner's keynote, which is free to all conference and expo registrants, takes place April 12 at 11 a.m.

"It's a new day for industry engineers," says Weiner, "facing challenges and opportunities with new tools, products and software at their disposal to create never before possible interconnected packages. A realm of new possibilities in design and manufacturing is being made possible by rapidly emerging advances in a wide variety of additive manufacturing processes of printed circuits and precision components, as well as specialty substrates.

"Looming new technologies, including AI, offer the chance to create new designs, such as precision capacitors *in situ*, odd-shaped precision inductors (in place), precision shielding in place, rapid precise placement of Type 6 or 7 solder pastes permitting higher first-pass yield on assembly of very fine components, and more that could

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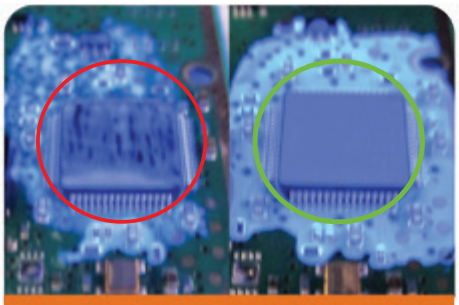

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## CA People

AIM appointed **Javier Corona** to district sales manager, Northern Mexico.

Altus appointed **Kevin Suen** applications engineer. He has a degree in mechanical engineering from Birmingham University.

APITech named **Matthew Erlichman** quality engineer and supervisor.

Flex named **Rob Campbell** president, Consumer Devices.

Hernon Manufacturing hired **Edgar Rosas** as country manager for Mexico.

IPC inducted **Joe O'Neil** to the Raymond E. Pritchard Hall of Fame in recognition and acknowledgment of contributions to IPC and the electronics industry.

Koh Young promoted **Ivan Aduna** to global MES leader. He previously designed test plans at Intel and worked on embedded software systems at Dextra Technologies.

MacDermid Alpha Electronics appointed **Karl Pfluke** district sales manager of the Southeast, supporting the Alpha and Kester assembly brands.

MicroCare appointed **Manuel Gonzalez** Eastern Mexico regional sales manager.

Plexus named **Steve Frisch (left)** president and chief strategy officer and **Oliver Mihm** chief operating officer.

STI Electronics promoted **Erin Lewis** to quality manager.

## CA Briefs

**BEMA Electronics** bought a **Seica** flying probe tester.

**Cicor Group** said discussions are underway to acquire **SMT Elektronik's** company's electronic manufacturing services activities in Germany. SMT Elektronik employs 145 staff in Dresden and had sales of €22.4 million, with a net profit of €1.2 million in fiscal 2020, much of which came from the EMS unit.

reduce re-spins or make faster adjustments.

"Design engineers who are aware of these innovations in equipment, processes, and materials and their capabilities can be more creative. One of the challenges will be to establish standards for newly designed products and their compositions."

In this keynote, Weiner will draw upon his more than a half-century of global firsts and experiences with major inflection points and new product entries into the PCB fabrication and EMS sectors of electronic packaging to introduce and predict the possible and the probable.

"Few people in the world have seen the variety of printed circuit, semiconductor and electronics packaging technologies that Gene Weiner has, and ever fewer are able to put them in the context of how they can be implemented," said Mike Buetow, president of PCEA and conference director, PCB East. "I guarantee attendees will come away with their eyes opened to new possibilities for design and manufacturing." (MB)

## Draper Team Develops Predictive Design Tool

**CAMBRIDGE, MA** – Draper has developed a predictive design tool that has been tested and validated to show it can predict material failure rates and help determine design requirements for printed circuit boards and similar products.

In tests, engineers found the tool accurately predicted methods to reduce and eliminate laminate crack initiation and propagation on a PCB.

The study, prepared for IPC Apex Expo 2022, was conducted by designing printed circuit boards, using different configurations and materials, and subjecting the boards to environmental stresses and other tests. Using principles of predictive design, engineers developed data sets to guide them. One data set included tests of the PCB materials for such attributes as fracture toughness and thermal conductivity. Another set included detailed design characteristics of the PCB itself.

With the data, the engineers developed a virtual test bed – a finite element analysis computer-aided model – and used it to run scenarios of various PCBs. The FEA model successfully predicted a 50% decrease in internal stress that would reduce or eliminate PCB laminate cracks.

By tweaking the kind of materials and design layouts of a PCB, the team was able to reduce the number, kinds and severity of defects in the board when minor design changes were made.

Wade Goldman of Draper led the team.

"The FEA model allows us to move attributes around to reduce the number and likelihood of cracks in the PCB," Goldman said. "If each design works as expected, PCB designers and manufacturers are no longer limited to manufacturing by trial and error. Instead, they can spend their time evaluating design changes that might be useful in order to reduce defects and not change their processes."

The model arrives at an opportune time for the technology industry, Goldman added. "These days it's all about designing higher density PCBs. As a result, interconnects are becoming smaller, which introduces fragility, and the industry is making more material choices to make higher density interconnects work. You need a predictive design tool to support that effort."

The predictive design tool is expected to provide PCB designers with a model for determining design rules for future products.

"With this new capability, we have taken a big step in being able to manufacture higher quality printed circuit boards." (CD)

## ICAPE Group Acquires Cebisa France

**PARIS** – An ICAPE Group subsidiary has signed an agreement to acquire 100% of Cebisa France, a printed circuit board supplier based in Lisses. The transaction was expected to close at the end of February. Founded in 1996, Cebisa France had sales of €2.8 million across its 50 customers in Europe last year.

**Cope Assembly Products** will represent all **Hentec/RPS** in Georgia, Mississippi, Alabama, and Tennessee.

**Dynamic Source Manufacturing** purchased its fourth **Juki** ISM3600 storage tower.

**East West Manufacturing** is receiving an undisclosed investment from **MSD Partners.**

**IPC** presented its highest corporate honors to **Apple** and **MacDermid Alpha.**

**Parmi** named **Horizon Sales** manufacturers' representative group of the year.

**Rehm Thermal Systems** named **Hilpert Electronics** distributor for Switzerland.

**Rocket EMS** has begun electronics manufacturing operations in a newly acquired 50,000 sq. ft. facility in Carson City, NV.

**Saki's** job data conversion function is now available with **Fuji** surface mount machines.

**Scanfil** will expand its EMS factory in Wutha-Farnroda, Germany, by 2,200 $m^2$, with production estimated to begin in the second quarter of 2022. The existing factory is 4,500 $m^2$ and employs approximately 270 staff.

**SMTA** is seeking student applications for the $8,000 Charles Hutchins Educational Grant (https://smta.org/page/hutchins-grant).

Following a merger announcement between **Tempo Automation** and **ACE Convergence Acquisition,** ACE filed a supplement to its Dec. 15 proxy statement, wherein ACE proposed to extend the date by which the company must consummate its initial business combination from Jan. 30 to July 13.

**Unitron Group** selected **Aegis'** FactoryLogix MES.

**Videoton EAS** will almost double its production capacity in Stara Zagora, Bulgaria, in the near future.

**Waséyabek Development** has acquired EMS firm **Safari Circuits** for an undisclosed sum.

**Worthington Assembly** is among the companies receiving grants from the Innovation Institute at the **Massachusetts Technology Collaborative (MassTech)** in an initiative to bring artificial intelligence to businesses across the state.

**Yunex Traffic** bought two **Mek (Marantz Electronics)** desktop AOI systems.

**Z-Axis** invested in an **Austin American Technology** HydroJet inline cleaner.

The deal came about after several months of negotiation and planning.

In a statement, ICAPE Group CEO Cyril Calvignac said, "We are very happy to have signed an agreement with Cebisa France, whose activities will soon be transferred to the teams of ICAPE France. With this new important step, ICAPE Group strengthens its leading position on the French electronic suppliers market." (MB)

## Element Solutions Acquires HSO Herbert Schmidt

**SOLINGEN, GERMANY –** Element Solutions acquired HSO Herbert Schmidt, a multinational developer of surface finishing technology and chemistry. Terms of the deal were not disclosed.

HSO focuses on environmentally sustainable products, especially in plating on plastics. In 2021, HSO was certified as a climate-neutral electroplating operation functioning under the values of sustainability and climate protection.

Future results from this acquisition will be reported in Element Solutions' Industrial and Specialty segment. (CD)

# Fire Scuttles Elvia's PCB Site in Loire Valley

**LOIRE VALLEY, FRANCE –** A fire in the early afternoon of Jan. 30 at Elvia's plant here destroyed the printed circuit board fabricator's entire production workshop.

The fire was contained at the end of the afternoon, and no injuries were reported.

A preliminary investigation has been opened by the Orléans public prosecutor's office to determine the origin and circumstances of the fire, which are still undetermined.

All factory activity has been shut down, sidelining the site's 87 employees.

While the Loire Valley plant is being cleaned up, a transfer plan is being prepared to permit production to continue, the company said.

It's unclear how the fire will affect the potential sale of Elvia. In early January, Tikehau Ace Capital announced it had entered into exclusive negotiations to acquire 100% capital of the company in a deal expected to close in the first half of this year.

Elvia was founded in 1976 and has five production sites in France and over 450 employees. (MB)

# Axion BioSystems Acquires M-Solv Manufacturing

**ATLANTA –** Axion BioSystems acquired printed electronics manufacturer M-Solv Manufacturing, a subsidiary of M-Solv Ltd. The creation of a new division, Axion BioSystems Manufacturing, UK, cements the six-year partnership between the companies.

"The need to control the supply chain has never been more important," said Tom O'Brien, CEO of Axion BioSystems. "This vertical integration not only ensures our customers have the products they need to conduct critical biomedical research. It also allows us to advance assay plate technologies more rapidly to meet the increasingly complex scientific demands of our users."

"The M-Solv manufacturing team is proud to have played a role supporting Axion's growth over the last six years," said Phil Rumsby, CEO, M-Solv Manufacturing. "Now, as part of the Axion Group, we are looking forward to working together even more closely to grow this part of our business, as we develop the next-generation of bioelectronic assay consumables. Alongside our biosensor business, we will continue to maintain and grow our strong position in touch-panel devices."

No financial terms of the transaction were disclosed. (CD)

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| Lam Cycles: | Up to 8x |
| Micro BGA Pitch: | .2 Millimeters |

FLEX / RIGID-FLEX

| | |
|---|---|
| Standard Flex: | 1 – 6 Layers |
| Rigid Flex: | 4 – 22 Layers |
| Rigid Flex HDI Lam Cycles: | Up to 2x |

## LEAD TIMES

RIGID

| | |
|---|---|
| Standard: | 15 Days |
| 2 – 10 Layers: | 24 Hours |
| 12 - 24 Layers: | 48 Hours |

HDI; BLIND/BURIED/STACKED VIA

| | |
|---|---|
| Via in Pad: | 48 – 72 Hours |
| HDI : | 3 – 15 Days* |

** Depending upon # of Lam Cycles*

FLEX / RIGID-FLEX

| | |
|---|---|
| Flex 1 – 6 Layers: | 5 – 15 Days |
| Rigid Flex 4 – 22 Layers: | 7 – 15 Days |
| Rigid Flex HDI 2x Lam Cycles | 20+ Days |

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# Global Flex PCB Market to Grow at 9% CAGR Through 2026

**DUBLIN –** The global market for flexible printed circuit boards is projected to reach $20.3 billion by 2026, growing at a CAGR of 9.2% during 2020-2026, according to Research and Markets.

Double-sided FPCBs are projected to grow at a 9.5% CAGR to reach $10.4 billion by the end of the analysis period.

Growth in the rigid-flex segment is revised to an 8.6% CAGR for the next seven-year period. This segment currently accounts for 21% of the global FPCBs, says the research firm.

In the global single-sided segment, the US, Canada, Japan, China and Europe will drive the 7.5% CAGR estimated, accounting for a combined market size of $2.4 billion by the end of 2026.

## NOTHING TO WATCH

| Trends in the US electronics equipment market (shipments only) | % CHANGE OCT. | NOV. | DEC. | YTD% |
|---|---|---|---|---|
| Computers and electronics products | -0.6 | 0.3 | 0.8 | 5.5 |
| Computers | 1.4 | 0.1 | -2.5 | 1.1 |
| Storage devices | -3.5 | -2.7 | -0.7 | 26.7 |
| Other peripheral equipment | -2.0 | -4.1 | 8.4 | 3.7 |
| Nondefense communications equipment | 0.7 | 1.0 | -1.4 | 6.3 |
| Defense communications equipment | 1.7 | -3.8 | 0.0 | 3.2 |
| A/V equipment | -0.4 | 14.1 | -8.7 | 2.6 |
| Components[1] | 1.4 | 0.5 | -0.6 | 6.6 |
| Nondefense search and navigation equipment | 0.7 | -0.5 | 0.1 | 2.6 |
| Defense search and navigation equipment | 0.1 | 0.1 | 0.1 | 2.1 |
| Medical, measurement and control | -1.1 | 1.1 | 2.0 | 5.7 |

[r]Revised. *Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: U.S. Department of Commerce Census Bureau, Feb. 3, 2022

## US MANUFACTURING INDICES

| | SEP. | OCT. | NOV. | DEC. | JAN. |
|---|---|---|---|---|---|
| PMI | 61.1 | 60.8 | 61.1 | 58.8 | 57.6 |
| New orders | 66.7 | 59.8 | 61.5 | 61.0 | 57.9 |
| Production | 59.4 | 59.3 | 61.5 | 59.4 | 57.8 |
| Inventories | 55.6 | 57.0 | 56.8 | 54.6 | 53.2 |
| Customer inventories | 31.7 | 31.7 | 25.1 | 31.7 | 33.0 |
| Backlogs | 64.8 | 63.6 | 61.9 | 62.8 | 56.4 |

Source: Institute for Supply Management, Feb. 1, 2022

## KEY COMPONENTS

| | AUG. | SEP. | OCT. | NOV. | DEC. |
|---|---|---|---|---|---|
| Semiconductor equipment billings[1] | 37.8% | 35.5% | 41.4% | 50.7%[r] | 46.1%[p] |
| Semiconductors[2] | 30.0% | 27.6% | 24.4% | 24.5%[r] | 28.3%[p] |
| PCBs[3] (North America) | 1.48 | 1.25 | 1.15 | 1.10 | 1.17 |
| Computers/electronic products[4] | 5.26 | 5.27 | 5.30 | 5.34[r] | 5.35[p] |

Sources: [1]SEMI, [2]SIA (3-month moving average growth), [3]IPC, [4]Census Bureau, [p]preliminary, [r]revised

# Hot Takes

- **Worldwide smartphone shipments** were 362 million during the fourth quarter, down 3.2% year-over-year. On an annual basis, the market grew 5.7% in 2021, with 1.35 billion smartphones shipped. (IDC)
- **Total semiconductor sales** will rise 11% this year, following a 25% increase in 2021 and an 11% increase in 2020. (IC Insights)
- **Worldwide tablet shipments** amounted to 46 million units during the fourth quarter, down 11.9% year-over-year, posting a decline for the second time since the pandemic began in 2020. (IDC)
- Six million **electric cars** (battery electric and plug-in hybrid) will be shipped in 2022, up from four million in 2021. (Gartner)
- The overall **electronic component sales** sentiment index registered 116.5 for January, slightly up from the prior month's results. (ECIA)
- Sales of **printed circuit board and multichip module CAD software** increased 14.5% year-over-year in the third quarter to $298.3 million. (ESDA)
- **North American EMS orders** in December were up 47.1% year-over-year and 13.8% sequentially. Shipments were up 0.9% compared to December in the prior year and 8% sequentially. (IPC)
- Global shipments of **traditional PCs** (desktops, notebooks, and workstations) reached 92.7 million units during the fourth quarter, up 1% year-over-year. (IDC)
- Global electronics manufacturing survey results show nearly nine in 10 **electronics manufacturers report material costs** are rising, with an additional four-fifths reporting rising labor costs; 13% of the electronics manufacturing supply chain reports inventory is growing, and one in 10 say inventories from their suppliers are growing. (IPC)
- **Global semiconductor sales** totaled $556 billion in 2021, the highest ever annual total and an increase of 26.2% year-over-year. (SIA)
- Device suppliers shipped 30% more **IC units to the automotive industry** in 2021 compared to 2020. (IC Insights)
- The **semiconductor shortage** and the Covid-19 pandemic disrupted global OEMs' production in 2021, but the top 10 OEMs increased their chip spending by 25.2% and accounted for 42.1% of the total market. (Gartner)
- **Worldwide shipments of foldable phones,** including flip and fold form factors, reached 7.1 million units in 2021, up 264% over 2020. Forecasts project shipments will reach 27.6 million units in 2025, a CAGR of 70% from 2020 to 2025. (IDC)
- The supply of **NAND flash device controller ICs** remains tight, particularly those demanding 55nm and 12/16nm process manufacturing. (DigiTimes)

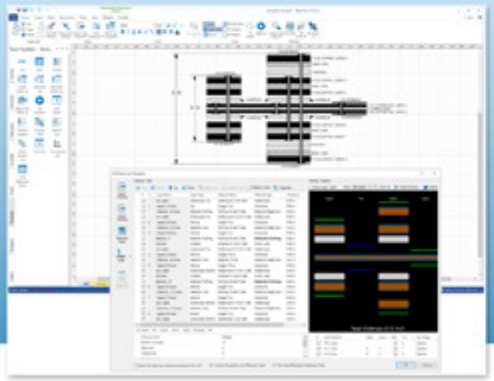
# Support For Flex, Rigid Flex and Embedded Component Designs Now Available.

BluePrint-PCB

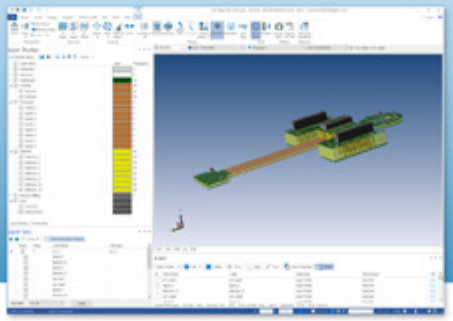
CAM350

DownStream's CAM350 and BluePrint-PCB support importation and visualization of PCB designs containing Flex, Rigid Flex or Embedded components. Visualize designs in both 2D and 3D, and easily document complex Flex or Rigid- Flex Stack-Ups for submission to PCB Fabricators.

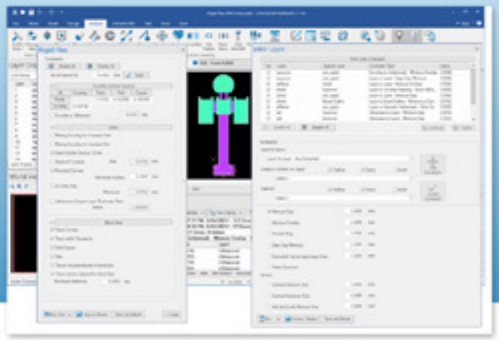
- Import and Visualize Flex, Rigid-Flex and Embedded Component Designs
- 3D Visualization to Validate PCB Construction and Component Assembly
- Manage Variable Stackup Zones for Rigid-Flex Designs
- Easily Create Custom Flex or Rigid-Flex Fabrication and Assembly Documentation
- Use DFM analysis to analyze a flex or rigid-flex design for potential fabrication or bend related defects



Use Stack Up Visualizer and Blueprint's Rigid-Flex Stackup template to easily manage and document rigid-flex stackups.



A rigid-flex design in 3D. Shown with layers spread to improve visualization of the layer stackup.



Use Rigid-Flex and Inter-layer DFM analysis to analyze flex and rigid-flex designs.

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# Get Ready for New North American Opportunities

As governments realize the importance of investing in domestic manufacturing, opportunities are coming for EMS firms and PCB fabricators.

IT TAKES TIME to gain perspective, especially perspective on the industry you are immersed in. In my case, it's been 30 years since I entered the printed circuit board market. During the first six or seven years, it was heady, upbeat times in North America. Growth was a bounty supporting hundreds of domestic fabricators. Materials, supplies and capital equipment were made "locally" in North America. Then, around the new millennium, everything changed.

Suddenly, work headed to Asia, and fabricators contracted at an unprecedented scale to fewer than 200 within a few short years. The collateral damage was a collapse of materials, supplies and capital equipment companies that supported the industry. Even worse was the exodus of skilled talent who sought careers in more promising industries and never looked back. The relatively few companies that survived did so by hunkering down, focusing on a niche, and investing in only the equipment they needed to support their business base, in some cases taking draconian steps that worked short term but eventually led to their demise. Over the first decade-plus of the new millennium, it was depressing to be a North American circuit board fabricator.

However, times change, and with that change, opportunities emerge – finally!

After decades of ignoring reality – and for a variety of reasons and events, many of which have nothing to do with printed circuit boards, or even electronics – government and industry leaders are "shocked" to learn so much of North America's manufacturers are no longer globally competitive and how much more capability and capacity is required for economic and military security. Now that they understand the need to invest in manufacturing, more specifically in electronics manufacturing – everything from chips to bare circuit boards and substrates – opportunities for the North American PCB industry finally may be knocking.

Do we open the door and take full advantage, or ignore it and squander our chance?

To take advantage of the current momentum to expand and enhance North American capabilities and manufacturing capacity may require a radical rethinking, or at least retraining, in how we as an industry operate. The entire risk/reward equation in particular needs to be revisited. After nearly 20 years of operating in a hunkered-down mode to mitigate risk and maximize reward, many in our industry may need to be retrained to break old habits and embrace a paradigm shift the opportunities of the future offer.

The first step toward taking advantage of new opportunities may be a brutally honest self-evaluation of what your company does, for whom, and with what resources. Most important is understanding what government or "C-suite" investment in electronics technology may look like and how that will impact your customers. As an example, if chip plants are built in North America, what other electronics manufacturing may now become more cost-effective if done closer to those plants vs. overseas. And, what printed circuit board technology will that increased demand for capacity impact?

With investment in more advanced technology, will new materials and the processing knowhow and equipment be outside current capabilities or comfort zones? Discussions with material suppliers should include a dialogue on what to be aware of; begin experimenting to be better prepared.

If the gap in North American electronics capability points to a specific type of printed circuit board technology that will be in especially high demand, that may be the place to consider increasing capital investment to either add capacity, enhance capability or broaden product offerings to include the growth opportunity. This review should include an estimated capital equipment budget and supporting cash flow, as well as a reality check with current customers to understand if their products and purchasing demands may also be impacted and shifting.

When demand increases, what type of employees will your company need to hire? This leads to workforce development opportunities that currently exist, and in the next few years will expand with an increase in qualified people seeking jobs in electronics. More important, with the emphasis on investing in new capabilities, what talent gap might you have that would prevent being able to produce a new technology? Getting involved *now* may be the best way to ensure having qualified talent when needed.

To take advantage of any opportunity that a reinterest in North American electronics manufacturing may present, it is essential to stay informed and get your team ready. Nothing will happen overnight, but it will happen more quickly than anyone who has become comfortable in the current industry paradigm imagines. We all need to be aware significant new opportunities are finally on the horizon.

After so long operating in a contracting industry segment, we in North America cannot afford to let the coming opportunities be squandered. Opportunity for growth is knocking for us all. ▫

**PETER BIGELOW**
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# A 'No X-Out' Policy is a PCB Cost Driver

A board's level of technology should dictate how often to expect imperfections.

ONE OF THE most common questions I get from PCB buyers is, "How many X-outs are acceptable?" Some might say receipt of a PCB manufacturing panel or array with *any* X-outs indicates the supplier cannot maintain a high level of quality.

This is not necessarily the case.

An X-out occurs when a defective board in an array or manufacturing panel of like PCBs has been shipped. The board is literally marked with an X in permanent marker to signify it is flawed.

While a panel or array with zero X-outs is ideal, the board's level of technology should dictate how often to expect this kind of perfection. If the board is a single-, double- or easy four-layer item, then a PCB buyer should expect – in fact, should demand – the manufacturer deliver panels free of defective boards.

However, if it is a higher technology – such as an HDI design – scrap will happen in every manufacturing lot. To expect otherwise is not realistic.

Any experienced PCB supplier knows this custom-made item – requiring more than 100 different manufacturing processes – will have a board (or boards) with some sort of rejectable imperfection in every manufacturing lot released to the floor. To address this issue, before the board order hits the production floor, the fabricator will release an overage, depending on the board's technology, to ensure its manufacturing processes yield the number of boards required to fulfill an order.

The more high-tech the board is, the more overage may be necessary to account for any fallout.

For example, let's say 1,050 pieces are released to meet an order requiring 1,000 individual boards. In this case, the manufacturer decides a board's technology will require only an additional 5% in materials overage.

At final QC, the vendor then finds 32 pieces (or about 3%) did not make it through the manufacturing process for various reasons. Those bad boards are scrapped.

Because a 5% overage was produced, 1,018 pieces are good. So, the 1,000-piece order is shipped as promised, and the additional 18 pieces are put into finished spares. Everyone is happy, with most customers not paying any attention to the fallout that occurred within that overage amount.

Sometimes, though, having PCBs delivered in an array or panel format might highlight manufacturing challenges, especially when a customer has a "No X-out" policy.

If you put that same order in a four-up array, then 250 arrays would need to be perfect to meet the 1,000-piece requirement. Based on those numbers for that technology, the manufacturer could expect the same percentage of fallout. But boards found at final QC that don't pass muster are "connected" to three pieces that passed with flying colors. This means 32 arrays with an X-out or 128 pieces total (32 x four-up) are not allowed to ship, regardless of their quality.

The vendor must release more overage (about 15%, or 152 pieces, because it's a four-up array) to accommodate the normal fallout that occurs during the manufacturing process for arrays that can't have any X-outs.

Whether your company accepts X-outs or not should be detailed in your firm's PCB fabrication specifications. This information will guide your board suppliers on how much material (overage) they must release – based on their technical capabilities – to fulfill an order.

Here is an example of an EMS company's X-out policy that is clearly spelled out:

"X-outs are allowed. However, not more than 20% of the PCBs in the array can be X'd-out, and no more than 10% of the arrays to be shipped may contain an X-out."

This means if you have, say, a 2,000-piece order manufactured in a 10-up panel requiring 200 arrays to be received, the most you should receive is 20 panels that contain no more than two X-outs each.

Your fabrication specs should also state how X'd-out panels are to be received to avoid causing headaches for both receiving and production departments. A statement like this works:

"X'd-out arrays are to be segregated and identified accordingly at time of shipment."

PCB buyers should keep in mind the amount of real estate needed for perfect arrays (no X-outs) means the overall cost of the board will be higher. The adage about not allowing the perfect to become the enemy of the good is applicable here.

Before your company sets its X-out policy, sit down with your manufacturing department. There are ways for an assembler to handle manufacturing panels with X-outs, but the department responsible for shipping quality, finished assemblies should have final say on X-outs.

A rigid "No X-out" policy will likely cost you more without improving the PCB manufacturing process. In most cases, a more flexible approach is warranted. □

**GREG PAPANDREW** has more than 25 years' experience selling PCBs directly for various fabricators and as founder of a leading distributor. He is cofounder of Better Board Buying (boardbuying.com); greg@boardbuying.com.

# PCB Surface Finishes: When to Change It Up

The primary purpose of surface finishes is to prevent oxidation of the copper prior to soldering components.

BACK WHEN I held a soldering iron, we used a mixture of tin (63%) and lead (37%) for the solder (Sn63). The boards had the same coating on the plated holes and surface-mount pads. The application for surface mount is referred to as hot air solder leveling (HASL) and applies to any of the available solder types. The beauty of Sn63 is it has a lower melting point and is eutectic. "Eutectic" means the metal solidifies rapidly over a short temperature range. The benefit is fewer disturbed solder joints and good "wetting," where the surface finish and the solder form a cohesive bond for a reliable connection. You can still buy Sn63 off the shelf at the local electronics store.

On the other hand, lead is a dangerous metal that can cause birth defects and other health issues. The Europeans took the vanguard with the RoHS initiative. If you want to sell electronics products to consumers, the lead content must be the minimum possible – not eliminated entirely but found primarily as a trace element within chips.

SAC (Sn-Ag-Cu): a heroic alloy. Metallurgists all over the world looked for replacement formulas. Tin is still viable and is generally mixed with small amounts of silver and other elements such as antimony, copper or bismuth. Tin makes up the bulk of the alloy, typically around 95% to 99.3%. If pure tin was used, the results could be problematic. Tin whiskers from dendritic growth present a shorting risk.

Without lead, tin has a much higher melting point and does not solidify as quickly. The double-complication requires a dielectric material that can withstand the higher temperatures without breaking down.

The maximum working temperature of the material is one of the primary selling points. It is known as the glass transition (Tg) temperature. The materials we used in the old days did not stand up to the process, so the entire PCB material set had to be seriously upgraded. Going lead-free raised the reflow temperatures considerably. Boards and components alike have gone green since then.

Exemptions exist where tin-lead is still allowed. Spacecrafts that will eventually burn up on reentry are one such exemption. The goal of RoHS is to reduce the amount of lead that goes into the landfill. Provided the company can certify all its products will be returned to

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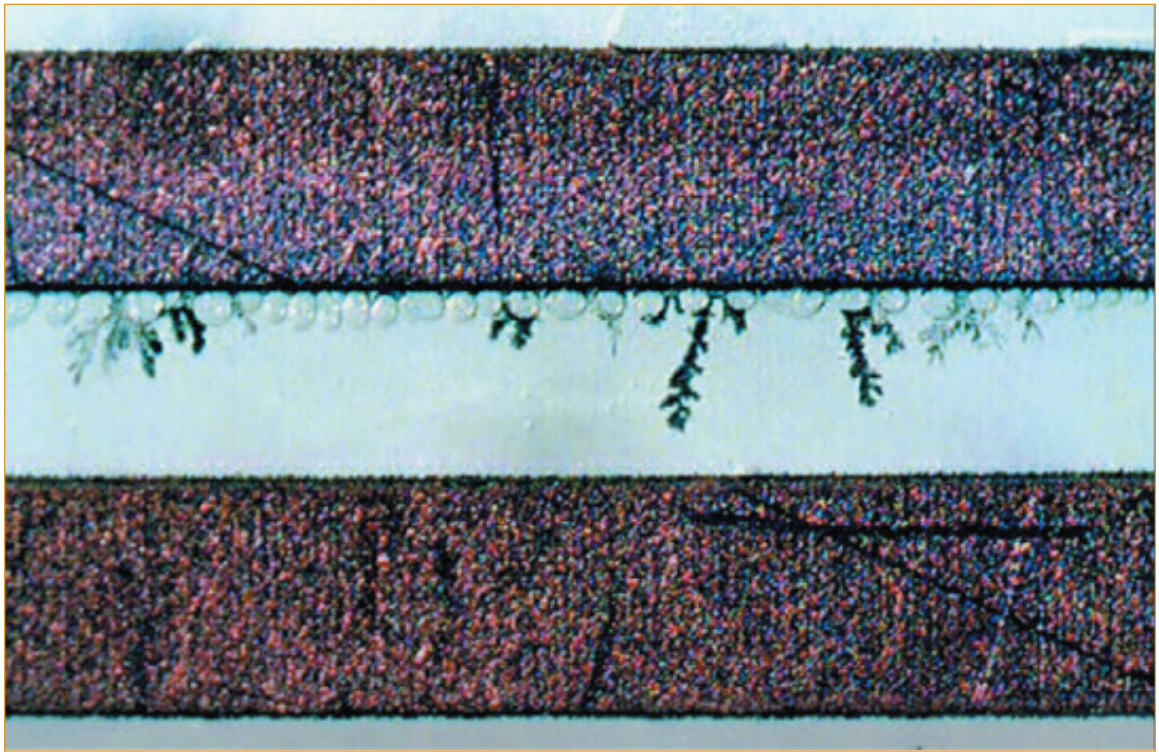

**FIGURE 1.** Pure, non-alloyed metals exhibit crystalline growth as the metal forms branches over time. Environmental conditions can aggravate the process. *(Source: NTS Corp.)*

the factory for proper disposal, Sn63 coatings on the PCB are permissible. Obviously, consumer products do not get such an exemption.

ENIG: the gold standard. While tin-silver plating is still viable, the "gold standard" is gold. The mainstream alloy is immersion gold over electroless nickel over copper, or ENIG for short. The reason this is a preferred plating is the downstream process of assembly is more boring without the likelihood of tin whiskers. We like it to be boring when it comes to making goods. Those who study S-parameters also have a fondness for the consistency of ENIG finishes.

This plating is primarily aimed at high-density interconnect fabricators. The process can yield a solderable footprint with via-in-pad situations. Fine-pitch BGAs and other shrunken circuits require microvias. Plating with ENIG will likely improve yields due to the land patterns coming out flatter than with other types of plating. It's also a go-to finish for flex circuits. It plays well with solder mask, making a good base for the following layer.

A note on "black pad": This process defect was a hot topic for a few years. That time has passed. The fabricators worked out the right amount of phosphorus in the nickel to prevent the defect that was more than a cosmetic issue. That concern was laid to rest.

ENIPIG: not too hard, not too soft. Electroless nickel, immersion palladium, immersion gold adds palladium as a physical barrier between nickel and gold. That opens up the process. The main benefit to ENIPIG is the outer layer of gold is soft enough to be a good candidate for wire bonding, while still working well for soldering. The alternative for chip-on-board is a selective soft gold finish: the do-everything finish.

When selecting the correct finish, know the constraints. While ENIPIG has an upcharge, it's not as expensive as soft gold or hard gold when used in combination with medium gold. Note medium hardness is geared for solderability, while hard gold creates a more durable contact surface for "gold finger" edge connectors. To meet the specification for HDMI, the gold fingers must withstand 10,000 insertion/extraction cycles.

OSP: a minimalist approach. Organic solderability protectant is a very thin coating consumed by the reflow process. In the factory, we had to be aware of the date codes on boards with OSP. You don't want old boards with this coating.

During design, when reaching back to padstack definitions, the designer must coordinate something extra when using OSP. We had to include a paste stencil opening on our test points when the boards had OSP, or the test points would end up with bare copper. The exposed copper will tarnish over time. None of the other finishes have this requirement.

An IPC specification for OSP (IPC-4555) is on the horizon. Per a report on this publication's website in August 2020, "The goal is to develop performance specifications for high-temperature OSPs, defined as capable of withstanding up to two IR reflows in conjunction with tin-silver-copper (SAC) or tin-bismuth (SnBi) alloys at a peak temperature of 245°-250°C and showing the same wetting balance results at three reflows as zero, with a maximum 20% drop."

This is good news since OSP is well-suited to mass production runs. The micro-thin coating does not hinder solderability. The cost is low, along with the shelf-life. Organic solderability protectant has been around for quite some time with proprietary processes, so it will be beneficial to have a performance standard across the board. ❑

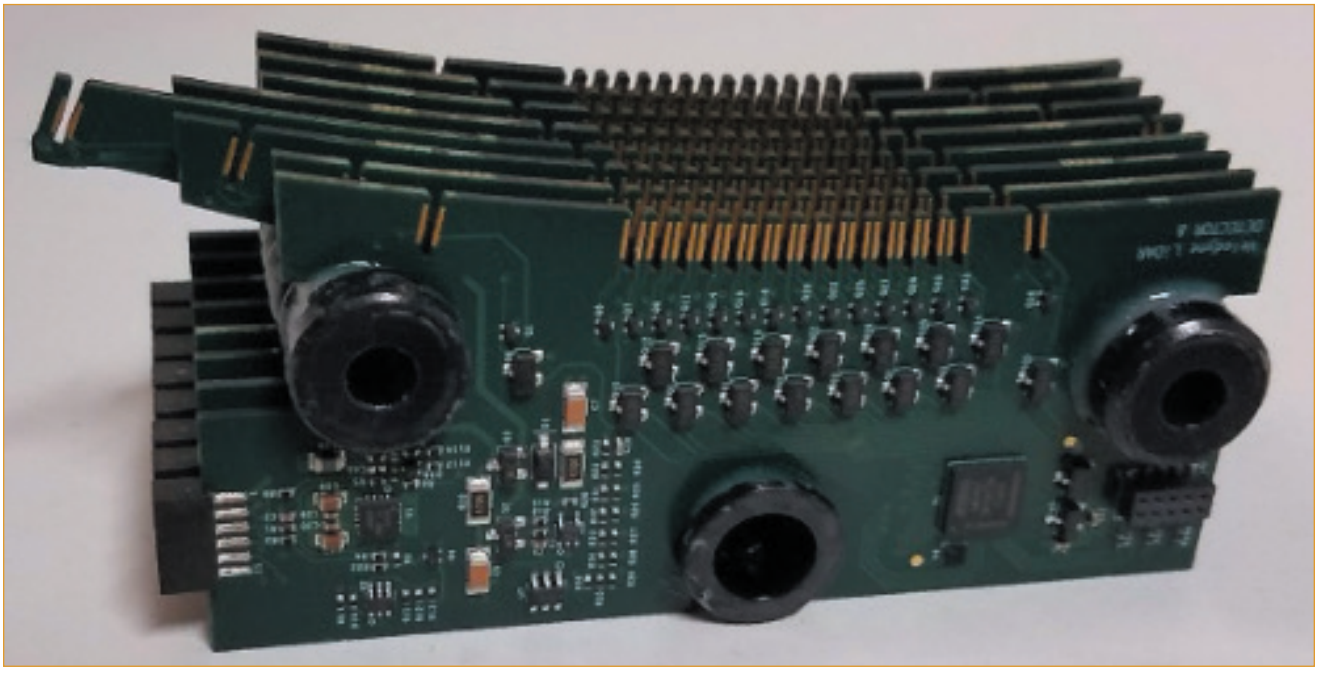

**FIGURE 2.** ENIG finish with through-hole vias and surface-mount components.

# Alternate Reality is Getting Very Real

The metaverse offers opportunity for escapism and empowerment.

MARKET RESEARCH PUBLISHED last summer suggests the total AR/VR market will top $700 billion by 2025, suggesting a compound annual growth rate close to 75%. Those are amazing statistics, although we know investment in virtual and augmented reality has surged during the pandemic. Spending on VR has increased, particularly among consumers constrained to stay at home for extended periods. They have time, and they're bored. But professional applications are also expanding quickly in marketing, retail, healthcare and manufacturing.

As a concept, AR/VR is closely connected with another emerging phenomenon: the metaverse. The distinction between the two is quite blurred. The metaverse is perhaps best envisioned as an alternative reality whose scope extends throughout the entire internet and into the real world. Although there will be elements of virtual reality, and a VR headset will provide one means of entering the metaverse, the big tech giants are thinking much bigger. Facebook's parent company has even changed its name to Meta, a clear expression of its ambitions.

We can expect this alternative reality to start becoming accessible through gaming and entertainment applications. People will exist and move around as avatars, go to shops, attend concerts. The chance to style our appearance and create our own reality is a fantastic opportunity for escapism. And who could blame anyone seeking an escape from the *real* real world?

Important opportunities exist to improve our working lives, however, as well as the quality of services such as healthcare and emergency first response. With the benefit of instant access to building records through the internet, police or firefighters can capture information about the layout, occupants and fire-escape routes within their field of view to preserve their own safety and provide more effective support to those inside.

The opportunities to enhance mental well-being are perhaps even more profound, particularly in the aftermath of the pandemic. The numbers of people suffering from anxiety-related disorders such as agoraphobia are expected to have increased. Those already suffering, having been compelled to stay indoors for extended periods, will likely have experienced setbacks in their battle. The metaverse could greatly expand the prospects for treatment by providing a controlled environment for a patient to enter, move around in, and deal with challenges that are carefully designed to help build confidence.

In a similar vein, metaverse technology can have a democratizing effect on formerly specialized areas of research, like sports performance. Elite sportspeople are known to employ visualization to prepare mentally for high-pressure events. Rehearsing their responses helps fine-tune performance and strengthen the self-control to achieve their ultimate goal. The desire for outstanding achievement is common, yet few can get the right help to use visualization effectively. The metaverse can provide a suitable environment to try it out, with the aid of online courses delivered by your own personal coaching avatar.

*continued on pg. 70*

**FIGURE 1.** Expect VR headsets to use flex circuits and IMS to reduce size and improve thermal management.

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# Rogue Wave Estimation in PDNs Using the MULTI-TONE TECHNIQUE

Effective strategies for calculating rogue wave noise levels.

by ISTVAN NAGY

For about 20 years, PDN design and analysis focused on the target impedance method. In recent years, additional considerations surfaced about rogue waves, but more as a general discussion. Here we present a new design/analysis method for estimating rogue wave amplitudes we can compare against the digital chip specs for design verification.

Electrical designs must be verified against possible worst-case conditions. For power distribution networks (PDN digital chip supply rail), this is typically done by comparing their impedance profiles against a target impedance requirement. From recent research and publications, we know the target impedance method for analyzing PDN design does not always predict the worst-case noise voltage because different frequency components of the chip supply current load steps can superposition on top of each other. This is sometimes called rogue waves (RW).

The industry has been evaluating different approaches to dealing with RWs: for example, adjusting the target impedance or flattening the impedance profile. Adjusting the target impedance is not sufficient because cases can occur when an adjusted target impedance is already met by the original design's impedance profile, but it still fails with RW noise amplitude that's too large. The whole impedance profile would need shifting down, not just the target impedance line. That is not easy to do. Achieving flat impedance profiles ($Q < 0.5$) on real digital designs is impractical. For a board designer, a more practical approach is useful to help with the initial component selection and checking the design at the early stage (when the schematic is being drawn) for a pre-layout pass/fail criteria, while not yet considering spatial or post-layout data.

In addition to the target impedance crossing criteria, additional criteria are needed for the designer, namely checking whether the worst-case noise amplitude (RW) is larger than the maximum allowed noise or not by using a crafted worst-case excitation waveform in simulation. We can perform this new type of check by computing the required excitation from the simulated PDN impedance profile. A known method for this is the reverse-pulse technique (RPT) that computes a wide band waveform consisting of rectangular load stepping with specific timing detail. This method requires the use of FFT/IFFT and accurate integral calculus to generate a step response, only correct if the PDN impedance profile was sampled in a linear fashion down to DC. That poses computational resource challenges and is impractical for everyday design projects.

This article introduces new methods. First is the case of implementing the RPT with a log-scale impedance profile that can be computed on 1,000 samples instead of millions of samples, but it is inaccurate. On 1,000 time domain samples (post-IFFT), we could not accurately display both a 100MHz and a 100Hz waveform. We investigate how inaccurate it is, or whether the inaccuracy might be acceptable in practical digital design cases.

The other new method is the multi-tone technique (MTT)

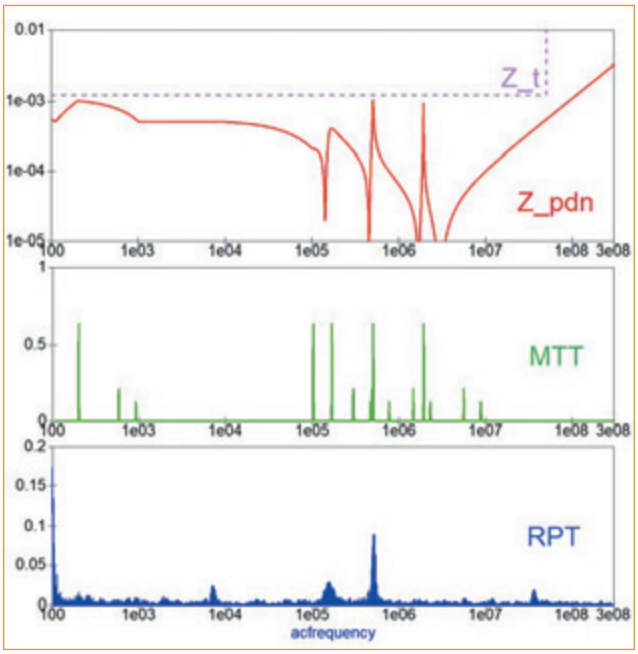



**FIGURE 1.** Spectrum comparison of MTT and RPT excitation waveforms, both computed from the same impedance profile.

that detects the frequencies of the impedance profile peaks and automatically places periodic excitations to each peak. This works on log or linear scale and does not require FFT or accurate integral calculus, but produces a theoretical signal. It is more like a system vulnerability check, rather than an actual test vector like the RPT.

Both the MTT and RPT seem to "attack" the PDN impedance profile at high-impedance areas, but with different strategies **(FIGURE 1)**. MTT only focuses on peaks. RPT has a complicated distribution partly focusing on peaks, plateaus and other areas. On digital board VDD rails, we don't see multiple sinusoidal excitations. Instead, we have load current stepping/toggling between two levels. From recent publications, we know rogue waves can be created like this: The PDN can be excited with one toggle rate or frequency; it resonates. Then we suddenly change the toggle rate while the system is still resonating on the old frequency on stored energy (forced response), so the voltage response to the old and new frequency are super-positioned to create a larger wave: a rogue wave.

Likely the main requirement of an RW is to present different frequencies at different times, sequentially, relying on recent remnants of resonance from stored energy. The target impedance method only ensures a single frequency component will not cause larger than the allowed voltage disturbance (percentage of VDD). To test and demonstrate different features, phenomena and corner cases, the PDN model had to be tuned differently with different capacitor and VRM parameters.[1,2,3,4]

Further, it will be demonstrated how these complex procedures can be automated with a single software tool: either Keysight ADS or the open-source QUCS. They serve as circuit simulators, SI-simulators and Matlab-like mathematical computational engines in one, allowing us to create custom equations and waveform processing. Normally we create templates, then reuse them in design projects.

The quality factor (Q) describes how under-damped an oscillator or resonator is. It is the ratio of the energy stored in the resonator to the energy lost in one radian of the cycle of oscillation. With higher Q peaks on the impedance profile, the oscillations die out more slowly. This means it oscillates longer, while the load switches the excitation to another resonant frequency that in turn increases the chances of creating a rogue wave. This is why often there is a focus on flattening the impedance profile to prevent the resonances from lasting too long. If we want energy loss to 0.1x in half period (3.14rad), then a Q < 1/(1-(0.1^(1/pi))) = 1.92 limit is required. For 0.2x energy remaining, we would need Q < 1/(1-(0.2^(1/pi))) = 2.5 limit. That is often achievable with 100nF or larger capacitors, but 0.2x remaining amplitude after half-period is not a guarantee to zero rogue waves. Our simulation template can check for Q factor between capacitor value pairs analytically. This does not compute the RW voltage amplitude; it provides a vague measure for RW probability.

$$Q12 = sqrt((ESL1+Lmnt1)/C2)/(ESR1+ESR2)$$

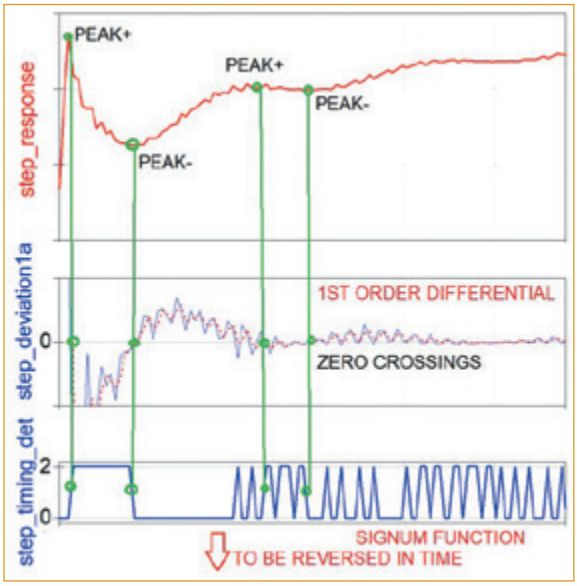



**FIGURE 2.** Timing extraction in RPT.

## The Reverse-Pulse Technique

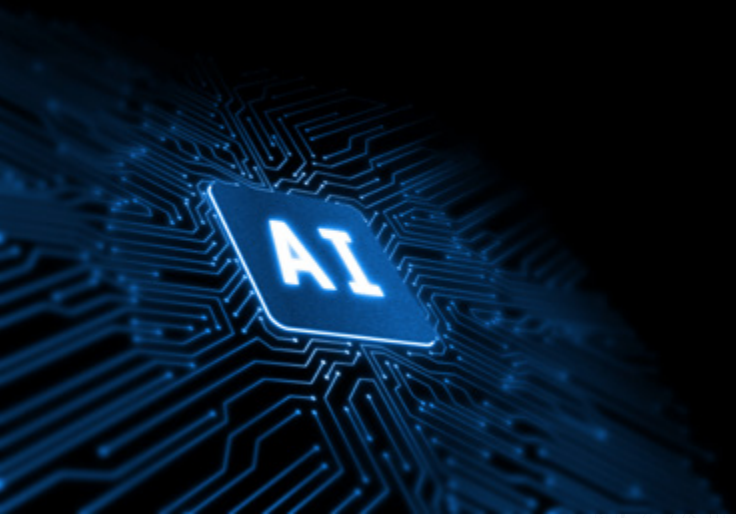
A more common method for worst-case voltage response, or rogue wave computation, is the reverse-pulse technique (RPT). This requires FFT, IFFT, differential, integral and time (vector) reversal computations that would only be correct or accurate when using linear sampling on both the frequency and time domains. With logarithmic frequency sampling, we expect huge inaccuracy or distorted curves, but the spectrum of the excitation waveform aligns exactly with the peaks and high-impedance areas on the impedance profile, so maybe it is not that bad. A linear scale RPT down to DC would require at least 100,000 or, more likely, millions of frequency points to have decent resolution at a wide frequency range that is prohibitive in most simulation tools, especially the free ones. The way RPT is described requires an experienced engineer to assess waveforms, enter data manually, make decisions and use multiple tools.

This could also be automated using post-simulation equations in Keysight ADS or in the open source QUCS.

One attempt to compute a 100,000-point linear scale RPT on QUCS resulted in the simulation freezing at the vector reversal operation. Further simulations were conducted using a reduced bandwidth, reduced sample size, linear sampled RPT between 10kHz and 10MHz, plus a DC point on 1,000 points (10kHz even spacing) run in five minutes on a low-power laptop. Assuming a flat plateau created by VRMs, the DC value was the real value of the lowest frequency sample (10kHz).

The impedance profile as a numeric vector, or "waveform," is processed through several steps to get the voltage response. From the AC circuit simulation result, the complete complex conjugate symmetrical spectrum with DC component had to be constructed at the size of 2^n or 2,048 samples for the FFT/IFFT to work correctly; that requires a 1,023-point AC simulation. The symmetrical spectrum as a vector was built as [real(Zpdn[0]),Zpdn,0,conj(Zpdn_rev)]. First we compute the step response:

$$[AC\text{-}sim] \rightarrow Z\_pdn(f) \rightarrow [BW\text{-}limit] \rightarrow [symmetrize] \rightarrow [IFFT] \rightarrow Impulse\ Response(t) \rightarrow [Integral] \rightarrow Step\ Response(t)$$

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Then detect the voltage fluctuation timing on the step response; then create a toggling load step waveform; then reverse the timing of it (vector reversal). This is the excitation. In the QUCS template, the timing extraction **(FIGURE 2)** was done by computing the 1st order differential calculus of the step response, then chopping it up with a comparator (using the signum function). In other words, the positive and negative peaks are turned into zero crossings, then vertical edges of a square waveform. Then we can compute the response to that excitation:

$$Excitation(t) \rightarrow [FFT] \rightarrow Excitation(f) \rightarrow [Multiply\ by\ Z\_pdn(f)] \rightarrow [IFFT] \rightarrow Noise(t)$$

Finally, we can measure the amplitude of this noise waveform by computing the maximum value minus the minimum value. All RPT equations can be seen in **FIGURE 3**.

| Name | |
|---|---|
| z | Z_pdn*bw_limit2 |
| z1 | [z[1022],z[1021],z[1020],z[1019],z[1018],z[1017],z[1016],z[1015],z[1014] |
| z2 | [z[799],z[798],z[797],z[796],z[795],z[794],z[793],z[792],z[791],z[790],z[7 |
| z3 | [z[599],z[598],z[597],z[596],z[595],z[594],z[593],z[592],z[591],z[590],z[5 |
| z4 | [z[399],z[398],z[397],z[396],z[395],z[394],z[393],z[392],z[391],z[390],z[3 |
| z5 | [z[199],z[198],z[197],z[196],z[195],z[194],z[193],z[192],z[191],z[190],z[1 |
| Z_pdn_upp | conj([z1,z2,z3,z4,z5]) |
| zavg | (integrate(abs(z),1))/1023 |
| Z_pdn_ds | [real(z[0]),z,0,Z_pdn_upp] |
| impulse_response | ifft(Z_pdn_ds) |
| step_response | cumsum((impulse_response)) |
| step_deviation1a | diff(abs(runavg(step_response,3)),acfrequency,1) |
| step_timing_det | (1-sign(1*(step_deviation1a-0))) |
| r | 1-0.5*step_timing_det |
| r4 | [r[399],r[398],r[397],r[396],r[395],r[394],r[393],r[392],r[391],r[390],r[389] |
| r5 | [r[199],r[198],r[197],r[196],r[195],r[194],r[193],r[192],r[191],r[190],r[189] |
| step_timing_rev | [r4,r5,linspace(0,0,624)] |
| excitation | [step_timing_rev,step_timing_rev] |
| excit_freqd | fft(excitation)/2048 |
| voltage_spectrum | Z_pdn_ds*excit_freqd*delta_current |
| noise_wf | (ifft(voltage_spectrum))*2048 |
| noise_wf_displ | real(noise_wf) |
| noise_wf_ampl | max(noise_wf[10:900]+1)-min(noise_wf[10:900]+1) |
| noise_rpt | noise_wf_ampl |
| pass_rpt | ((noise_rpt/spec_max_wf)>1)?0:1 |

**FIGURE 3.** RPT equations.

Limitations. Sometimes the RPT picks up on the very high-frequency end, but that is not realistic; it's overly pessimistic because every digital board PDN has very high impedance at very high frequency. In fact, they have infinite impedance at infinite frequency. The solution is to decide the frequency range of interest and bandwidth limit of the impedance profile before allowing it to be processed by either RPT, MTT or another technique. This also makes sense for simple target-impedance checking, as the impedance profile will cross the target impedance line at high enough frequency no matter what. The examples above were between 10kHz and 10MHz, so this issue didn't occur, but on real design verification, we often go up to 50 to 500MHz with the analysis. Very few chip datasheets mention this bandwidth limit. If they do, it is typically 20 to 50MHz. My final QUCS template implements a bandwidth limiting function.

While testing different PDNs with LOG-RPT, especially the smoother ones, it was observed the time domain waveform seems to fly off near the last samples, causing the peak voltage measured to be higher than the main fluctuations seen throughout most of the waveform. This is likely a computational artifact. We can apply a window function on the waveform and only check the maximum and minimum peak values in the middle 90% of the samples.

In a test done with both QUCS AC-sim and LTspice transient simulation, the windowed version seemed closer to the Ltspice results. There was no VRM in this model, as LTspice does not support S-parameter files. In Ltspice we get a step response curve. By measuring the first two positive and first negative peaks, we can calculate the rogue wave amplitude as described in the original reverse pulse technique. Ltspice uses linear time sampling and no transformations, so it's accuracy can be used as a reference, except it cannot handle measured VRM S-parameter models, so Ltspice is only useful here as a method reference with an RLC PDN model, not for real design validation.

$$Vnoise = Vpp1+Vpp2-Vpn1$$

## The Multi-Tone Technique

The MTT avoids the accuracy (in logarithmic scale) or computation resource (in linear scale) issues within the reverse pulse technique (RPT) and provides a simple, fast way for a board design engineer to check the design for rogue waves with a pass/fail output. MTT sums up all the peaks (tones) multiplied by the load step automatically, then checks if the RW amplitude is larger (fail) or smaller (pass) than the max allowed noise from the datasheet. The MTT assumes these "tones" will be applied sequentially to the DUT, relying on stored energy, creating the rogue wave. Therefore, it is inappropriate to compute a time domain waveform from it using IFFT due to the inaccuracy of the logarithmic sampling and the lack of sequencing.

The noise voltage is:

$$Vnoise = Zpdn(f1)*Idelta+ Zpdn(f2)*Idelta$$

While the maximum allowed peak voltage is given as a percentage of the VDD voltage:

$$Vmax = VDD*tolerance\%$$

Then the target impedance line is:

$$Ztarget = Vmax/Idelta$$

Instead of manually reading the frequency values of the peaks from an impedance curve, we can automate all that with waveform processing equations while remaining in the frequency domain. That is the point of the MTT. Since this method does not use FFT/IFFT or normal differential or integral calculations, accuracy should not be an issue. In regular differential and integral calculations, the resulting sample values are dependent on the gap width between the samples. Therefore, the gap must be accurately accounted for in appropriate units (Hz or ns), and each gap must be equal. None of the calculations below care about the gap widths. We only use differential computation to obtain frequency information for the creation of frequency domain Dirac Delta pulses, not to obtain accurate voltage levels. Accurate voltages are obtained through simple multiplication. We only do integral calculation to sum the levels of a few Dirac-like pulses, regardless of the frequency separation between them. It is more of an intentional misuse of integral calculus.

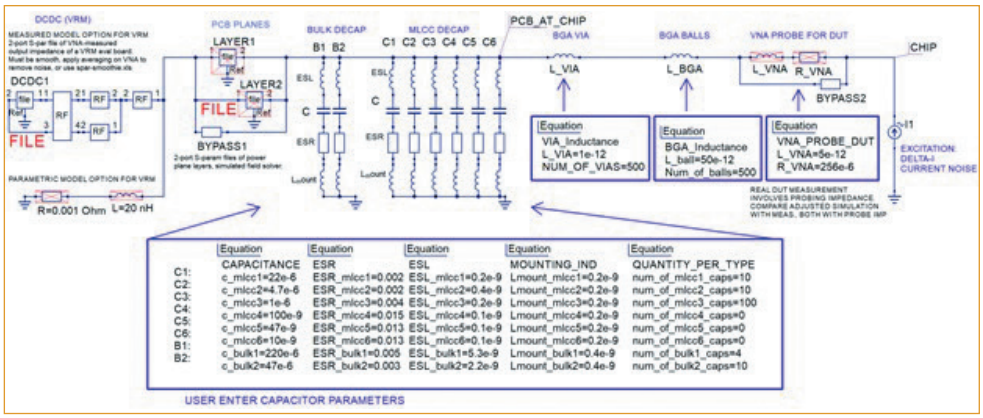


**FIGURE 4.** AC simulation model schematic, complete PDN.

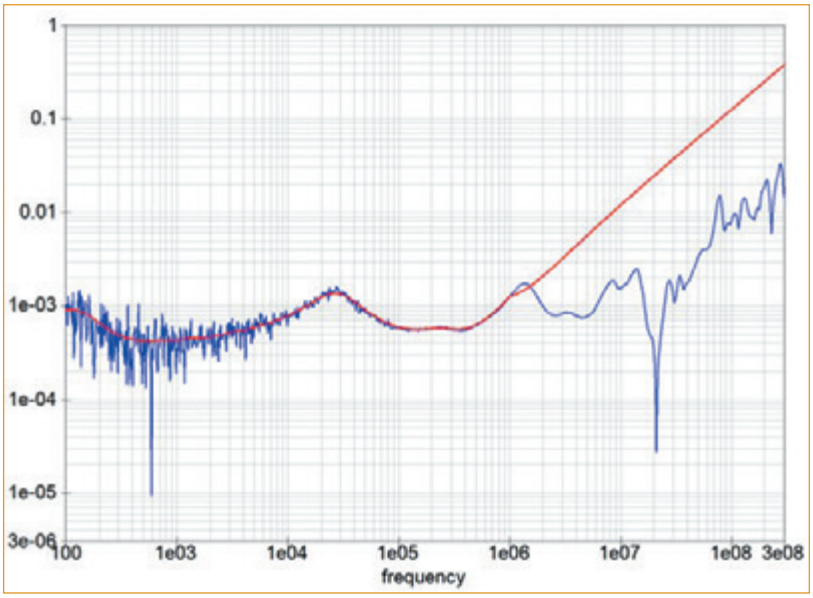


**FIGURE 5.** Post-processed version of a measured VRM model, with smoothing and high-frequency cutoff (at 1MHz).

Step one: System model and simulation. Simulate the PDN model using the AC simulation feature. The system model in a schematic format in **FIGURE 4** consists of a 1-amp AC current source excitation at the chip, capacitors provided as RLC parameters and S-parameter models for VRM (measured with VNA or manually created S-par file) and PCB power planes (from any 2-D field solver, a rectangle with estimated major X/Y dimensions). The VRM model would ideally be measured on a chip vendor's evaluation board after we have carefully removed all smaller decoupling capacitors. We can post-process the S-parameter file in a partly automated Excel template created for this, with averaging or filtering – or replacing the upper frequency range with a 20dB/d slope. We could alternatively use a theoretical handwritten VRM S-parameter file. Several were provided with the template. The equation-controlled RF block converts the shunt through a 2-port S-parameter file of the VRM into a 1-port impedance part.

The measured S-parameter models of VRM evaluation boards are usually very noisy, with hundreds of sharp peaks and valleys (grass) that confuse the MTT algorithm. To mitigate that, we must take the measurements with strong averaging or filtering to smooth the curve or post-process (smoothing) the measured model with an Excel file (created for this project and template) before inserting it into the PDN template. It also makes sense to completely replace (cut off) the higher frequency portion with a 20dB/decade inductive slope above a user-selectable threshold. Its desired effect can be seen in **FIGURE 5.** Both the smoothing and the cutoff are partially automated using an Excel template included with the QUCS template.

Step two: Intermediate results. The simulation result is a Z_pdn(f) impedance profile stored inside the simulation tool as a vector with 1,023 elements as complex impedance values at distinct frequency points. An example can be seen in **FIGURE 6** that uses a simple manually created theoretical VRM model, instead of using

*continued on pg. 40*


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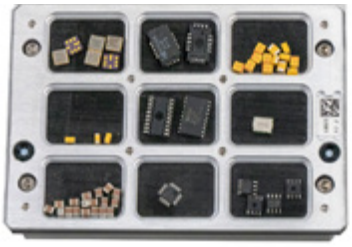

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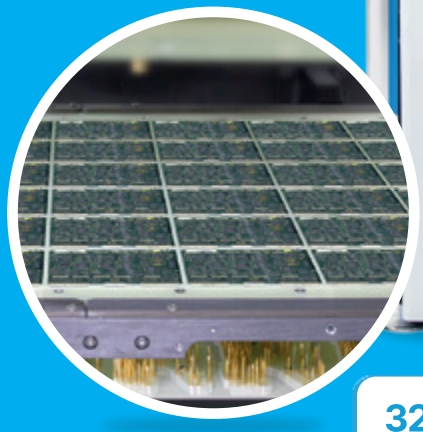


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*Rogue Wave, continued from pg. 25*

the measured VRM model. The capacitor values were tuned for demonstration purposes such that several peaks almost touch the Z_target line, not violating it, but they will violate maximum noise due to rogue waves, as we will see later.

**Step three: Post-process the waveforms.** In both ADS and QUCS, we place the equation component in the schematic that can contain multiple equations for computing and transforming post-simulation waveforms. We create waveforms from waveforms. After several steps, we can do a min./max. measurement to get the information we seek, like peak voltage. This is a creative process. **FIGURE 7** shows the series of equations, while **FIGURE 8** shows the intermediate waveforms graphically.

First we compute a discrete differential of the impedance profile by subtracting each sample from the previous sample. Then we magnify the results excessively to create vertical-looking edges (and zero-crossings) at the same frequencies where the impedance profile had peaks. Then we cut off the waveform at +1 and -1 levels using the signum function. After this we create a waveform that has little Dirac Delta 1 sample-wide pulses, where previously we had edges, using another discrete differential. Now we have negative Dirac pulses at the parallel resonances and positive ones at the series resonances, plus one pulse at the lowest frequency (to be removed).

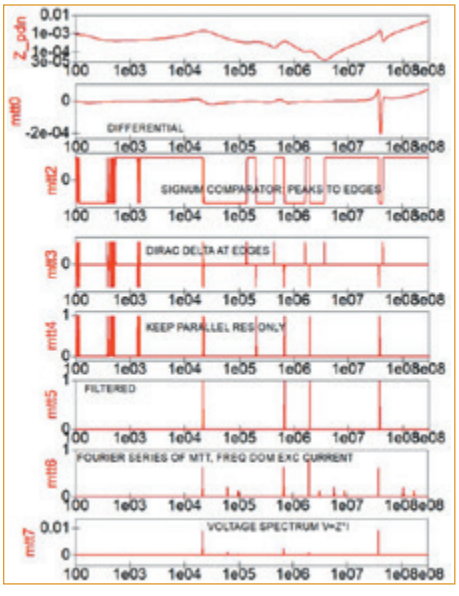


**FIGURE 8.** Intermediate waveforms from the equations.

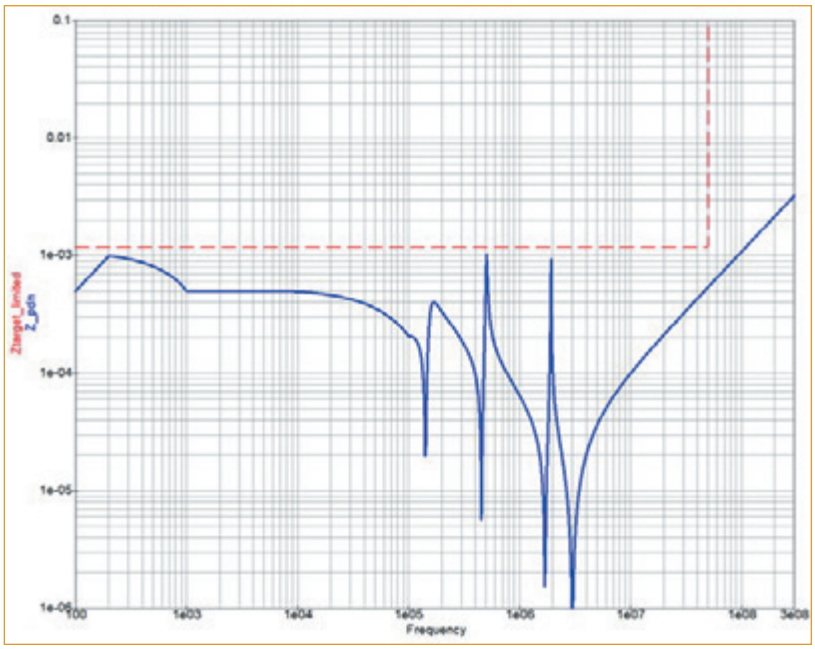


**FIGURE 6.** A complete PDN impedance profile with limited target impedance and manual VRM model.

| Name | Value |
|---|---|
| mtt0 | abs(Z_pdn[0:1022])-abs([Z_pdn[0],Z_pdn[0:1021]]) |
| mtt1 | mtt0*1e15 |
| mtt2 | sign(mtt1) |
| mtt3 | ((([mtt2[1:1022],mtt2[1022]])-([mtt2[0:1022]]))) |
| mtt4 | 0.5+0.5*(sign((-1)*mtt3-0.1)) |
| mtt5 | mtt4*FILTER8 |
| mtt6 | [0,0.636*mtt5[1:1022]]+0.212*[linspace(0,0,74),mtt5[1:949]]+0.127*[linspace(0,0,105),mtt5[1:918]] |
| mtt7 | abs(Z_pdn)*bw_limit*abs(mtt6)*delta_current |
| mtt8 | max(cumsum(mtt7)) |
| pass_mtt | ((mtt8/spec_max_wf)>1)?0:1 |
| noise_mtt | mtt8 |
| pass_z_mtt | PASS_Z*pass_mtt |
| FLT_THRSHLD | 0.5 |
| FILTER1 | [(min(Z_pdn[1]))*linspace(1,1,50),Z_pdn,(Z_pdn[1022])+((Z_pdn[1022]-Z_pdn[1021])*linspace(0,100,100))] |
| FILTER2 | runavg(FILTER1,101) |
| FILTER3 | ((((abs(Z_pdn)-abs(FILTER2)))/abs(FILTER2)) |
| FILTER4 | mtt0*(0.5+0.5*(sign(mtt0-1e-12)))*(1/(abs(FILTER2)*3000)) |
| FILTER5 | ([FILTER4[0:1022]]+[0,0,0,FILTER4[0:1020]]+[0,0,0,0,0,0,0,0,0,FILTER4[0:1017]]) |
| FILTER6 | 0.5+0.5*sign(([mtt4]-[0,0,mtt4[0:1020]]-[0,0,0,mtt4[0:1019]]-[0,0,0,0,mtt4[0:1018]])-0.5) |
| FILTER7 | FILTER3*FILTER5*FILTER6*(0.5+0.5*(sign(FILTER3*FILTER5-1e-12))) |
| FILTER8 | 0.5+0.5*sign((FILTER7*1e6)-FLT_THRSHLD) |

**FIGURE 7.** The equations for the MTT.

After this we flip the curve upside down and eliminate the series resonances. This waveform is basically the excitation with multiple tones, but we need to apply two more steps: filter out the Dirac Delta pulses at the small impedance wrinkles and apply a Fourier series to make it more realistic. This is the load current spectrum of the excitation. Then we compute the voltage spectrum seen on the PDN as V = Z_pdn*excitation*Idelta*bw_limit.

Finally, we compute the sum of all voltage peaks using cumulative sum (integral), also known as the superposition of all resonant voltage response waves. We then compare the noise amplitude against the original datasheet specification and determine whether the design is a pass or a fail.

Even using a post-processed, smooth VRM S-parameter model, the impedance profile still has hundreds of micro-peaks (wrinkles) that throw off the MTT algorithm. To mitigate that, a FILTER algorithm was created that only allows big and sharp peaks. It computes the peak height at the detected frequencies

(through relative impedance deviation, distance from a moving average); it computes its sharpness (steepness of the left side of the peaks through differential and a shift) and removes duplicate peaks. Then a carefully selected threshold is applied to ignore the smaller peaks. Finally, the filter is applied halfway in the MTT process, and only the more pronounced (tall/sharp) peaks make it into the final spectrum.

Digital board PDNs are not excited with sine waves. We only have digital chips generating load current steps or toggling, like a square wave or a pulse sequence. For a square wave, only about half the energy is applied at the toggling frequency, so the MTT tones should be reduced and replicated at 3x/5x/7x harmonic frequencies with 2/n*pi amplitudes, as a Fourier series. The main tone is 0.636 high; the 3f tone is 0.212 high with a 73-sample shift (when using 100Hz to 300MHz on 1,023 samples); the 5f tone is 0.127 high with another 30-sample shift, basically dispersing the energy in the spectrum to be more realistic.

Using a linear sample shift as frequency multiplication only works in log scale simulation, so a LIN-MTT with Fourier series would not be accurate. Both the original MTT – and even the target impedance method – wrongly assume the full energy of a single toggle rate excitation can appear 100% at a single frequency point. So, the MTT is adjusted with the Fourier series. Note the target impedance method also needs relaxing for the same reason, by raising Ztarget by 57%, even though we never do that for the sake of simplicity.

In one example (100Hz-300MHz, LOG 1,023 points), we got 26.7mV rogue wave amplitude with MTT and 16.1mV with RPT. This impedance profile in Figure 6 should not result in anything higher than 12mV noise, since the whole curve is under the target impedance line that was computed assuming 12mV noise (VDD*tolerance%). But it does, due to rogue waves created by a multi-frequency excitation at the parallel resonant frequencies.

## A Comparison

A final relative percentage deviation table between four methods (16 combinations) was simulated using parameter sweep at 18 component value combinations in a reduced range between 10kHz and 10MHz on 1,023 points. Both linear and logarithmic frequency sampling were used. The capacitor values were adjusted as 0.1x-1x-10x in a parametric sweep simulation. One capacitor remained constant, and two manually created theoretical VRM models were used: 0.25mΩ and 2.5mΩ plateau. It seems the different types resulted in very different noise levels, as seen in **TABLE 1.** The logarithmic RPT and MTT can differ as much as 67%, but, in most cases, around 20%. The LIN/LOG MTT differ a few percent only as a result of the interpolation of the VRM model.

## Automated PDN Design Through Optimization

With pass/fail variables for the rogue wave amplitudes and target impedance, we could create a simulation that automatically adjusts capacitor quantities, instead of values – as it's more practical from a selection of eight different catalog parts – to produce a design that meets all the requirements. This can be done using a simulation called optimization that reruns the AC simulation 100x with different pseudo-random component parameters (individual capacitor quantities), while looking to satisfy a set of user-entered goals.

**TABLE 1.** Maximum Difference Found Between Methods

| % diff | LIN-RPT | LIN-MTT | LOG-RPT | LOG-MTT |
|---|---|---|---|---|
| LIN-RPT | 0 | 64.3 | 34.5 | 68.8 |
| LIN-MTT | 55 | 0 | 61.7 | 8.3 |
| LOG-RPT | 52.8 | 62.6 | 0 | 67 |
| LOG-MTT | 56.5 | 9 | 65.7 | 0 |

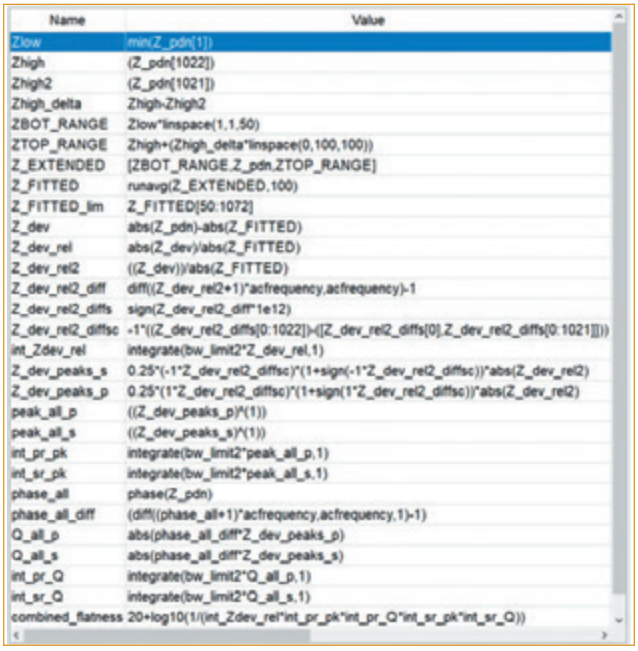


**FIGURE 9.** Flatness metrics computation.

Both the AC-sim and the OPT simulation controllers are placed in the QUCS (or ADS) model schematic. QUCS uses an optimizer simulator that is a separate open source project called ASCO. It had to be fixed to work with this PDN template. While the individual capacitor quantities are controlled by the optimizer, the VRM model had to be manually swapped out and rerun. Optimizer goals were the pass/fail variables for Ztarget and MTT to be > 0; total MLCC cap quantity equal to the number of power pins on the ASIC; bulk cap quantity less than a user-defined maximum; and a flatness metric limit to help with other goals indirectly.

We can measure the flatness using several arbitrary metrics computed from the impedance profile, then combine them into a single number **(FIGURE 9)**. (Another paper called them "scores.") We can compute a fitted impedance curve as a moving average to cut between the peaks, then compute the deviation from it in relative terms. Then we can compute several further variables from that and from the impedance phase curve. Phase differential is intuitively related to the quality factor. The area under the relative impedance deviation is computed with definite integral calculus. The peak heights and peak sharpness

for parallel (positive) and series (negative) resonances can also be obtained as Dirac-like pulses and summed up automatically with cumulative sum. The template computes all these with a series of intermediate waveforms using differential, integral, signum and other functions. (The only reference I found to flatness requirement is the Q < 0.5 from literature, or the calculation above for Q < 2.5.) Instead of using Q or flatness for pass/fail check, we can more easily use a combined flatness metric as an additional optimizer goal that may or may not help the optimization process with the main RW amplitude pass/fail goal indirectly. Multiply the different scores, apply 1/x, logarithm and multiply by 20 to create a single flatness metric ranging between 1 and 20.[3,5]

In one example, the MTT noise voltage amplitude was reduced from 64.9mV to 18.6mV, while improving the flatness score from 9.5 to 12.1, as the optimizer changed the capacitor BOM quantities from [10, 10, 100, 10, 10, 10, 4, 10] to [383, 75, 1, 9, 30, 3, 0, 15]. We can see in **FIGURE 10** how the impedance profile became somewhat smoother, simpler and a bigger "V." Practically, we can run the optimizer with MTT (30 min.). Then, if we are curious, we can run the AC-sim on the optimizer result BOM with RPT, but without the optimizer activated. The RPT with optimizer takes a day to run.

## Conclusions

All these methods create excitation waveforms with load current toggling between min./max. levels at different specific timing that create an excitation spectrum with a few automatically chosen peaks. All of these methods have blind spots. If the PDN is flatter and has no parallel resonances, then the MTT underestimates the worst-case noise compared to RPT that finds attack points on a flat impedance profile. On the other hand, if two parallel peaks are near each other, then sometimes the RPT misses one of them.

Probably the best strategy for a designer is to calculate the RW noise level with two to three different methods, all with logarithmic sampling for fast computation. Then take the worst-case result to be compared against the chip specs for final pass/fail condition.

Benchmark. On a low-power laptop, it takes a few seconds to run an AC simulation, a few more to run the MTT, 10 minutes to run the RPT and 100x the single simulation to run the optimizer. The optimizer with MTT can complete in one hour, with RPT 48 hours. The slowness of the RPT is caused by the QUCS tool's deficiencies reversing vectors that are part of the RPT algorithm. Two vector reversals are required: one for the excitation waveform time reversal and one for creating a symmetrical spectrum before applying the IFFT. If they fix the known matrix multiplication bug, then we can multiply the vector with a rotated identity matrix, instead of bit by bit reordering, to speed up the vector reversal significantly. This allows us to include the RPT in the optimization goals.

A QUCS template was created for pre-layout design creation and experimentation by performing an automated check on target impedance and rogue wave amplitude. It can be used to help select the right decoupling capacitor values or quantities, voltage regulator part, loop compensation values (measure a retuned VRM evaluation board with a VNA and use the new S-parameter model) to meet the datasheet requirements from the ASIC chip vendor. The template is provided free to observe the details of the equations or to use it in product design. With QUCS and ADS, we can implement and automate the latest published scientific analysis techniques in our simulations. We don't need to wait for tool vendors to implement them as hard features. For example, the inclusion of measured VRM S-parameter models or the computation of rogue wave estimation are not yet available in any commercial software as built-in functions. The MTT and LOG-RPT methods were demonstrated in pre-layout simulation. Since none of the commercial tools support them, neither do they support measured VRM models, and QUCS does not support post-layout extraction. A post-layout RW analysis considering spatial information could be conducted by extracting the PDN impedance profile from an SI/PI tool into an S-parameter file, inserting it into the QUCS template, disabling all planes and capacitors, running the simulation as usual. □

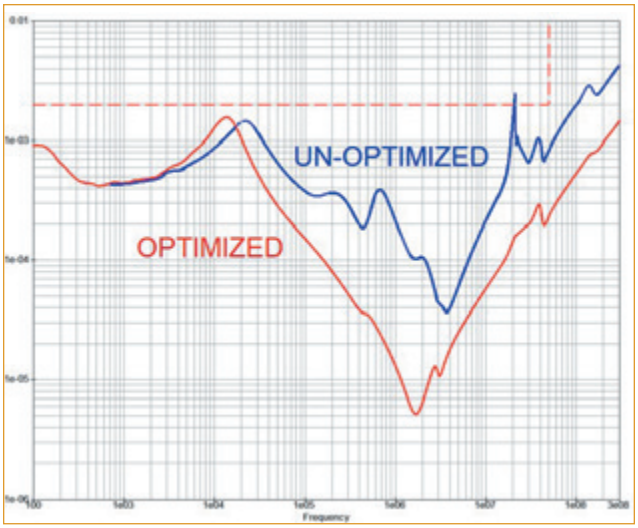


**FIGURE 10.** Optimized impedance profile.

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3. Steven M. Sandler, *Power Integrity Using ADS,* 2020.
4. Steven M. Sandler, Eric Bogatin and Larry Smith, "Power Distribution Network (PDN) Impedance and Target Impedance," EDICON 2018.
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## TOOL LINKS

PDN template: https://buenos.extra.hu/download/PowerIntegrityDesign2_prj.zip
QUCS tool: http://qucs.sourceforge.net/
ASCO optimizer: http://asco.sourceforge.net/index.html

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# Does a HEATED CONDUCTOR Have Signal Integrity Implications?

Signal traces internal to the board change temperature along their length, changing resistance. by DOUGLAS BROOKS, PH.D., JOHANNES ADAM, PH.D., and ULISSES CASTRO

In our recent book,[1] an image shows how heat from a relatively hot trace flows downward through the board (FIGURE 1). What is important to recognize here is how little horizontal heat dispersion there is. The heat seems to flow straight down. What thermal images like this obscure is the relative horizontal and vertical scales. The horizontal width in this image is 50mm, while the vertical height is less than 2mm. Not enough room is underneath the trace for much horizontal dispersion. Consequently, the temperature of the bottom layer of the board directly under the trace is only a few degrees cooler than the temperature of the top layer, regardless of what is beneath the top layer.

We discuss this and its implications in some detail in another recent article[2], but in this one, we want to suggest a different issue: whether this heat flow poses a potential signal integrity implication.

We will start with a simple model of a heated pad such as might be found under a BGA or microprocessor. We use a simulation tool called thermal risk management[3] to do the analysis. We model a board that is 100mm (4")[4] square with a 20mm (0.75"), 1oz. pad in the center of it. The board material is standard FR-4, 1.6mm (63 mils) thick. We apply enough power to raise its temperature to 62.9°C, 42.9° above the ambient. Under these conditions, the temperature directly underneath the pad on the bottom surface of the board is 61.2°C, 1.7° lower than the pad.

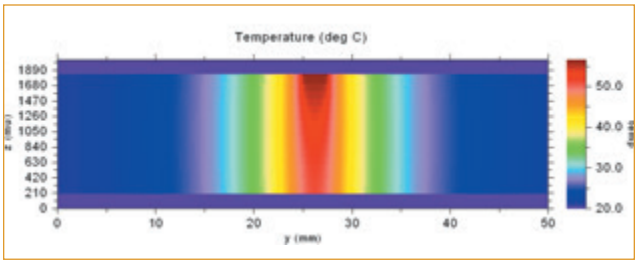


FIGURE 1. Heat from a hot trace tends to flow straight down through a PCB.

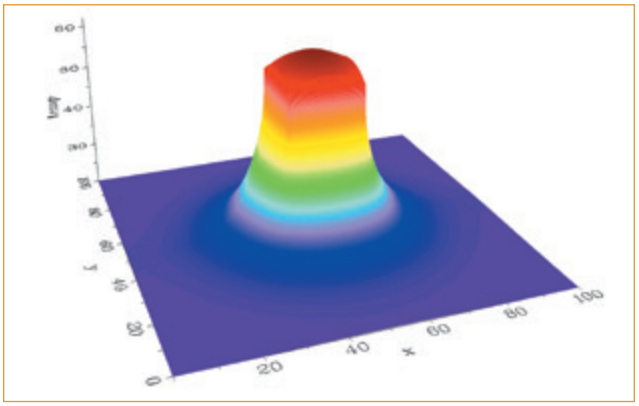


FIGURE 2. Thermal gradients around the simulation.

If we now place a 1oz. copper plane on the bottom of the board, the temperature of the pad will lower. Under these conditions, the temperature of the top pad is 40.1°C, and the temperature directly under the pad on the bottom layer plane is 35.6°C, a difference of 4.5°C.

FIGURE 2 illustrates the thermal gradients around the top layer of this model. The pad is not a uniform temperature. The center of the pad is the hottest at 40.1°. It cools least effectively. Heat conducts primarily down from the center. The corners of the pad cool most efficiently. The heat from there conducts down and out in a 90° arc. The sides of the pad are in between. They tend to cool down and straight out from the pad. As a result, the temperature drops off sharply to the sides of the pad, but the area directly under the pad stays fairly hot.

If a trace is routed underneath the heated pad, assuming no self-heating, the temperature of the trace will have almost the same thermal profile as the pad. This is true whether the trace is below, above or originates underneath the heated pad, as in a BGA. We simulate this by routing a 90mm long (3.5") trace, 0.4mm (16 mil) wide, 1oz (0.033mm) thick on the middle layer of the board directly under the centerline of the pad at the point on the board where Y = 50mm.

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**FIGURE 3** illustrates the thermal profiles of our models along the X-axis (where Y = 50) of the top layer, middle layer and bottom layer of the board, with and without a plane on the bottom layer.

Elsewhere[2], we postulated the bottom layer underneath a heated pad or trace would be less than 10° cooler than the heated pad or trace, regardless of what was underneath the pad or trace, in most practical situations. That is true in this simulation. There is only 1.8°C maximum difference between the top and bottom surfaces without a bottom layer plane and 4.5°C with a bottom layer plane. The maximum temperature of the trace is almost the same temperature as the bottom surface of the board in either case (shown here without a plane).

If there is a plane under a heated pad, the plane is within a few degrees of the pad. This has implications for thermal vias. A thermal via typically extends from a heated pad to an underlying copper surface, usually a plane. The formula for thermal conduction is:

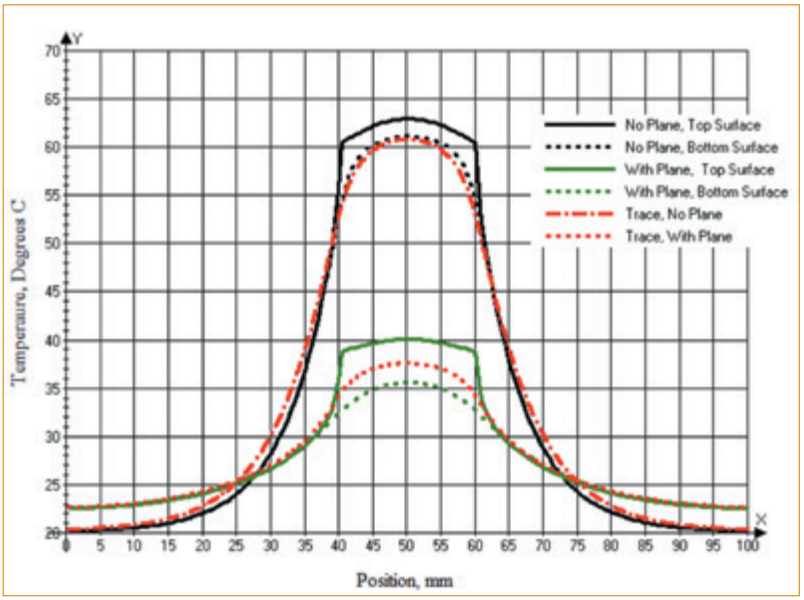


**FIGURE 3.** Thermal profile of the top layer, bottom layer and trace layer of the simulation, with and without a bottom layer plane.

$$Q/t = kA(\Delta T)/d$$

Where:

- Q/t = Rate of heat transfer (watts, or joule/sec.)
- K = Thermal conductivity coefficient (W/m·K)
- ΔT = Change in temperature (°C = °K)
- A = Overlapping area
- d = Distance between pad and plane

**EQ. 1.**

"IF THERE IS A **PLANE UNDER A HEATED PAD,** THE PLANE IS WITHIN **A FEW DEGREES** OF THE PAD. **THIS HAS IMPLICATIONS** FOR THERMAL VIAS."

If the underlying surface is nearly the same temperature as the pad – for instance, ΔT is very small – then the thermal conductivity through the via is extremely low. This is why thermal vias are so inefficient cooling pads.[5]

If the trace changes temperature along its length, then it also must change resistance along its length because of the temperature coefficient of resistivity. TRM allows us to measure the resistivity at every point along the trace.[6] If we know the resistivity and the trace dimensions, then we can calculate the point resistance at every point along the trace.[7] **FIGURE 4** graphs the point resistance along the trace simulated without a plane underneath it. The trace resistance under ambient conditions is 0.1149Ω. Under peak temperature conditions, the trace point resistance is 0.1332, a 15.9% increase. If we average the area under the curve, we calculate the average trace resistance is 0.1235Ω, using an ohmmeter.

We don't need a thermal simulator to achieve a rough estimate of this effect. We can estimate the resistance of the trace under ambient conditions (20°C) by Equation 2.

$$R = \rho * L/(W * Th) = 0.017 * 90/(0.4 * 0.033) = 0.1159\Omega$$

Where:

- ρ = Resistivity = 0.017 Ω-mm²/m
- L = Length of the trace = 90mm
- W = Width of the trace = 0.4mm
- Th = Trace thickness = 0.033mm

**EQ. 2.**

We can estimate the change in resistance by noting the temperature coefficient of resistivity is about 0.0038, and the change in temperature is about 42.9°C. Therefore, the point resistance at the

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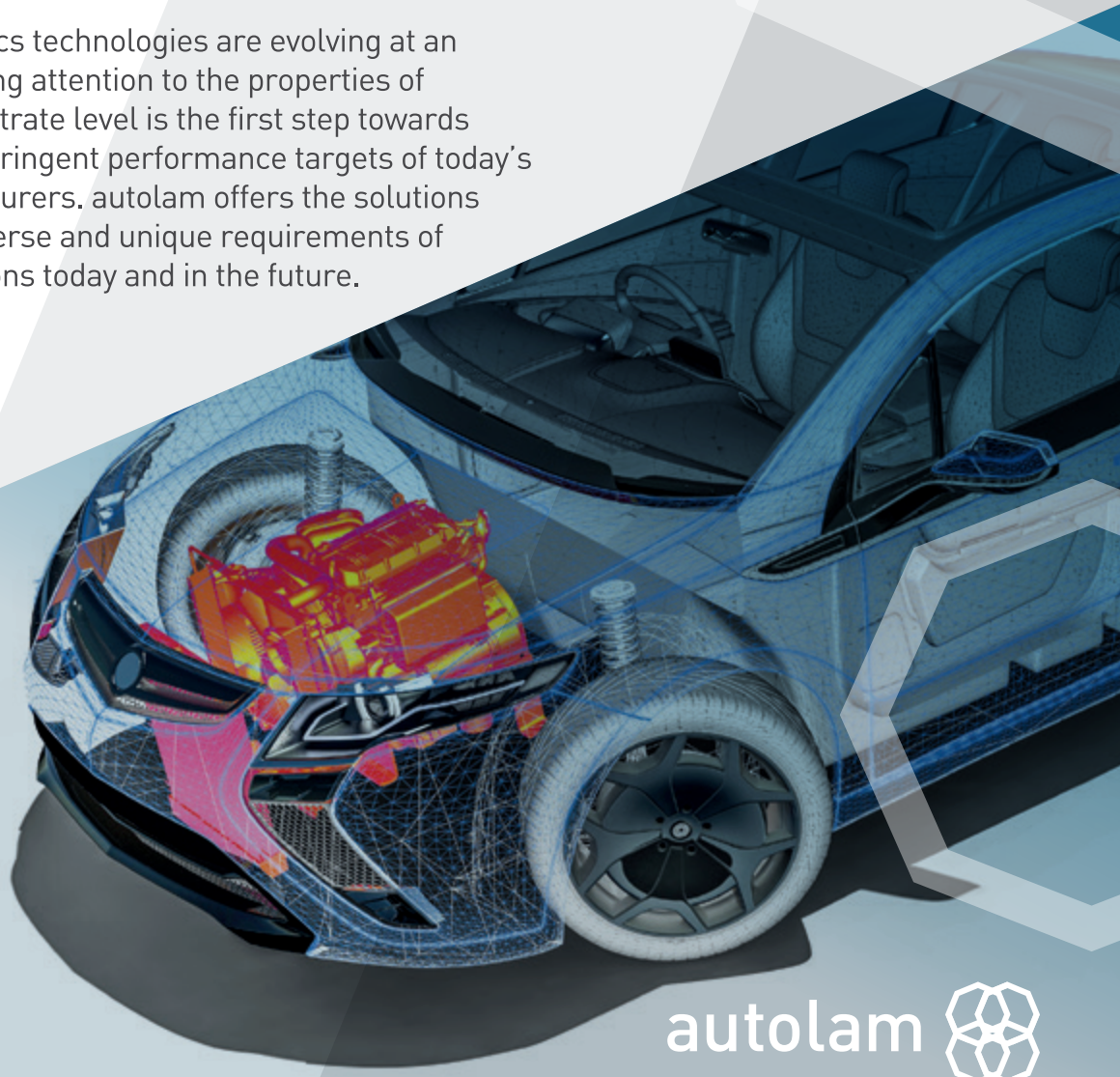

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maximum point is estimated by:

$$R = 0.1159*(1 + 0.0038*42.9) = 0.1347\Omega$$

EQ. 3.

We can now estimate the average resistance of the entire trace by recognizing this new, elevated resistance occurs over 20mm of the total 90mm length, or 20/90 = 22.22% of the length. So:

$$\text{Trace } R = 0.2222*0.1347 + 0.7777*0.1159 = 0.1200\Omega$$

EQ. 4.

This approach overestimates the average resistance because it overestimates the temperature of the pad, ignoring the thermal gradients on the pad. It underestimates the total resistance because it underestimates the horizontal heat spreading at the edges of the pad. These two factors do not exactly cancel, but they do offset each other. The result is a rough estimate of what will happen when a trace crosses under – or over – a heated pad.

Now the question is: Could this change in resistance have signal integrity implications?

A. Suppose the trace is one side of a differential pair of traces. Would a difference in resistance of one side of the differential pair be enough to change the signal relationship along the trace and lead to a false signal?
B. Suppose we are dealing with rise times so quick or temperature changes great enough the characteristic impedance of the trace is nonlinear. Would the change in impedance be enough to cause a damaging signal reflection?
C. The changing resistance will lead to a changing voltage/current relationship. Could this cause a change in the electromagnetic field around the trace, resulting in an EMI or crosstalk issue?

These questions are beyond the scope of this paper, and we leave them to others to investigate. It is possible thermal changes like these are so small they are trivial, but someone should test that possibility.

We have based these questions on the results of a simulation. A relevant question is if we can replicate these results on a real board. We had a board available on which to test these results. It was small: 14.2 x 127mm x 1.6mm thick. It had a 4.5", 100-mil-wide trace on the top layer (the "victim trace") with a 2.5mm (100 mil) trace crossing underneath it (the "aggressor trace") on the bottom layer (FIGURE 5). We could apply current to the aggressor trace and measure both the temperature profile and the average resistance of the victim trace.

There were difficulties defining all the parameters of the simulation model, however[8]:

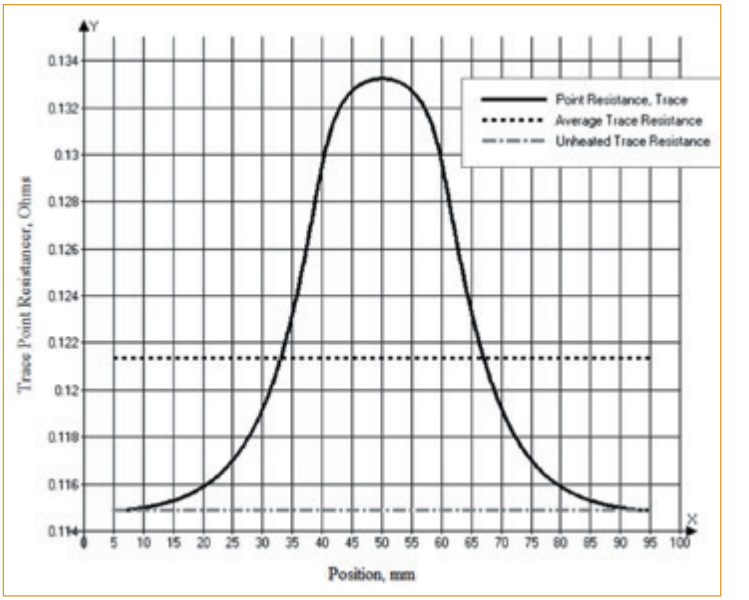


FIGURE 4. Point and average resistance of the modeled trace under a heated pad.

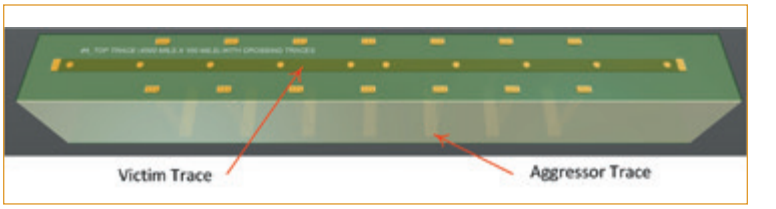


FIGURE 5. Experimental trace available for testing.

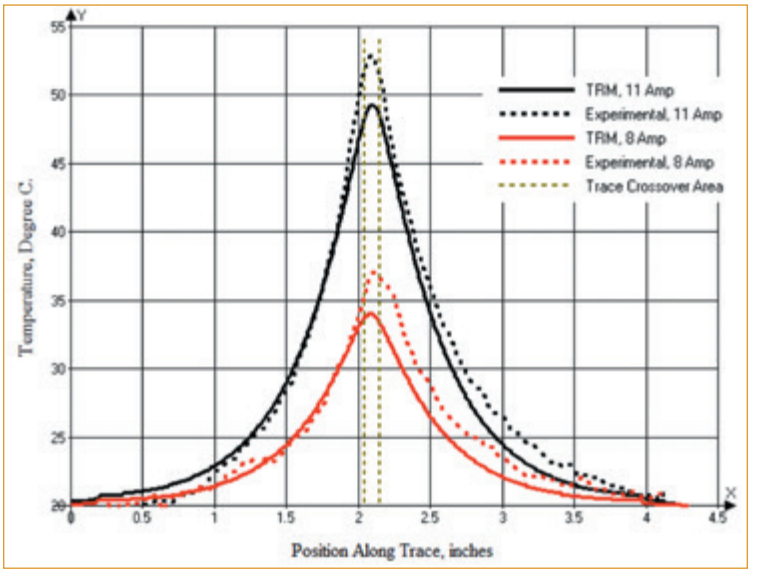


FIGURE 6. Experimental temperature results vs. modeled results for the victim trace.

1. Not all the relevant parameters were known about the board material, most important the thermal conductivity coefficients (in plane and through plane).
2. We were not certain of the resistivity of the copper traces.
3. We were not certain of the thickness of the copper traces, and in this type of investigation, the results are *extremely* sensitive to the trace thickness. A difference of 1µm in thickness makes a big difference in the results.
4. The numbers (trace resistance) we are dealing with here are extremely small, so comparisons are risky.

Nevertheless, we attempted to do so with acceptable results. **FIGURE 6** illustrates the calculated victim trace temperature profile from the TRM model compared to the experimental result measured with a thermal imager. The two sets of observations are for an aggressor current of 8A and 11A. The maximum differences between the experimental results and the model results are less than 3°C (on the order of 5% or so), within the measurement error of this experimental setup. Note how much more sharply the curves peak in this case compared to Figure 3. That is because the heated trace is only 2.5mm wide compared to a 20mm square pad for the case above.

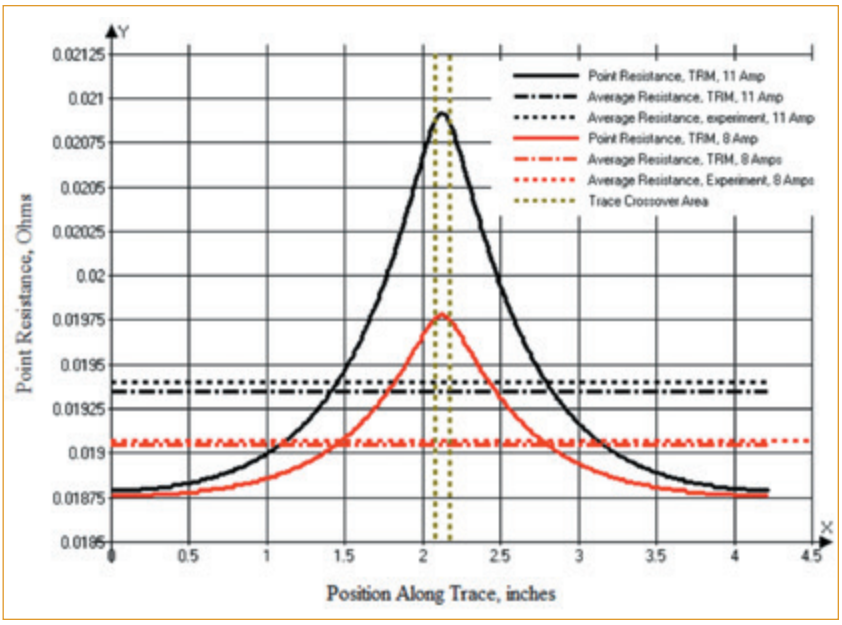


**FIGURE 7.** Modeled vs. experimentally measured resistance along the victim trace.

**FIGURE 7** shows the simulated model resistance vs. the experimentally measured resistance for currents of 8A and 11A. The modeled resistances were determined the same way they were in Figure 4. We could only measure the trace (average) experimental resistance, but not the point resistance along the trace. As can be seen, the results are very close.

The quantitative experimental results are reasonably close to the modeled results, but what is most encouraging is the shapes of the curves are almost exactly as expected.

We can conclude signal traces internal to the board can – and most assuredly do – change temperature along their length. Therefore, they change resistance. The question posed here is whether that change is significant enough to worry. ▫

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2. Douglas Brooks and Johannes Adam, "Thermal management: A Close Look at Vertical Heat Flow in PCBs," www.edn.com/thermal-management-a-close-look-at-vertical-heat-flows-in-pcbs/, EDN, Oct. 19, 2021.
3. TRM was originally conceived and designed to analyze temperatures across a circuit board, taking into consideration the complete trace layout with optional joule heating, as well as various components and their own contributions to heat generation. TRM was written by Johannes Adam, Ph.D.
4. Unit conversions are approximate.
5. Douglas Brooks and Johannes Adam, "A Close Look at Facts and Myths About Thermal Vias," www.edn.com/pcb-design-a-close-look-at-facts-and-myths-about-thermal-vias, EDN, Aug. 31, 2021.
6. The resolution is determined by the thermal pixel setting. (See reference 1, Chapter 6.)
7. Think of the "point resistance" as the resistance of the trace (in Ω) at that point. Resistance is a point concept because temperature, trace thickness, copper resistivity and dielectric thermal conductivity coefficients, among other things, are also point concepts. We define point resistance using the standard formula resistivity times length divided by conductor cross-sectional area – at a point. Total trace resistance is the average of all point resistances along the trace.
8. We try to quantify uncertainties such as this in Chapter 7 of our book (Reference 1) and devote the entire Section 13.3 on the question of whether traces are uniform thickness. (They are not.)


**DOUGLAS BROOKS, PH.D.,** has bachelor's and master's degrees in electrical engineering from Stanford and a Ph.D. from the University of Washington. For the past 27 years, he has owned an engineering service firm and has published two books, including *PCB Design Guide to Via and Trace Currents and Temperatures;* doug@ultracad.com. **JOHANNES ADAM, PH.D., CID,** has a doctorate in physics from University of Heidelberg. In 2009 he founded Adam Research and works as a technical consultant for electronics developing companies and as a software developer. **ULISSES CASTRO** has a bachelor's in electrical engineering from Instituto Tecnológico de Tijuana and a master's in engineering from Universidad Autónoma de Baja California. He has over 21 years of experience in manufacturing and electronic design.

# APEX WAS LIVE Again. We Should Be Thankful for That.

The annual trade show was slow by historical standards but attendees were pleased to be there. by MIKE BUETOW

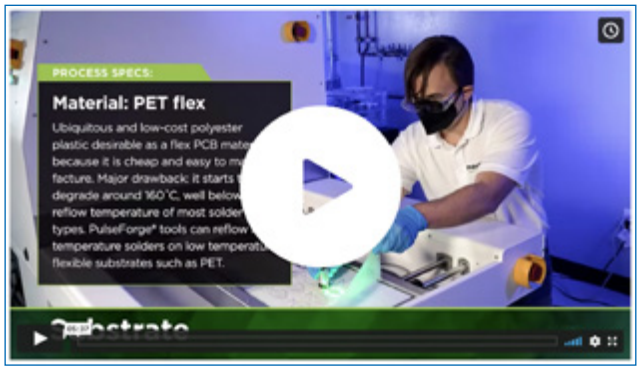
The annual IPC Apex Expo trade show, traditionally the largest assembly show in the US, was more "expo" than "apex" when it resumed as a live event in San Diego in late January. Traffic was certainly lower than typical, and notably quiet at times. See what Covid hath wrought.

Several suppliers decided not to bring equipment. Some others cut back on the number of machines they brought. Many exhibitors reduced their employee headcount as well, leaving those East of the Mississippi at home and counting on their West Coast staff to carry the load.

Apex remains primarily an assembly equipment and materials trade show. The message from several SMT line vendors is Covid has led to diversification to North America from China, as companies can't afford long lead times and face pressure to keep the IP of sensitive products in the West.

Another trend cited is toward turnkey SMT line solutions.

The show's highlights – and there were a few – were less about what's possible now and more about what might be mainstream in a few years.




**VIDEO.** PulseForge Photonic Soldering (Vimeo)

Rogers' new 3-D-printed dielectric material, called Radix, was getting buzz, so much so even some of its competitors were mentioning it. The proprietary composite materials are for RF applications where physical constraints are a factor. The system shown at Apex has a targeted Dk of 2.8 and a Df of 0.0043 at 10GHz when cured.

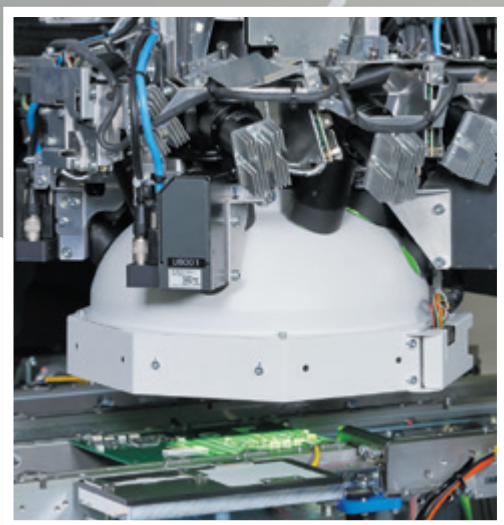
Likewise, PulseForge did not have one of its pulsed-light curing (read: photonic) soldering machines on the floor, but the videos demonstrated how it can solder on almost any surface, such as paper, plastic or fabrics, and is really, really, really fast. Think Star Trek warp speed fast. Because all parts on the board are soldered at once, the traditional solder oven profile is eliminated. A company video showed an inline SMT configuration featuring an ESE printer, Hanwha placement machine, and the PulseForge Digital Thermal Processing unit. The soldering process of a 12-up panel of very thin Arlon PET material with 0201 LEDs and resistors took less than 10 seconds, and working samples were available in the booth.


*Covid's impact on attendance was notable.*

Other advances, in alpha order, included the following. Note that because of the number of booths, visiting every company is impossible and as such some newsworthy technologies are inevitably omitted.

Arlon showed its new low Dk, low-loss, high Tg polyimide materials. The latest edition to the series, 86HP, is for high-speed digital applications where high thermal conductivity is required.

# Eliminate defects with Yamaha's AI enhanced AOI

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ASM demoed its latest TQ printer and the Command Center factory floor control monitor, which can be thought of as a cockpit that shows the status of all individual lines.

Asys touted its Serio 6000 printer, claimed to be the first fully automatic printer. The system offers automation in stages, whereby squeegees and stencils can be set up asynchronously, and tools for the next product cycle can be stored directly on the printer and automatically installed as needed. Even setup can be performed autonomously via a Cobot.

Data I/O has new APIs on its Connex device programming software.

Digitaltest/JOT Automation have teamed on the new Sparrow M5, an ICT tester inside a handler.

Digitaltest's Sparrow M5 is an ICT tester inside a JOT Automation handler.

Although it debuted at the end of 2020, this was the first time we saw ECD's SelectiveRIDER, a selective solder version that fills out its portfolio of soldering profilers. The SuperM.O.L.E Gold 2 sits atop a pallet and captures data on fountain height and diameter, fountain X/Y accuracy, solder temperature, flux penetration and more.

Fuji never disappoints, this time with the new NXTR placement platform, a high-end model that supports larger panel sizes and enhances part handling. A newly developed automatic feeder exchange system is said to eliminate manual changeover and supply. The NXTR also links with Fuji's integrated production system, Nexim.

Inovaxe showed a new feeder rack for the SREX 1B component storage system. It also has a handheld mobile scanner.

ITW has several new models, including a printer and dispenser "coming this year." We did get a demo of the Edison ACT II printer, which was on the floor but is not yet set for release, and a quick rundown of the new tilt axis feature coming on the Prodigy dispenser.

K&S focused primarily on wafer and advanced packaging bonding/assembly equipment. Its newest machine, Luminex, is a laser-based mini and micro LED die transfer system capable of sorting, mixing, re-pitching, die bonding, or mass placement.

KIC is pushing integration of its reflow profiler's connectivity with CFX and Hermes standards. It has created an API package for its semiconductor packaging users. Next up is a vacuum reflow profiler.

MacDermid was one of the few materials firms with advances to discuss. Its Affinity Gold 3.0 is a hybrid plating system that enables fabricators to plate any gold thickness required over nickel-palladium without the corrosion that occurs with

*continued on pg. 58*

## PCEA New Product Introduction Awards Announced

CIRCUITS ASSEMBLY and PCD&F announced the 2022 New Product Introduction Award winners for electronics assembly equipment, materials, software, and PCB fabrication.

The 15th annual NPI Awards recognizes the leading new products during 2021. An independent panel of practicing industry engineers selected the recipients.

**The winners are:**

1-Click SMT.....Soldering – Selective *(MAS-i4)*
Arch Systems..... Software – Process Control *(ArchFX Analytics)*
CyberOptics..... Test and Inspection – SPI *(SQ3000+)*
Europlacer Component Placement – Accessory Technologies *(ii-Tab)*
Europlacer..... Component Placement – High Speed *(ii-A2)*
EVS..... Soldering – Alternative *(EVS 11KLFHS)*
Heller Industries.....Soldering – Reflow (Convection) *(MKV-VF)*
Indium..... Adhesives *(NC-702)*
Juki Automation.....Component Placement – Multi-Function *(JM-50)*
Juki Automation.....Component Storage *(ISM UltraFlex 3600S)*
Koh Young.....Process Control Tools *(Neptune C+)*
Kyzen..... Cleaning Materials *(Aquanox A4626)*
Omron..... Test and Inspection – AOI *(VT-S1080 3D AOI)*
PSA Systems.Automation Tools *(Matrix Automatic SMT Support Tooling)*
Rogers Corp. .....Laminates *(3D Printable Dielectrics)*
Scienscope ..... Labeling Equipment *(Scienscope IMS-200)*
SPEA .....Test and Inspection – ICT *(T300 Board Tester)*
VJ Electronix ..... Test and Inspection – AXI *(Apogee 90)*

To view the awards ceremony, visit:

**https://register.gotowebinar.com/recording/7382123689212464392**

# DESIGN ENGINEERING: Back to School

RIT and industry have developed a novel curriculum for teaching PCB design. Is this the start of a college trend?

**by MIKE BUETOW**

We are always interested in the approaches being taken to recruit and train the next generation of engineers. Readers may recall last summer we did a podcast with a group of recent graduates from the Rochester Institute of Technology's Capstone program. There, the students conceive, design, source and build electronics hardware as part of a senior project. It's truly a great way to immerse themselves in what a career in our industry could look like.

What we didn't mention was RIT is launching another hands-on program. This one focuses on printed circuit board design. The first class started in January with 25 students. Chris Banton, director of marketing at EMA Design Automation, and Dr. James Lee, acting chair of the Electrical and Computer Engineering Technology department at RIT, explained what spurred the program and what it hopes to accomplish.

Mike Buetow: Chris, I know sharing knowledge has been a passion of EMA's forever. Is it presumptuous to ask whether the idea for the class started with you?

CB: I don't think so. It really started from feedback from customers. They're just having a harder and harder time sourcing new engineers who understand PCB design. I know you've done articles and surveys, and there's a gap here. Designers are starting to get older and retire, and there's just the explosion in electronics, so there's even more demand than maybe there was before. We were really looking at how we help our customers get the engineers with the skills they need to be successful. With our proximity to RIT and our CEO [Manny Marcano] being an RIT graduate, we thought it would be a great fit to see if we can work together and find a way to educate newly minted engineers with the skills they need to get the jobs they want.

Chris Banton

MB: So, Manny approached RIT?

JL: That is correct. Manny, being one of our alums, came to us and said there is this big need out there, and there were not many programs at engineering schools across the country. He said, "Would you be interested in starting a program?" We had several conversations back and forth, and it started with this initial offering. We have seen excellent interest from the students, and we [will] be expanding to a multi-course offering, and something that students can get on their transcripts and get certifications so they're able to put that in their portfolio and improve their employment outlook.

Dr. James Lee of RIT is working with EMA Design Automation to implement the new curriculum.

MB: Are there models at RIT for working with industry to develop curricula?

JL: Yes, we are very open to working with the industry to meet their needs from a curricular perspective. This is a perfect example where an industry sees a need and really a lack of focus in engineering programs. Another program we've worked with is signaling through railroad areas. That is a specialty no other engineering programs have been focusing on. A third example would be engineering documentation, which is also something that's very critical but is not really focused on in engineering school.

MB: RIT is well-known for its engineering programs, of course, which include computer engineering, computer engineering technology, electrical engineering, microelectronic engineering, software engineering, and robotics and manufacturing engineering technology, among


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others. I could see a case made for the PCB design class to fall under any of those. So which degree program is the class included in?

JL: It's really set up to cut across multiple disciplines. RIT is uniquely designed in that we have both a College of Engineering and a College of Engineering Technology, both of which produce engineers; it's just a matter of how people learn. If they learn in a more applied, hands-on fashion, that's a very good fit for the College of Engineering Technology, whereas if it's more of a theoretical background, that's a more traditional engineering program. But this course, and when we expand it to multiple course offerings, will be available to engineers from several of the programs you talked about, so the program of computer engineering technology, electrical engineering technology, there's also a mechatronics program that will be able to take this course, and those are from the College of Engineering Technology, but then those equivalent programs that understand circuits as well from the traditional engineering program – computer engineering, electrical engineering – will also be able to participate and come up with what we call an option for printed circuit board design.

Students are designing printed circuit boards and learning from industry experts.

MB: Let's get into the nature of the program. This initially is one class, correct?

JL: Yes, initially we started with one class that is really the basics of using the software, OrCAD, and understanding how to go from an established electrical circuit to a printed circuit board.

MB: Will you start with schematics, or will you jump into routing and placing?

JL: I believe they will start with schematic and work from there to component placement and a little bit of optimization.

CB: The intent is to give that end-to-end process, so the student can see the schematic side but also how that board gets realized in the layout, and there will be some DfM discussion as well because that is another area where not enough students and maybe EEs in the field get to experience what it takes to actually build [the board] at a yield that [will] make your company successful. The goal is to take a student through that whole process. As we discussed in the past, we're seeing more and more EEs tasked with PCB design, and we're trying to help them through it, to give them the skills to be confident and capable to hit the ground running when they start at the company.

MB: And you really do need to understand that whole flow, as a single person has responsibility for multiple things now with regard to the circuit, the design and then getting it into manufacturing. They can't just have one person do the schematic and then throw it over the wall.

CB: I agree. I think it's beyond just the manufacture. It's the complexity of the design, the signal integrity issues, power integrity issues. Everything is so interrelated now that it's really hard to just chuck over the wall and hope for the best because that's usually a recipe for failure.

MB: Who is teaching the class, and what's their background?

JL: We have a person EMA suggested, Kirsch Mackey. He will teach the course. He will teach it remotely, which [will] be a nice innovation. He has a lot of experience with PCB design, as well as teaching PCB design to military and other entities, and we're really thrilled with all his expertise and his experience.

MB: Is he an EMA staffer?

CB: No, he is someone we've been aware of. He's been putting out courses on LinkedIn and Udemy, and he's been a longtime Cadence user through his time in school as a [teaching assistant] and in his professional career. We've been trying to support his efforts and look at this opportunity to formalize some of the work he's doing with people who get out of school and then need to learn this stuff. How do we take it into the school and make it part of the curriculum?

MB: EMA of course has many staffers with expertise in board design. Will any of them be supporting the program, either inside or outside of the virtual classroom?

CB: It's something we have been talking about it. That's probably something that, as Jim alluded to, would be in the next course. This one is kind of the "101," if you will, and there's just so much you could get into.

I think as we expand the offering, especially with the initial response we got, then see how that works in terms of the other EMS folks, but we do have plenty of people [who] have lots of experience, and the great thing is they're always willing to share, which is very important.

MB: How many students registered for the class?

JL: We had to limit the class to 25 due to facilities, and we need to be able to have a computer for every student. We have 25 registered and I believe a waitlist of five.

MB: That's terrific! Do they have any type of project or something they have to realize by the end of the year as part of the curriculum?

JL: The actual learning exercises are up to Kirsch, and he is working with some of my full-time faculty to really understand the breadth of what is expected in a college curriculum in a single course, but they will be working on different projects. At this point, with this first course we will not be actually physically building anything, but that is planned for the broader option when they become available.

MB: What metrics for success has the university put into place to evaluate how the program is going?

JL: Really the metrics of any university are based on student interest. If you can generate enough student interest, then that is an area they are interested in. An enrollment of 25 in an initial course offering is really outstanding. It is seldom that many students are interested in a brand-new course. Students are no different from anybody else. They want to make sure they can look at reviews before they take that course. The nice part about this partnership is EMA Design Automation was very forthcoming with their time to come in to talk to the students, to give them examples of printed circuit board design and functionality, and it really helped generate interest from all students of all areas.

MB: Could a non-student or perhaps one who isn't in engineering take this course?

JL: At this point no. That really is something that is planned into the future. What we would like to happen, coming from a longer-term perspective, is we get this first course up and running with engineering students, people who "speak the speak" electrical circuits and understand the different components as they are working with the software for printed circuit board designs, and then we'll expand it where we have the option we talked about, so four or five courses available not just for printed circuit board design but also some manufacturing aspect to it as well. Once we have that in place, we would be in a position to evaluate the need or interest in what we would call non-degree certification. Once we get to that phase, someone from outside RIT or an engineering discipline could sign up and take the courses.

Noah Carrier, an undergraduate student in RIT's College of Engineering Technology, and his classmates are learning skills in printed circuit design as part of a new course developed with industry experts.

MB: You mentioned certifications. Is that the type of certification you're thinking about, or are you talking about other industry certifications that might be offered through RIT?

CB: At least for this initial course, one of the things EMA is offering, since the students will be going through using the software to realize this design, is the chance to get certified in Cadence software. It's a badge they can have on their résumé and their LinkedIn page, and gives an employer that assurance that not only do they understand the process, but they can run the tools that are used by most of the companies in the industry. The thing could be great going forward, to give a broader certification that works with some other certification bodies like PCEA, but that's the start with this 101 course. You know you've mastered the basics and have a proficiency in the tools.

MB: Jim, I know some universities have really kind of dug deep into distance learning platforms. Is that something RIT has explored, or is this a fairly new type of a program?

JL: As with every university, we had some work going on in distance learning platforms prior to Covid. Then Covid came in and really forced all courses to go online. We learned a lot about what works and what doesn't, and we're applying those learnings to courses like this to expand our offerings, to have some resources from a teaching perspective that we may otherwise not have had, as well as resources from a student perspective. As students are becoming more comfortable being out in society, we're able to make those offerings. We have learned a lot over these past couple of years, and all those learnings are going to be used in this course to really benefit that distance learning option.

MB: Chris, will the students be set up with a student version of the OrCAD tool?

CB: Part of our commitment to this is the donation of software and access to certification and those kinds of things.

MB: Are they installed on a client basis on their own laptops, or are they coming into a lab at RIT to use the software?

CB: From the EMA side, we give them the option for both because there is an in-person option and also a remote option, so the student can go into a lab to use the software but also has access to it on

their personal machine for the balance of the year. Even if they take that and start running with it, they'll have access to the software to do that.

JL: Exactly right. One of the things we've learned in giving remote classes is different students need different amounts of in-person help, especially when it comes to computer programs and computers in general. We wanted to make sure we had a spot for every student to come into a physical space and be able to get help getting software up and running and get the computer up and running, making sure they could connect with Kirsch and be of part of the class. We have this 25-seat lab available [where] we have teaching assistants, so if especially the first couple of weeks they just can't get on their screen what Kirsch is doing on the projection, there's somebody there to help them. If that's more than what they need, they also have the option to log in remotely from their apartment or wherever they are to participate in the class.

MB: I can't believe it's taken this long for anyone to develop a program like this, but I'm excited to hear more about it as it goes along.

JL: We're really grateful for the partnership with EMA. It has worked out really, really well, and I want to thank them for continuing to prod me to get this program going.

CB: We're happy to work with you. It's been a great experience, and we are beneficiaries of RIT graduates here at EMA as well, so there is some self-serving nature to this on our end. ▫

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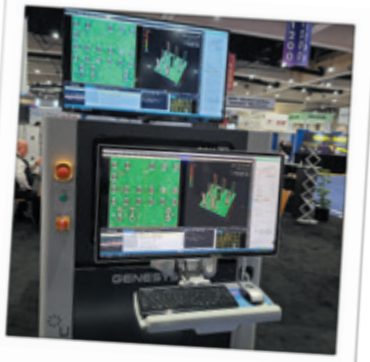
*Apex, continued from pg. 53*



*Mirtec's Genesys-Pin AOI detects missing connector pins, pin offset and forked pins.*

normal immersion gold. The process is suited to fabricators looking to run ENIG and ENEPIG in a single-line configuration. On the Alpha side, HRL3 is a new low-temperature solder sphere alloy designed for BGA, CSP and wafer-bumping applications. The lead-free alloy (Alpha is not publicizing the composition) has a melting point of 145°C and is said to be best-in-class for thermal cycle reliability and drop shock.

Mirtec is capitalizing on the automotive demand with its Genesys-Pin AOI, which inspects up to 50mm-tall connectors and detects missing and forked connector pins.

Mycronic has a new high-speed valve on its MYD10 dispenser. The jet printer has new software with AI auto-polarity recognition.

Nano Dimension is opening a new lab and demo office in Waltham, MA. The company, which acquired SMT equipment maker Essemtec last year, is aggressively expanding and hiring as it brings its additive manufacturing message to the masses.

Parmi's 3-D AOI software now has auto-teach function.

*Apex remains primarily an assembly show, although several suppliers decided not to bring equipment.*

IGEPIG (immersion gold/electroless palladium/immersion gold) is the next generation of final finish material. It has no palladium activators and nickel (so no black pad) and is said to be higher reliability than ENIG or ENEPIG, with lower signal loss than the former and superior fine pattern ability. While only available in Japan at present, Uyemura is so high on its possibilities, it thinks in five years this finish will "dominate."

Viscom demonstrated its iX7059 3-D automated x-ray (AXI) for high-density and double-sided PCB assemblies. Curiously, the IPC New Products showcase touted the iX7059 XL, a large board version of the machine, but the model on the floor was the iX7059.

Zestron is expanding its lab in Taiwan. It sees a "tremendous" amount of activity in Mexico, so much so, it expects another double-digit growth year in North America. ▫

**MIKE BUETOW** is president of Printed Circuit Engineering Association (pcea.net); mike@pcea.net.

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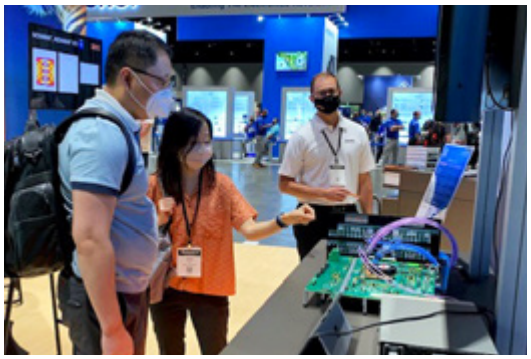

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# Planning to Sell Your EMS BUSINESS?

Here are prospective buyers' questions. Do you have the answers? **by BOB ROSSOW**

If you're an owner planning to sell your EMS business, here are questions to expect from would-be buyers. Forewarned is forearmed, as they say. For those who haven't been through the process yet, this is a basic primer before striking a deal.

### "Can I relocate your business to my own location?"

Prospective buyers want to increase their sales and bottom lines, so many, if not most, buyers are looking for new customers, not real estate or used equipment. If they can move your customer base into their own shop, they can make much of your labor force redundant and maximize their profit. So, depending on the buyer's intent, this can be *the* question that makes or breaks the deal.

### "What is your labor rate?"

This is extremely important if a prospective buyer wants to relocate the business. If your labor rate is lower, then your contract rate is probably lower too. As a result, if they move the business to their location and must pay a higher rate, either they have to raise prices and risk losing customers or take a hit on the bottom line. This can be a deal-killer.

### "How long after the sale is the owner willing to stay?"

Other than price, this question is asked most often. The typical agreed-upon timeframe is six months or a year, but this question naturally leads into the next one.

### "Do you have a general manager who can take over when you leave?"

If the buyer intends to continue the business at the same location, they will be concerned about what happens to the company when you walk out the door with their money in your pocket. Will the customers leave with you? Will the employees stay? Do you personally have technical expertise that will be hard to replace? Is there a competent GM who can run the business? May I meet them?

The importance of these questions cannot be overstated. If you can't answer them satisfactorily right now, perhaps this is not the best time to sell. You may wish to change things to better accommodate prospective buyers and wait until you have better answers before putting the company up for sale.

### "Is this a stock sale or an asset sale?"

Your accountant and lawyer can give the best advice here. A stock sale, of course, means the entire company is sold as-is at the time of sale. An asset sale means only certain listed assets of the company are included in the sale. Buyers like asset sales, as it limits their liability to any and all claims the company may have (or may get from past actions) against it. These issues might include lawsuits by customers, suppliers, employees, etc.

In these sales, tax advantages or disadvantages for both the seller and buyer may come into play. Again, the recommendation here is to get professional help on this decision.

In my opinion, however, the single biggest advantage of an asset sale over a stock sale for the seller is speed. Issues about the company prior to the sale are virtually eliminated, so due diligence is reduced. If a seller must move quickly, an asset sale is a real time-saver. Stock sales can drag out for months, and the amount of paperwork needed can be a time-burner for the seller when they have a business to run as a day job.

### "How many customers do you have? What are their sizes? What percentage of your business do your top-three customers provide?"

Customer-base questions such as size and percentage of overall business of the top-three customers are key. Some prospective buyers will pass on the pursuit of companies with a single customer that makes up 30% or more share of gross sales. Generally, buyers want to see a diverse customer base with the largest customers in the 10% range. They worry about the risk of losing customers, of course, so the most attractive scenario is a potential acquisition with relatively

smaller and numerous customers. They will also ask how long you've had these customers and what kind of profit they generate.

### "What markets are you in?"

You will likely be asked what markets you are in, what dollar amounts you generate in each, how many customers you have in each, what percentage of overall business each market represents, etc. This information may be used to find out how well your business will fit into the buyer's particular mix.

**FIGURE 1.** Prospective buyers like to see things that differentiate a company from others in the field.

### "How skilled is your labor force?"

If you're manufacturing highly complex components that need engineering and design, this will be a key question. Are your engineers long-term employees who are unlikely to quit if the company is sold? Are they being paid at scale for your area? Are they happy? The prospective buyer will see them as valuable assets, and the loss of even one good engineer can be costly. By the same token, if your business is mostly build-to-print, this may be less of an issue.

### "How many new customers do you get each year? How many do you lose?"

The prospective buyer is trying to understand how stable the underlying client base is. Are you losing customers regularly? Why? Are you expanding with a net gain of new customers each year? This also gets into the question of sales and the effort you put into this part of your business. Although it seems counterintuitive, buyers sometimes find it positive if sales endeavors are minimal. They see a way to expand the business, especially if there is extra capacity in the plant.

### "Is there anything unique or unusual about your company? Do you have a particular specialty?"

Are you known for a niche? Is this something a new owner can exploit? Prospective buyers like to see things that differentiate a company from others in the field. This could be specialty machinery, engineering expertise, a great reputation in a specific market – anything that gives your business a leg up over the competition. Think about it. Why do customers choose you over the next manufacturer down the road?

### "What negatives about the company will be discovered in due diligence? Are there any lawsuits in progress, etc.?"

This question does not come up often, but it is something you should consider before putting your company on the block. It is always better to be the one to tell a prospective buyer about a problem than to have them find out on their own. Can you do something about the problem now to lessen its effect on a sale?

### "Do you have extra manufacturing capacity if sales increase?"

You may be asked what percentage of the time your major equipment is in use. This can be a selling point if it is low for two reasons: More business can be accommodated without additional capital expenditure, and fewer hours on a machine can mean a longer time before replacement.

### Here are the major documents you may be required to furnish:

This will vary with prospective buyers, but the list below is typical, though hardly complete. Variations of these documents, as well as other less common records, may also be requested. Prospective buyers may ask for just about anything, and once in a while, we have to say we don't have exactly what they want.

- Income statement (profit and loss statement) for at least the past three years, sometimes four or five. A year-to-date income statement may also be requested the further into the year it is.
- Balance sheet for the past three, four or five years. A year-to-date balance sheet might also be requested.
- Cash flow statement. Same periods and criteria as above.
- Customer list (with no names) may show dollar amounts of customers listed in order of size. This document often shows the industry of each customer and percentage of the overall business.
- The equipment list should be current.
- Backlog of orders currently in-house. Again, no names.
- Brief history of the company with major milestones.
- Organization chart (titles only).
- Inventory (not an itemized list). Usually, a dollar amount is sufficient early on. If inventory is part of the final deal, a joint accounting (your people and theirs) might be conducted shortly before closing.

Sometimes a question prospective buyers ask might seem irrelevant or may be a bit off-the-wall, but the seller should take it seriously. The buyer is trying to understand your business, and the more questions they ask, the more they will understand. Welcome the questions. Don't get frustrated. The questions indicate interest level and need to be answered before an offer can be made. ▫

**BOB ROSSOW** is founder of E/Search International (esearch21.com), an EMS business broker firm with an active buyers list of about 80 potential buyers interested in EMS companies; esearch21@gmail.com.

# Automated vs. Wave Soldering: What's More Efficient for Through-Hole Technology?

Using Lean Six Sigma to balance the increasing cost of solder.

WHILE THE DEATH of through-hole technology has been predicted for decades, the reality is some applications have components that require a level of solder joint robustness that only through-hole technology can deliver. In low- and medium-volume operations, the cost-effectiveness of soldering those mixed-technology printed circuit board assemblies using a selective solder machine is an easy calculation because it may eliminate the cost of operating a wave solder machine. However, operations doing high-volume assembly of predominantly through-hole PCBAs may find determining the cost-effectiveness of selective solder is more challenging since their wave solder machines operate continuously. In those cases, the question becomes: What is the point at which use of wave soldering becomes inefficient when the percentage of through-hole components on printed circuit board assemblies drops?

The cost of solder, along with other material and production costs, is increasing globally. While these cost increases are unavoidable, implementing efficiency improvements can help balance these costs by reducing the amount of solder needed and eliminating solder dross.

SigmaTron's Suzhou, China, team recently used Lean Six Sigma core tools to analyze whether an automated soldering machine would be a better choice than a wave solder machine on assemblies with only a few through-hole components.

The team used a define, measure, analyze, improve, control (DMAIC) process for the project. In the define phase, it selected metrics from September and set a goal to determine if automated soldering equipment could reduce solder bar use and solder dross generation by 40% to 45%. Two assemblies were selected for process comparison.

In the measure phase, the team determined that while less solder was used on the sample PCBAs due to the small number of through-hole components, solder dross generation remained the same since it was a byproduct of machine operation regardless of through-hole component count.

Wave solder dross studies from SigmaTron's Lean Six Sigma team in Tijuana, Mexico, provided baseline data on typical dross metrics to better validate team assumptions related to dross generation. The ability of teams in different facilities to compare past projects helps shorten learning curves in similar projects.

In the analyze phase, the team used fishbone diagrams to evaluate man, machine, environment, method and material in a brainstorming activity. The conclusion was the number of through-hole components did not justify the cost elements of wave solder.

In the improve phase, the team developed component-count-based criteria to determine which process was more cost-effective when tooling, energy use, solder use and solder-dross generation were considered. It also found bill of materials solder usage assumptions were incorrect when actual solder use was measured.

In the control phase, the team defined the new process and determined its use reduced cost more than 72%. Cost-reduction assumptions did not include the savings likely to be found in indirect labor associated with wave soldering machine maintenance, wave fixture cleaning and solder dross removal.

Final conclusions found PCBAs with fewer than 20 through-hole pins were good candidates for automated soldering. The machine itself had a cost of less than $10,000 and generated almost zero solder dross, resulting in no solder loss. Plus, the automated soldering machine is much easier to clean and maintain; there is no solder dross to be recycled or handled and no excess flux residue left on the PCBA. The automated soldering machine option typically delivers a more consistent result than wave soldering when the solder joint is close to the edge of the wave solder fixture. There are temperature-sensitive components with a narrow process window, or specific solder volume is required in a through-hole.

That said, the team found ensuring consistent results across a range of assembly types required fixturing modifications. They performed a design of experiments to test their assumptions. The basic fixture design is concave with multiple levels of rectangular, square or half-circle shapes to accommodate typical PCBA sizes and shapes. PCBAs that easily fit within these cutouts need no further fixturing. A clamshell fixture attached by dowel pins to the soldering machine platform is used to stabilize PCBAs whose shape or size does not fit within the concave portions of the standard fixture. All fixturing is designed for fast load and unload. The machines process two PCBAs or arrays simultaneously, depending on product configuration.

Using analytical continuous improvement processes such as Lean Six Sigma addresses the challenges of rising costs by evaluating evolving product designs against more cost-effective processing options. ▫

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# A Qualified Success

Industry colleagues reunite after two years for in-person lunches with a side of unrestrained conversation.

I MEET A certain friend periodically for lunch. I value his company and conversation. Time with him is never dull. He runs an EMS firm, also never dull. His work provides daily material for stories. He tells those stories well. Sometimes I'm privileged to hear them at our lunches. Talk flows with an easy and relaxed familiarity, a kind of relief. Sometimes the food gets cold. No matter.

Our discussions are more urgent now because the pandemic preempted our lunches for two years. We have a lot of pent-up opinions to catalogue and classify. Add to that winter's natural chill, which enforces a certain introspection. Two years is a long time to accumulate vent-worthy prejudices. Like a trusted confidante, our resumed midday dialogue is most welcome – and good therapy.

These exchanges with my friend take place in a bullshit-free zone. No topic is sacred. No opinion is off-limits. Salesmanship and posturing are implicitly discouraged. Aside from the standard business-related talk, we risk diverting into politics, history, science, philosophy, religion, child-raising, youthful folly, renewed inflation, government, taxes, hiring difficulties – whatever suits us at that moment.

He has many opinions, as you would expect of an EMS CEO. Sometimes I don't agree with them, but that's okay because sometimes he doesn't agree with me. Those sincere, but always respectful, differences are what make our luncheons so refreshing, interesting and educational. And now, long anticipated. There are no hidden agendas. It's amazing what one can learn when keeping an open mind and not trying to pitch something. Perhaps an unheralded benefit of the pandemic is the stripping away of many pretensions. Life's too short, as has been made crystal clear these past 24 months.

So many things have changed. We compare notes in our customary judgmental way. Items that may have seemed important only two short years ago no longer seem to matter. So many things have also stayed the same. People can still be obtuse, stupid, unthinking and intolerant. Colleagues can still be greedy, controlling, inconsiderate and intimidating. All this can be accomplished while social distancing and being fully vaccinated and boosted. Some use the pandemic as cover for bad behavior, masking moves they intended to make anyway. Covid simply furnished a readymade pretext.

Our discussions make use of a newly expanded vocabulary. Think of the neologisms we've learned: supply chain; spike protein; herd immunity; viral load; mRNA vaccines. We're all amateur epidemiologists now with an expanded lexicon of excuses when things don't go to plan: Los Angeles Harbor; Donbas/Ukraine; Xinjiang; reshoring.

We've aged at an accelerated rate. Commitments are now hedged. Everything is qualified and tentative. My friend and I note the prevalence of more nuanced language – after normal was redefined.

"If all goes well…"
"If everything arrives on time…"
"If everybody stays healthy…"
"If nobody gets sick…"
"If the flight isn't cancelled…"
"If the shipment isn't held up…"
"If the test is negative…"
If.
Many might add, "God willing."

Most understand the qualifiers. Understanding is often a function of age, although it is risky to generalize. We all know wise millennials and aged fools. The minute you generalize is the instant you are proved wrong, and you have the lesson of oversimplification and snap judgment thrown back in your face. The story of my life. (It keeps me humble.) But the fact remains, in my experience – and that of my lunch companion – most opt to muddle through rather than make a scene of futile protest. Mercifully, neither of us has experienced debates about masking adjudicated with fistfights yet.

What exactly have we learned? Are we smarter and wiser, or warier from the experience? My friend and I wrestle with that one. Lunch does indeed grow cold. The conversation gets hot.

Our discussion turns to communication skills among colleagues and coworkers. One unsung skill that pays dividends is the ability to ascertain and describe a situation, so it is comprehensible to a third party. That seems obvious enough. The surprising truth is many can't do it, or do it badly, resulting in much time expended, reexplaining the original problem to the intended recipient. We lament the hours lost rectifying misunderstandings that never should have happened, due to a basic lack of clarity in stating the issue.

Breaking down problems into easily digestible bites (or bytes) is a gift, a real advantage for those who have it. Communicating those bites (or bytes) to interested laypersons *so they understand and can act on them* is a sublime gift. An articulate engineer who can distill a technical challenge to its simplest terms for nontechnical laypersons, such as buyers or managers,

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who can effortlessly switch between those laypersons and technical peers, is golden. And almost impossible to find.

Equally scarce are those whose radiological skills can clearly describe the content of an x-ray image to an engineer. The recipient doesn't always know – or admit to knowing – what it is they are looking at.

The same goes elsewhere in companies for HR or accounting problems. Misinformation about 401(k) policies or charts of accounts can drive comprehension off the rails, leading to more time wasted. Once derailed, it's hard for the recipient to mentally regain proper course. Just as with articulate engineers, plain-speaking HR specialists and literarily astute bookkeepers and accountants are in short supply, and doubtless not floating off the California coast waiting to be unloaded in bulk. Plug-and-play candidates to fill open positions are becoming an endangered species. We both agree we need to devote more time to training our own.

Our discussion turns to the private equity boom. My friend tested positive for private equity, as his firm has been acquired twice in the past four years. No known cure. He hopes the side effects are long-term, and he can cash out at an opportune time and move on to the next challenge, or maybe no challenge at all. (Ain't capitalism grand?) Whether his company is more competitive as a result is an open question that only time will answer. Whether his employees will remain employed as the debts mount and the spreadsheets are deployed to justify the metrics is another. (Their feelings about the transactions were not available at press time.) One senses a reaction akin to a Russian conscript confronted with the imminent prospect of a Ukrainian winter sightseeing tour: high risk, abundant stress, with plenty of question marks about the future.

My turn. I describe with some exasperation the junior investment bankers and family office acquisition companies that leave friendly voicemails or emails about twice monthly, reminding me of my actuarial status through their queries about our company's future ownership. So solicitous. A favorite approach comes from ex-military officers. Like this:

*I'm a West Point graduate and former Blackhawk helicopter pilot interested in buying a business in the PCBA testing and inspection services industry with $5 million to $20 million in annual sales. The other day, I came across your company and am reaching out to learn more.*

*I can offer a distinct transition opportunity for you as someone who will appreciate the hard work you've put into the business, take care of the valued members of your team, and build upon what you've established. As a company commander in the Army, I always placed the mission and my people first – and that's exactly what I'd do with your company.*

Hmm. A Blackhawk raid on a delinquent account for past-due receivables would leave an indelible impression. Distinct transition opportunity indeed.

Or this:

*I hope December is off to a great start for you and the team at Dataset* (sic). *I'm reaching out today because I'm an experienced operations leader looking to acquire and grow a* (sic) *electrical and electronic manufacturing company. If you've ever considered handing over the reins and taking some chips off the table (i.e., selling some or all of Dataset), I would love to discuss the opportunity to carry on your legacy.*

*As a prior naval officer with years of operational leadership experience, I have a commitment to service and am passionate about a company's mission and employees. I work with a core group of investors experienced in acquiring and growing high-performing companies like Dataset, and I am committed to working with the experienced management team you have put in place.*

*If you're interested in discussing your options, please let me know some times over the next week that work for a quick call. I understand this can be a sensitive topic, so please know I will maintain strict confidentiality in our discussions.*

Lieutenant, now hear this! December was off to a great start until we received your email.

"Operational Leadership Experience" begins with knowing the correct spelling of the target company. It's D-A-T-E-S-T. Please direct your service and commitment to doing your homework. Speling is @ sensitif topik.

For those who embrace pacifism, or at least a less "regimented" approach, there's this:

*I'm following up on a letter I sent you last week that discussed my serious interest in your business and whether you've considered transitioning ownership of your company. If so, I would very much appreciate the opportunity to further discuss a potential option with you.*

*As I mentioned in my letter, I founded my company with the intention of acquiring and operating a business in the testing and inspection industry, and I'm particularly interested in your company. If this sounds like an option you're interested in discussing, and you (generally) meet the criteria listed in my previous email and attachment, please contact me using this email address or the phone number below. I've also attached a brochure that further explains my background.*

As with many, this pitch reads like a rich kid with family money looking to either fill his idle time or fulfill the thesis requirement for his MBA graduation project.

The pickup line is often some variation of the same theme: *I've often wanted to get into the testing business and run a testing company on my own...* Like they've been lying awake at night all their life, harboring this elusive Test Engineering Dream, and now it's within their third-party-funded grasp.

Interestingly, the prospective acquirers are all male. In all the years of receiving such inquiries, I have yet to receive a single proposal from a female aspirant. Take from that what you will. As my companion does.

We part ways, content in being back together, sharing knowledge and swapping stories about our dysfunctional, yet thriving, industry, and reimagining the New Normal. The more things change.... ▫

# State-of-the-Art Technology Flashes

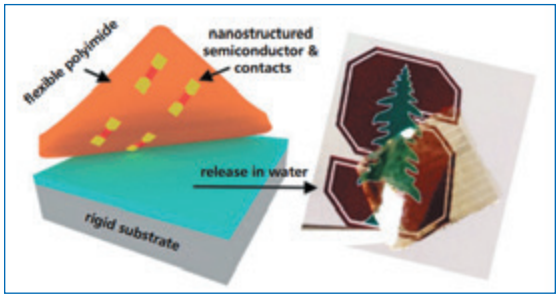
Updates in silicon and electronics technology.

*Ed.:* This is a special feature courtesy of Binghamton University.

**GARY MILLER** is technology analyst at IEEC, Binghamton University. He has over 40 years' experience in electronic packaging. He previously was the chief mechanical engineer at Lockheed Martin; gmiller@binghamton.edu.

The **INTEGRATED ELECTRONICS ENGINEERING CENTER (IEEC)** at Binghamton University is a New York Center of Advanced Technology (CAT) responsible for the advancement of electronics packaging. Its mission is to provide research into electronics packaging to enhance our partners' products, improve reliability and understand why parts fail. Research thrusts are in 2.5/3-D packaging, automotive and harsh environments, bioelectronics, flexible and additive electronics, materials for packaging and energy storage, MEMS, photonics, power electronics, sensors, embedded electronics, and thermal challenges in electronic packaging. More information is available at binghamton.edu/ieec.

**Manufacturing technique yields flexible electronics.** Stanford University researchers have invented a manufacturing technique that yields flexible, atomically thin transistors less than 100nm in length. Flexible electronics promise bendable, shapeable, energy-efficient computer circuits that can be worn on or implanted in the human body to perform health-related tasks. 2-D semiconductors have shown promise because of their excellent mechanical and electrical properties, making them better candidates than conventional silicon materials. Atop a solid slab of silicon coated with glass, they formed an atomically thin film of $MoS_2$ overlaid with small nano-patterned gold electrodes. The layering technique (chemical vapor deposition) grows a film of $MoS_2$ one layer of atoms at a time. *(IEEC file #12537, NASA Tech Briefs, 10/1/21)*



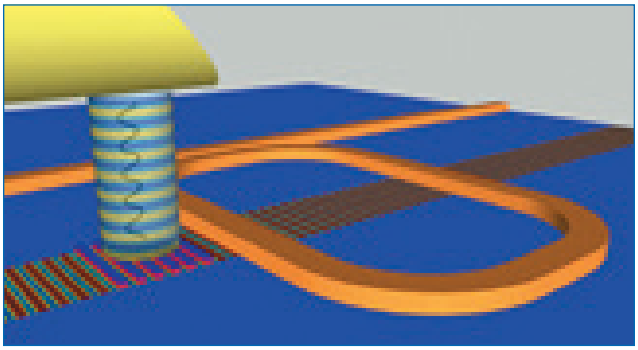

**New light sources may power next-generation quantum technologies.** Next-generation quantum technology, devices and phenomena are poised to advance with the help of a nanoscale system that could create light. Louisiana State University researchers have demonstrated the potential of metallic nanostructures to produce various forms of light. The team has also shown optical near fields provide more scattering paths that can induce complex multiparticle interactions. The coupling of single photons to collective charge oscillations at the interfaces between metals and dielectrics has led to the generation of single-surface plasmons. The findings unveil the possibility of using multiparticle scattering to perform exquisite control of quantum plasmonic systems and will provide a better understanding of the quantum properties of plasmonic systems. *(IEEC file #12538, Laser Focus World, 10/20/21)*

**Alibaba unveils "breakthrough" chip for its servers, cloud computing.** Alibaba has unveiled its general-purpose central processing unit (CPU), the Yitian 710, for its Panjiu servers that will drive the company's vast cloud computing operation. The new CPU was internally designed by Alibaba's T-Head semiconductor unit, based on architecture from British chip design company Arm. The Yitian 710 chip uses 5nm process technology, which the semiconductor industry refers to as an improved generation of chip fabrication after the 7nm process. By designing its own chip, Alibaba gets to directly improve the compute performance and power consumption of its data centers. *(IEEC file #12534, South China Morning News, 10/19/21)*


**Innovative silicon nanochip can reprogram biological tissue in living body.** Indiana University researchers have developed a silicon device that can change skin tissue into blood vessels and nerve cells. The technology, called "tissue nanotransfection," is a non-invasive nanochip device that can reprogram tissue function by applying a harmless electric spark to deliver specific genes in a fraction of a second. In laboratory studies, the device successfully converted skin tissue into blood vessels to repair a badly injured leg. The technology is currently being used to reprogram tissue for different kinds of therapies, such as repairing brain damage caused by stroke or preventing and reversing nerve damage caused by diabetes. *(IEEC file #12598, Science Daily, 12/10/21)*

**Optomechanical signal processing through acoustic wave interference on a silicon chip.** Optical signal processing using the phase, intensity or polarization of light is a rapidly growing field, along with the development of nanophotonics process technology. POSTECH researchers have successfully demonstrated an optical wave signal that can be amplified or canceled using optically driven acoustic waves on

a silicon chip. They used an active optical signal processing method using the interference of acoustic waves generated on a silicon chip. Three optical waveguides were fabricated side by side on a silicon chip via nano-processing. Two acoustic waves were interfered with by generating acoustic waves in two optical waveguides using optical forces and controlling the time to reach the third optical waveguide. *(IEEC file #12555, Semiconductor Digest, 11/3/21)*

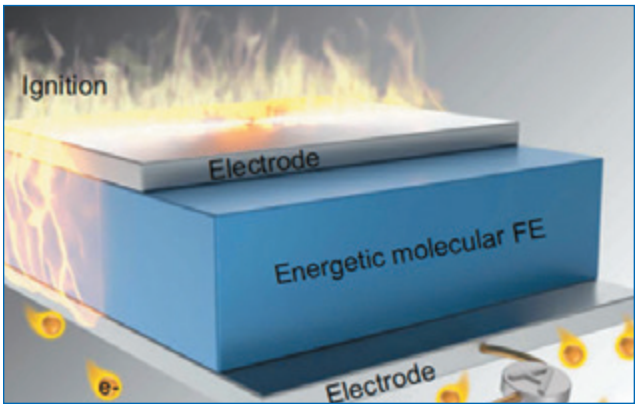


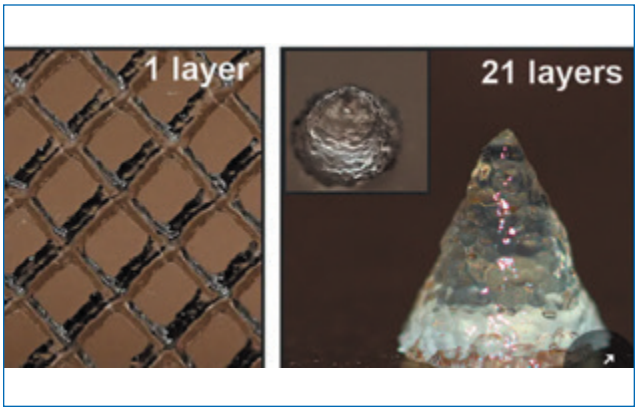
High-speed laser writing method could pack 500TB of data into CD-sized glass disc. University of Southampton researchers have developed a fast and energy-efficient laser-writing method for producing high-density nanostructures in silica glass. These tiny structures can be used for long-term 5-D optical data storage that is more than 10,000 times denser than Blu-Ray optical disc storage technology. The new approach can write at speeds of 1,000,000 voxels per second, which is equivalent to recording about 230kB of data per second. The physical mechanism used is a generic and energy-efficient writing method that could also be used for fast nanostructuring in transparent materials for applications in 3-D integrated optics and microfluidics. *(IEEC file #12557, Science Daily, 10/28/21)*

Energetic ferroelectrics. Energetic materials store a large amount of chemical energy that can be converted into mechanical energy. Energetic materials in the form of molecular crystals store chemical energy, while their strong electron-phonon coupling interactions promise high-energy density through thermal waves. At the same time, symmetry breaking in molecular crystals induces self-polarization and electron-phonon interaction, leading to molecular ferroelectrics. University at Buffalo, University of Maryland and ARL researchers studied if these two can somehow be combined to obtain a chemically driven electrical energy source with high-power density. Such a power source could be employed for on-demand energy sources, propulsion or thermal batteries. This work demonstrates the design of energetic molecular ferroelectrics consisting of imidazolium cations and perchlorate anions, showing a high-power density comparable to Li-ion batteries. *(IEEC file #12559, Science Daily, 10/28/21)*

New ultra-high material-efficient low-cost solar cells using nanowires. Norwegian University researchers have developed a method for making an ultra-high material-efficient solar cell using semiconductor nanowires. If this is placed on top of a traditional silicon-based solar cell, it could potentially double the efficiency of today's Si solar cells. The method uses GaAs material in a very effective way through nanostructuring, so solar cells are much more efficient. The most cost-effective and efficient solution is to grow a dual-tandem cell, with a GaAs nanowire cell on the top grown on a bottom Si cell, which avoids the use of an expensive GaAs substrate. The tiny footprint of the nanowire structure provides an additional benefit because it permits high quality in crystals in the nanowire and in the interface with the silicon, which helps improve the solar cell performance, making an ultra-high power-per-weight ratio solar cell that is more than 10 times more efficient than any other solar cell. *(IEEC file #12558, Science Daily, 10/28/21)*

This ink is alive and made entirely of microbes. Northeastern University researchers have created a bacterial ink that reproduces itself and can be 3-D-printed into living architecture. The microbial ink flows like toothpaste under pressure and can be 3-D-printed into various tiny shapes: a circle, a square and a cone, all of which hold their form and glisten like Jell-O. This new substance is not the first-ever living ink. Scientists have previously created printable gels that were cocktails of bacteria and polymers that helped provide structure when printed. One such ink contained hyaluronic acid, a seaweed extract and fumed silica. *(IEEC file #12578, The New York Times, 11/24/21)*



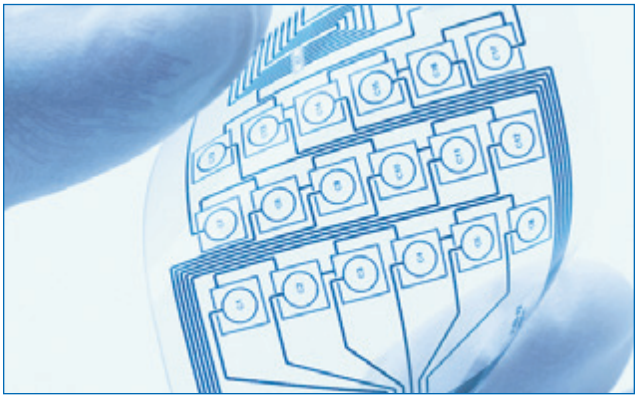
**Roswell Biotechnologies unveils first molecular electronics chip to digitize biology.** Roswell Biotechnologies announced the introduction of the first molecular electronics chip for biosensing applications. The Roswell ME Platform integrates single molecules into electronic circuits acting as sensor elements to create the first fully scaled biosensors on standard semiconductor chips. The sensor translates the dynamic process of molecular interactions into electrical measurements in real-time. The sensor targets are programmed according to the particular molecule wired into the chip, providing for a programmable and universal biosensor platform. This single-molecule measurement with resolution for individual binding events enables an unprecedented and information-rich view of biology to transform major markets. Applications include drug discovery, molecular diagnostics and sequencing. *(IEEC file #12564, PR Newswire, 11/15/21)*

## Market Trends

**Worldwide quantum dot industry expected to reach $8.6 billion in 2026.** The global quantum dot market is estimated to be worth $4 billion in 2021 and is projected to reach $8.6 billion by 2026, a CAGR of 16.2%. Increasing demand for quantum dots in display devices, advanced features of quantum dots and the diverse applications of quantum dots are some of the major factors driving the growth of the quantum dot market. Many quantum dot manufacturers are switching from toxic cadmium-based quantum dot devices to cadmium-free quantum dot devices. This act is in accordance with the RoHS directive in electrical and electronic equipment. Cadmium-free quantum dots are not only suited for displays but also applications such as lighting solutions, solar cells and biomedicine. *(IEEC file #12545, Semiconductor Digest, 10/20/21)*

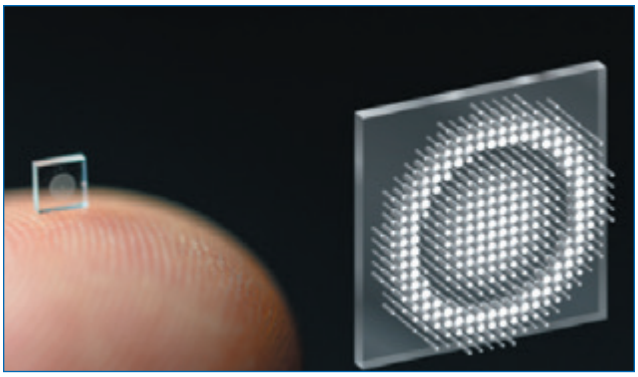
**Wireless charging: With WiGL, battery power is in the air.** Smart wireless power company WiGL completed an experiment demonstrating an ad-hoc mesh networking capability to allow wireless recharging of connected devices at distances of more than 5 ft. from a power source. The power source would be one of a series of transmitters on a wireless grid LAN (WiGL), embedded in walls or deployed in other ways around an indoor space. Each transmitter would be equipped with cellular-like beam-steering to allow a device in movement around a room to continue receiving a power charge as its signal gets handed off from one transmitter to another. Essentially, this renders irrelevant the need to monitor device battery levels while inside the coverage area, and device users would no longer need to impatiently check their devices every few minutes to see how close they are to fully recharged. *(IEEC file #12551, Fierce Electronics, 10/28/21)*

**Flexible sensors slide into the future with electronic printing.** A new method of "sliding" delicate high-performance electronics onto flexible surfaces could enable future developments in electronics. University of Glasgow researchers have found a way to solve one of the key problems of contact printing. The ability to reliably reproduce the same device at high volumes is key to developing an electronic product and bringing it to market. The team began by fabricating zinc oxide nanowires on a rigid surface, then designed an automated system to transfer the nanowires from their surface they were created on – the "donor" surface – to a sheet of flexible silicon (receiver surface). The system allows the team to mechanically control the movements of two flat platforms, which can pivot to ensure they align correctly to make the transfer happen smoothly. *(IEEC file #12549, Printed Electronics World, 10/25/21)*



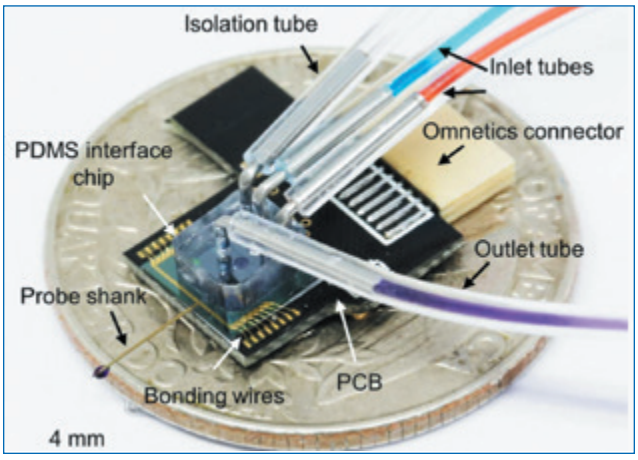
**Artificial intelligence in healthcare market worth $67.4 billion by 2027.** The artificial intelligence (AI) in healthcare market is projected to grow from $6.9 billion in 2021 to $67.4 billion by 2027, a CAGR of 46.2% from 2021 to 2027. Key factors fueling the growth of the market include market influx of large and complex healthcare datasets, a growing need to reduce healthcare costs, improving computing power and declining hardware cost, a rising number of partnerships and collaborations among different domains in the healthcare sector, and a surging need for improvised healthcare services due to imbalance between health workforce and patients. Additionally, the growing potential of AI-based tools for elderly care, an increasing focus on developing human-aware AI systems, and a rising potential of AI technology in genomics, drug discovery, and imaging and diagnostics to fight Covid-19 are expected to create a growth opportunity for the artificial intelligence in healthcare market. *(IEEC file #12565, Fierce Sensors, 10/27/21)*

**Researchers shrink camera to the size of a salt grain.** Micro-sized cameras have great potential to spot problems in the human body and enable sensing for super-small robots, but past approaches captured fuzzy, distorted images with limited fields of view. Princeton University researchers have overcome these obstacles with an ultracompact camera the size of a coarse grain of salt. The new system can produce crisp, full-color images on par with a conventional compound camera lens. A key innovation in the camera's creation was the integrated design of the optical surface and the signal processing algorithms that produce the image. *(IEEC file #12589, Semiconductor Digest, 11/29/21)*



**Power module packaging market will grow to around $3.6 billion by 2026.** In 2020, motor drives represented the most significant power module market, with a value of $1.6 billion. By 2026, EV/HEVs will become the most significant power module market, with a market value of $3.6 billion. In addition, the power module packaging raw materials market will reach $3.5 billion by 2026. The power, frequency, efficiency, robustness, reliability, weight, volume and cost requirements of automotive power modules are often more severe than industrial products due to safety standards and harsh environments. SiC semiconductors provide higher efficiency compared to silicon-based die. SiC-based power modules are also gaining popularity in the automotive market. The introduction of SiC technology pushes the development of new power packaging solutions, as SiC devices can work at higher junction temperatures and higher switching frequencies with smaller die sizes. *(IEEC file #12586, Semiconductor Digest, 11/18/21)*

**Brain chip combines microfluidics and electrodes.** KIST researchers have micromachined a multifunctional brain chip with microelectrodes for recording electrical activity, microfluidic channels for sampling extracellular fluid, and a microfluidic interface chip for multiple drug delivery and sample isolation. The cerebrospinal fluid, which is tested for neurotransmitters, is extracted at a low pressure to minimize channel blockages from prolonged use. The brain chip is small, yet it can perform various functions simultaneously. It will be useful in minimizing brain damage and studying brain diseases. *(IEEC file #12592, Electronics Weekly, 12/2/21)*




## Recent Patents

**Hybrid gate stack integration for stacked vertical transport field-effect transistors (assignee: IBM Corp.) patent No. US11139215.** A method of forming a semiconductor structure includes forming one or more vertical fins, each including a first semiconductor layer providing a vertical transport channel for a lower vertical transport field-effect transistor (VTFET) of a stacked VTFET structure, an isolation layer over the first semiconductor layer, and a second semiconductor layer over the isolation layer providing a vertical transport channel for an upper VTFET of the stacked VTFET structure. The method also includes forming a first gate stack, including a first gate dielectric layer and a first gate conductor layer surrounding a portion of the first semiconductor layer of the vertical fins.

**Method for fabricating nanopillar solar cell using graphene (assignee: Semiconductor Manufacturing International) patent No. US11139405.** A method of manufacturing a semiconductor device includes providing a substrate structure. The substrate structure includes a conductive layer and a plurality of nanopillars spaced apart from each other overlying the conductive layer. Each nanopillar includes a first semiconductor layer and a second semiconductor layer on the first semiconductor layer. The semiconductor layers have different conductivity types. The method also includes forming a graphene layer overlying the plurality of nanopillars. The graphene layer is connected to each of the plurality of nanopillars.

**Package to printed circuit board transition (assignee: Google) patent no. 11,147,161.** Package to printed circuit board transitions are described. In one aspect, a multilayer PCB includes an external layer having a transition region configured to receive an electrical component and a clear routing region outside of the transition region. The PCB includes first via(s) that extend from the transition region to an inner trace routing layer. The trace routing layer is disposed between the external layer and the second inner trace routing layer. The first inner trace routing layer includes a transition area disposed under the transition region of the external layer, a clear routing area outside of the transition region, and a transmission line that connects a via to a second via for a second electrical component.

**Thermal conductivity for integrated circuit packaging (assignee: Intel Corp.) patent no. 17/147,153.** Aspects of the embodiments include an edge card and methods of making the same. The edge card can include a printed circuit board comprising a first end and a second end, the first end comprising a plurality of metal contact fingers configured to interface with an edge connector, and the second end comprising a through-hole configured to mate with a post of a screw, the PCB further comprising an aperture proximate the second end of the PCB. The PCB can also include a thermal conduction

element secured to the PCB, the thermal conduction element supporting an integrated circuit package, the integrated circuit package received by the aperture, wherein the thermal conduction element contacts the PCB proximate the through-hole, and the thermal conduction element is configured to conduct heat from the integrated circuit toward the second portion of the PCB.

**Transparent PCB and method for manufacturing (assignee: Qing Ding Precision Electronics) patent no. 11,134,564.** A transparent PCB includes a transparent base film, a hardened layer, an electrode film, a first conductive paste, a second conductive paste and an electronic component. The hardened layer is formed on a side of the transparent base film. The electrode film is formed on a side of the hardened layer. The electrode film includes a first transparent conductive oxide layer, a metal layer and a second transparent conductive oxide layer. The first conductive paste is formed on the electrode film. The second conductive paste is formed on the electrode film and spaced from the first conductive paste. The electronic component is electrically connected to the electrode film through the first conductive paste and the second conductive paste.

**Multi-stack 3-D memory devices (assignee: Yangtze Memory Technologies) patent No. WO2021207351.** Embodiments of 3-D memory devices having multiple memory stacks and methods for forming the 3-D memory devices are disclosed. In an example, a 3-D memory device includes a first device chip, a second device chip, and a bonding interface. The first device chip includes a peripheral device and a first interconnect layer. The second device chip includes a substrate, two memory stacks disposed on opposite sides of the substrate, two memory strings each extending vertically through one of the two memory stacks, and a second interconnect layer. The bonding interface is formed vertically between the first interconnect layer of the first device chip and the second interconnect layer of the second device chip.

**Fabrication of a microfluidic chip package or assembly with separable chips (assignee: IBM Corp.) patent No. 11,198,119.** The invention is notably directed to methods of fabrication of a microfluidic chip package or assembly, providing a substrate having at least one block comprising one or more microfluidic structures on a face of the substrate; partially cutting into the substrate to obtain partial cuts, such that a residual thickness of the substrate at the level of the partial cuts enables singulation of said at least one block; cleaning said at least one block; and applying a cover-film to cover said at least one block, whereby at least one covered block is obtained, the applied cover film still enabling singulation of each covered block, where each block corresponds to a microfluidic chip after singulation. ▫

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*Material Gains, continued from pg. 20*

Of course, much depends on the availability of suitable software to create these environments and challenges. The scale of the internet can come to the rescue here, enabling facilities to be made available on a similar basis to today's mobile apps: Visit your metaverse store for low-cost or even free apps, possibly monetized on a subscription basis or through in-app purchases.

Then there is the question of hardware. Apple is reportedly working on a VR headset that is expected to be extremely lightweight – less than one pound, with later models weighing even less. Of course, headset weight is a key metric for any VR application to avoid discomfort. Weight is even more important in the metaverse, however, where users will expect to be comfortable for extended periods.

Numerous challenges must be overcome when packaging high-computing performance into a wearable form factor. Effective thermal management, of course, is extremely important and a huge challenge. In addition to lightweight for comfort, designers will be under pressure to create attractive designs people will want to wear. We can expect creative solutions, particularly using shaped, insulated metal substrates.

On the other hand, the supply of space-saving technologies like flexible printed circuit (FPC) will experience increased pressure. The automotive sector is already placing a huge demand for FPCs, as vehicle electrification continues to rise. It is reckoned future electric vehicles could contain more than 100 circuits on FPCs.

We can also look forward to exciting developments in sensors for contextual awareness. Leading MEMS sensors are already integrating small, embedded machine-learning cores that enable smarter functionality and faster response than their predecessors. Sensing techniques also are undergoing a significant change with the advent of sophisticated depth-sensing based on infrared time-of-flight measurements. These enable much faster and more energy-efficient 3-D perception than conventional imaging techniques. The sum of all these parts could deliver compact, stylish, low-power and comfortable wearables that enable us to exist quite naturally in the metaverse.

As this concept evolves, I am sure the most successful applications will be those that enhance our connections with each other. I would compare it with the original Facebook, which overpowered competitors and predecessors simply by offering more and better ways for people to interact, in real-time and through various groups, to share as many aspects of their lives and interests as they wish.

No doubt escapism and entertainment will be the main priorities for a sizeable number of metaverse users, but I see many opportunities to help people improve their well-being, achieve ambitious personal goals, and enhance working experiences. It does have great potential to make the real world a better place. ▫

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## ALTIUM DESIGNER 22

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**Altium**
**altium.com/altium-designer/whats-new**

## T-TECH ISOPRO 6.0 SOFTWARE

Quick Circuit systems are equipped with IsoPro software, which enables automatic data conversion from almost any CAD package. Is designed to be intuitive and has the ability to import DXF and export Gerber data.

**T-Tech**
**t-tech.com/product-category/isopro-software/**

## ROGERS RADIX 3-D PRINTABLE DIELECTRICS

Radix 3-D printable dielectrics material features dielectric constant of 2.8 and low loss characteristics at microwave frequencies. Radio frequency designers can create new components, reportedly eliminating need to consider typical manufacturing design constraints. Composite materials are designed for digital light processing 3-D printing, enabling scalable, high-res printing process for end-use RF dielectric component manufacturing. Dissipation factor is 0.0043 at 10GHz when cured. Intended for use as RF materials in applications where new geometric freedom can enhance figure of merits of RF system, such as gradient dielectric constant structures and other 3-D parts. Can manufacture systems and components at scale.

**Rogers Corp.**
**rogerscorp.com**

## ALTAIR POLLEX ESD SOFTWARE FOR ALTIUM

Altair PollEx electronic system design software is free for Altium users. Predicts and maximizes PCB performance and verifies manufacturability. Supports ECAD software products including Altium Designer. Reportedly makes board-level simulation and design verification features accessible to Altium Designer users.

**Altair**
**altair.com/pollex-for-ecad**

## ASM MATERIAL TOWER

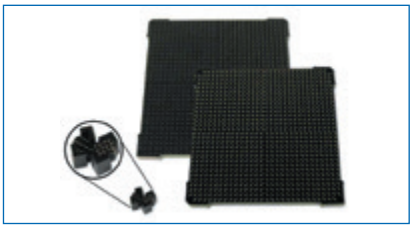
New generation of ASM Material Tower supports classic manual withdrawals, as well as fully automated AIV-supported material flow processes in integrated smart factory. With intelligent software control, modular storage system is versatile, scalable and interconnected. Multiple towers can be combined into clusters where material is exchanged between units via integrated transport module. Distribution of materials within storage system is handled by intelligent algorithms. Number and type of transfer points can be flexibly selected and modified for manual operation and for use with autonomous transport systems. Is designed to hold up to 960 7" reels or 480 15" reels. Packages can be supplied or withdrawn in magazines holding up to 30 reels for specific setups. MSDs can be stored and exposure times monitored. Software handles vertical integration into range of MES solutions. Is fully integrated into ASM Works software infrastructure; can be linked to ASM Material Manager software module. Standalone operation or connection to third-party solutions is possible via Tower Cluster Controller.

**ASM**
**asmpacific.com**

## PANASONIC MEGATRON 8

Megatron 8 material for multilayer printed circuit boards is for high-speed communication networking equipment such as routers and switches. Combines resin design expertise with ultra-low dielectric dissipation factor glass cloth and low-profile copper foil; improves dielectric properties of material for low transmission loss required for high-performance, high-layer-count PCBs on existing PCB manufacturing lines. Reportedly reduces transmission loss for PCB materials at 28GHz by 30% compared to Megatron 7. Thermoset resin material has heat resistance and reliability similar to previous generation; has same manufacturability and processability as conventional PCB laminate and can be manufactured using standard multilayer PCB processes. Comes in two types of glass cloth products.

**Panasonic**
**panasonic.com/global/corporate/industry.html**



## IRONWOOD GRYPPER

Grypper test sockets are for BGA devices, including large array ASICs; I/O down to 0.35mm pitch. Can be designed to any I/O count specific to custom BGA requirements for characterization, validation and failure analysis. G80 LIF allows testing of 896 I/O, 31 x 31 0.80mm pitch BGA. Small socket is 12-ball socket at 0.40 pitch and 1.2 x 1.6mm; incorporates built-in alignment corners. To connect device, insert into socket by pressing on top of device; no lid is required. Contact grips onto solder balls of device. Extraction tool can be used to pop device out of socket. Electrical performance of -1dB insertion loss to greater than 40GHz. Force required to insert a device is 25gm/contact. Configurations: Socket with RoHS solder

ball (SAC 305) replicates device; socket configured with SnPb solder ball allows reflow/attachment onto PCB that has components mounted. Lower melting temp. of SnPb solder will not affect any adjacent components that might be close to target area where socket is to be placed. Socket can be purchased with no solder balls. Non-solder-ball version requires use of 0.2mm-thick stencil for correct amount of solder paste.

**Ironwood Electronics**
**ironwoodelectronics.com**

## WELLER LASER LINE 400V

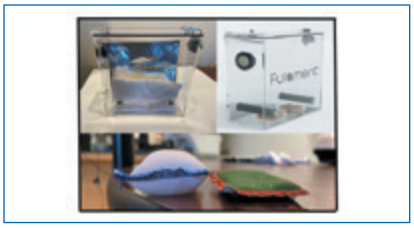
Laser Line 400V fume extraction unit has blower capacity of 615 $m^3/h$. Is designed to purify air from industrial machines; can be coupled with up to eight workplaces. Is expandable (modular) for greater prefilter volumes. Comes with HEPA H13 particle filter and fine-dust pre-filter (class F7). Is for laser marking, grinding, cutting and welding with high amounts of dust. Incorporates constant flow control. Electronic filter control includes visual and audible filter alarm. Performs efficiency tests via USB port.

**Weller Tools**
**apextoolgroup.com**

## TELEDYNE FLIR X858X AND X698X

X858x and X698x science cameras provide high-speed and high-res thermal imaging for scientific research and engineering applications, including PCB test and measurement, within mid-wave infrared and long-wave infrared spectrum. Offer recording, triggering, and synchronization capabilities. Can remotely adjust focus, improving quality of thermal data acquisition. Can transfer data from onboard solid-state drive to computer for processing and analysis, executed through FLIR Research Studio or the FLIR Science Camera SDK. Enable users to immediately access local copy of data. Support long-duration recordings, only limited by size of on-board, off-the-shelf SSD. Include dedicated trigger input on rear panel and tri-level sync input, providing access to all methods of recording and synchronization across multiple camera units and types. In combination with motorized lens support, each model includes integrated four-position filter wheel; can be loaded with neutral density or spectral filters. Feature cooled thermal camera core with high-def res (1280 x 1084) and 180Hz frame rate. Feature 640 x 512 thermal res with greater than 1kHz frame rate.

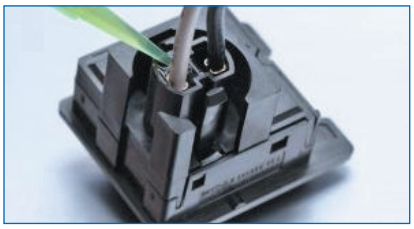
**Teledyne FLIR**
**flir.com/instruments/science/next-generation-x-series**



## STEEL CAMEL FULABOX

Fulabox dry box controls condensation that attacks moisture-sensitive devices and filament. Matched with Moisture Hog desiccant bags, it can pull diffused moisture out of parts over time at ambient temp. Reduces damage caused by heat. Has robust seals, hardware and easy setup for filament delivery. Testing available upon request.

**Steel Camel**
**steelcamel.com**



## MASTER BOND EP21AC

Master Bond EP21AC is a two-part epoxy with non-halogenated filler formulated for applications where arc resistance and flame retardancy are required. PLC (performance level category) of 0 under UL746A High Amp Arc Ignition test. Flame-retardant, per UL94HB standard for flammability testing. Suitable for encapsulating, potting or coating. Elongation of 10% to 20%. Can resist thermomechanical stresses. Volume resistivity greater than $10^{14}$ohm-cm. Has dielectric constant of 4.7 at 75°F. Other properties include tensile strength of 5,000-6,000psi and tensile modulus of 300,000-350,000psi at 75°F. Is serviceable over temp. range of -60° to +90°C; 1 to 1 mix ratio by weight; cures at room temp. or more rapidly with heat. Mixed viscosity is 30,000-50,000cps. Working life is 75-120 min. at room temp. Bonds to metals, ceramics, composites and many plastics and rubbers.

**Master Bond**
**masterbond.com**

## SCS PRECISIONCURE UVC (MUV)

SCS PrecisionCure UVC microwave UV curing system features programmable curing profiles and small footprint. Also features lamp movement trolley that enables UV lamp to move across horizontal axis over product on conveyor. Can customize each profile to vary dosage of UV exposure on different components of single board. Uses Heraeus Noblelight microwave-activated UV lamps. Comes in single, double and triple lamp configurations. Operates as standalone machine or as complement to SCS PrecisionCoat selective conformal coating and dispense system. Features Windows-based software with touchscreen monitor and is designed for continuous operation.

**Specialty Coating Systems**
**scsequip.com**

## INDIUM FINE DIAMETER FLUX-CORED WIRES

Fine diameter 0.004" (0.10mm) flux-cored wire is made with Pb-free alloys to help meet requirements of fine-pitch applications. Designed to provide fine wire for increased solder joint density and miniaturization in applications where solder paste reflow and other soldering approaches are not effective, such as robotic soldering for fine-pitch attachment of small components to medical devices or fine-pitch PCB assemblies. Hand soldering and rework may be possible. Fluxes recommended are Core 230-RC and CW-807. Fine diameter wire is available in SAC 305; SAC 387; Sn96.5Ag3.5; Sn96.3Ag3.7; and Sn96Ag4.

**Indium**
**indium.com/flux-cored-wire**

# In Case You Missed It

This column provides abstracts from recent industry conferences and company white papers. Our goal is to provide an added opportunity for readers to keep abreast of technology and business trends.

## Semiconductors

"Molecular Electronics Sensors on a Scalable Semiconductor Chip: A Platform for Single-Molecule Measurement of Binding Kinetics and Enzyme Activity"

*Authors:* Carl W. Fuller, *et al.*

*Abstract:* For nearly 50 years, the vision of using single molecules in circuits has been seen as providing the ultimate miniaturization of electronic chips. An example of such a molecular electronics chip is presented here, with the important distinction that the molecular circuit elements play the role of general-purpose single-molecule sensors. The device consists of a semiconductor chip with a scalable array architecture. Each array element contains a synthetic molecular wire assembled to span nanoelectrodes in a current monitoring circuit. A central conjugation site is used to attach a single probe molecule that defines the target of the sensor. The chip digitizes the resulting picoamp-scale current-versus-time readout from each sensor element of the array at a rate of 1,000 frames per second. This provides detailed electrical signatures of the single-molecule interactions between the probe and targets present in a solution-phase test sample. This platform is used to measure the interaction kinetics of single molecules, without the use of labels, in a parallel fashion. (*Proceedings of the National Academy of Sciences,* February 2022, www.pnas.org/content/119/5/e2112812119)

## Solder Joint Reliability

"Effect of the Welding Process on the Microstructure and Mechanical Properties of Au/Sn–3.0Ag-0.5Cu/Cu Solder Joints"

*Authors:* Xinmeng Zhai, Yue Chen, Yuefeng Li, Jun Zou, Mingming Shi, and Bobo Yang

*Abstract:* This paper investigates the influence of the welding process on the microstructure and mechanical properties of Au/Sn-3.0Ag-0.5Cu/Cu solder joints. In this study, the flip-chip LED chip and the substrate were connected by a heating platform, hot air reflow, and vacuum reflow soldering methods to form Au/SnAgCu/Cu composite solder joints. Sn-3.0Ag-0.5Cu is selected as the solder. The microstructure of the solder joint interface and the inferred surface is studied to characterize the influence of different welding methods on the intermetallic compound (IMC) interface. The void ratio of the flip-chip solder layer was tested to characterize the effect of the effective connection area between the chip and the solder joint on the shear strength. The experimental results show the void ratio of the solder joints welded by the heating platform is as high as 26%; the IMC interface thickness is higher; and the diffusion coefficient of the solder is the lowest. The void distribution of hot air reflow soldering joints is relatively uniform, and there is less solder residue on the fractured surface. Vacuum reflow soldering has the lowest void rate in the solder joints, and the solder joints have flat cross sections with almost no solder residues. The fracture occurs at the lower layer of solder. When the soldering method is vacuum reflow, the IMC layer of the flip-chip solder joint is the thinnest, and the diffusion coefficient of the solder is the highest. There are almost no voids in the solder layer, and the mechanical properties of the solder joint are the best. At this time, the photo-thermoelectric parameters of the filament are the best, and the performance is the most stable and reliable. (*Journal of Electronic Materials,* January 2022, https://link.springer.com/article/10.1007/s11664-021-09426-1)

## Flexible Electronics

"Stencil Printing of Liquid Metal upon Electrospun Nanofibers Enables High-Performance Flexible Electronics"

*Authors:* Dr. Zhao Gang, *et al.*

*Abstract:* The authors report on a simple, fast, and green flexible electronics preparation technology. The stencil printing method is adopted to pattern liquid metal on the thermoplastic polyurethane membrane prepared by electrospinning. With layer-by-layer assembly, flexible circuits, resistors, capacitors, inductors, and their composite devices can be prepared parametrically. These devices have good stretchability, air permeability and stability, while they are multilayered and reconfigurable. This strategy is used to fabricate flexible displays, flexible sensors and flexible filters. Flexible electronic devices are also recycled and reconfigured. (*ACS Nano,* November 2021, https://pubs.acs.org/doi/10.1021/acsnano.1c05762)

"Prediction of Solder Joint Reliability with Applied Acrylic Conformal Coating"

*Authors:* Duarte Nuno Vieira, *et al.*

*Abstract:* Conformal coating is not recommended in some components such as BGA and QFN packages since it can reduce solder joint reliability when exposed to temperature fluctuations. Therefore, by using a finite element analysis, a thermal cycle test was simulated with and without conformal coating. The simulation output was extrapolated to lifetime theoretical methods to predict the number of cycles until the failure of the solder joints. This study demonstrates that for both components without conformal coating, solder joint lifetime was a precise approximation. Coated solder joints reveal a drastic reduction in their reliability due to the influence of the conformal coating behavior and its thermomechanical properties. (*Journal of Electronic Materials,* October 2021, https://link.springer.com/article/10.1007/s11664-021-09232-9)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