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IEEC

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College Training Programs for Electronics with JOHNNY VANDERFORD and COURTNEY TENHOVER

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PRINTED CIRCUIT DESIGN & FAB/CIRCUITS ASSEMBLY is distributed without charge to qualified subscribers. For others, annual Subscription Rates in U.S. funds are: \$80 (U.S. and Canada), \$145 (all other countries). Single copy price is \$8.50. All subscription and single copy orders or inquiries should be directed to PRINTED CIRCUIT DESIGN & FAB/CIRCUITS ASSEMBLY, PO Box 470 Canton, GA 30169, email subscriptions@upmediagroup.com.

PRINTED CIRCUIT DESIGN & FAB/CIRCUITS ASSEMBLY is published monthly by UP Media Group Inc., PO Box 470 Canton, GA 30169. ISSN 1939-5442. GST 124513185/ Agreement #1419617.

Periodicals postage paid at Canton/Ball Ground, GA, and additional mailing offices. © 2022, UP Media Group, Inc. All rights reserved. Reproduction of material appearing in PRINTED CIRCUIT DESIGN & FAB/CIRCUITS ASSEMBLY is forbidden without written permission.

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MIKE BUETOW EDITOR-IN-CHIEF

Next-Generation Engineers Need Next-Generation Training

OU KNOW THE labor situation is bad when even the Air Force is getting involved to find solutions.

Indeed, as was recently announced, the Air Force Research Laboratory is working with NextFlex to come up with ways to attract students to careers in technology and science.

NextFlex isn't a random choice. It was formed under the auspices of the US Department of Defense's Manufacturing Technology Program. As one of eight DoD Manufacturing Innovation Institutes, the consortium is a partnership among the DoD, industry and academia. Its specific focus is development of flexible hybrid electronics (FHE), and to develop an education and workforce development program.

To the latter, the goal is nothing less than the creation of a skilled pipeline of STEM talent ranging from R&D to manufacturing. To that end, NextFlex is working on training and recruitment programs that work hand-in-hand with existing curricula. Called FlexFactor, this model is considered far more effective than designing a program from scratch and convincing institutions to adopt it.

In these programs, students attempt to address real-world problems, create the hardware that might solve that problem, and design the business model for their solution. They are similar to capstone projects at universities such as Rochester Institute of Technology, which go a long way toward resolving the criticism that higher education teaches only theory and leaves graduates woefully short on relevant industry experience.

"Colleges adopt and run FlexFactor for local high school students in their service area as a means of engaging students with STEM pathways in higher education," says Emily McGrath, workforce development director, NextFlex. "So, although the participants are all in high school, the teams represent their colleges (not their high schools) in the finals because we work with the colleges, not the high schools, to run the program."

This is appealing, I think, because today's students seem much more driven by hands-on instruction and an accelerated path to accomplishment.

One of the facets of the Printed Circuit Engineering Association is to promote printed circuit engineering as a profession and to encourage, facilitate, and promote the exchange of information and integration of new design concepts through communications, seminars, workshops, and professional certification. So central is training to our mission, we spell it out in our bylaws.

We have affiliated with PCE-EDU, a training

company established by some of the leading names in printed circuit engineering and manufacturing tooling. They include Rick Hartley, Mike Creeden, Susy Webb, Steph Chavez, and Gary Ferrari. They have developed a 400-page handbook (*Printed Circuit Engineering Professional*) that covers more than 65 major topics ranging from design to materials and fabrication processes. (I should note several of the aforementioned experts will be presenting at our PCB East conference in Marlboro, MA, in April.)

To teach the principles set forth in the Printed Circuit Engineering Professional curriculum, PCE-EDU has set up a five-day course covering the basics of the profession, materials, manufacturing methods and processes; circuit definition and capture; board layout data and placement; circuit routing and interconnection; signal-integrity and EMI applications; flex PCBs; documentation and manufacturing preparation; and advanced electronics (energy movement in circuits, transmission lines, etc.). At the end of the workshop, registrants may take the optional certification, called the CPCD, or Certified Printed Circuit Designer. PCEA is the registrar and certifying body for the CPCD.

Again, the emphasis is on real-world engineering and design, not pie-in-the-sky theory. Students are taught facts and principles in a tool-agnostic way. One medium-term goal is to get institutions to adopt the CPCD, much in the way they are latching onto FlexFactor, so students are not just aware of careers in printed circuit engineering and manufacturing, but prepared for them.

Not so long ago, a Lockheed-Martin engineer keynoting an industry conference extolled the virtues of the F-35 joint strike fighter. And I admit, the warfighter is a freak of advanced engineering. But after his presentation, I asked what L-M was doing to compete with the Facebooks and Googles to attract the next generation of engineers. His somewhat incredulous "what, me worry?" response: "Who wouldn't want to work on a machine like this?"

The answer, of course, is far too many people.

Covid has highlighted the skilled labor shortage experienced at many technology companies over the past three decades. Finding the right employees is an ongoing industrywide problem. Fortunately, programs by organizations like NextFlex and PCEA are starting to fill the void. \Box

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PCDF People

Canadian Circuits appointed **Richard Denier** general manager.



MacDermid Alpha Electronics Solutions appointed Erik Weyls vice president, Circuitry Solutions. He most recently held several positions of executive leadership with Coventya, a

specialty chemicals solutions provider.

Microsoft named **lan Jackson** PCB layout team manager.



Nano Dimension appointed Greg Caldwell vice president of global marketing. He previously was head of marketing and sales enablement with Anark, and has held director level posi-

tions at 3D Systems, Microsoft and Sun Microsystems.



Printed Circuits promoted **Bob Burns** to vice president, sales and marketing. He has been with the fabricator in sales for more than 20 years.



Summit Interconnect named Carl Schlemmer quality assurance manager. He has held a variety of management and sales positions in fabrication since the mid-1970s, most

recently with Eagle Electronics.



Gerry Partida to vice president of technology. He has more than 30 years' experience in PCB fabrication with Summit, Marcel Electronics and Orbotech.

Summit Interconnect promoted

Technic appointed **Denis Jacques** global product manager of PWB products.



Uyemura USA announced **Tony Revier (top left)**, founder and president, has entered a threeyear agreement to focus exclusively on primary accounts, and on international relations. Vice president of sales **Mark Eonta** becomes president and CEO. He joined the company in 2012.

PCDF Briefs

Altair CTO Brett Chouinard says the future of design engineering includes more engineers who understand data science and local solutions for supply chain issues.

The technological benefits that 3-D stacking of integrated circuits brings have the potential to ease chip shortage concerns, according to **Cadence**.

PCB West Issues Call for Abstracts for Fall Show

ATLANTA – UP Media Group Inc. seeks abstracts for its annual PCB West technical conference coming in 2022. PCB West will be held October 4 to 7, 2022, in Santa Clara, CA. The event includes a four-day technical conference and one-day exhibition to be held at the Santa Clara (CA) Convention Center.

Presentations of the following durations are sought for the technical conference: one-hour lectures and presentations; two-hour workshops; and half-day (3.5 hour) and full-day seminars.

Preference is given to presentations of two hours in length or more, and no presentations of less than one hour will be considered.

Papers and presentations must be noncommercial in nature and should focus on technology, techniques or methodology. Abstracts of 100 to 500 words and speaker biographies should be submitted to pcbwest.com/abstract-submission-guidelines by Feb. 25. Accepted presentations are due Aug. 31.

Speakers receive complimentary access to the online proceedings, complimentary pass to the technical conference, and more.

PCD&F/CIRCUITS ASSEMBLY is media partner for the event, and the Printed Circuit Engineering Association is a sponsoring association. (CD)

Nan Ya PCB to Acquire Symtek Automation Asia

TAICHUNG CITY, TAIWAN – Nan Ya Printed Circuit Board announced it is acquiring Symtek Automation Asia for NT\$502.3 million (US\$18 million). A 30% deposit will be paid; 60% will be paid after delivery, and 10% after acceptance.

Executive officers approved the transaction after the procurement organization completed a price comparison and negotiation.

Symtek supplies printed circuit board and semiconductor process equipment. It has over 350 employees in Zhongli, Taiwan, and over 350 employees in Dongguan, China. The company was founded as Schmid Automation Asia, then went independent in 2014 and was renamed Symtek Automation Asia. (CD)

CIRCUITS ASSEMBLY Reopens SEA Registration

ATLANTA – CIRCUITS ASSEMBLY reopened registration for its annual Service Excellence Awards (SEAs) for EMS providers and electronics assembly equipment, material, service, and software suppliers. The 2022 program returns to its original format after a focus



group of past participants emphasized the value of the feedback they receive from their customers.

Now in its 30th year, the SEAs honor companies for excelling in the critical area of customer service, permitting participants to benchmark customer service against their peers. It is the only industry awards program that uses direct customer feedback to determine best-in-class.

Customers are surveyed to determine their satisfaction with a participating company in various categories, including dependability/timely delivery; manufacturing quality; responsiveness to requests and changes; technology; and value for the price. For the first time this year, participants will be rated on flexibility/ease of doing business.

Also in 2022 is a new award category: the overall best-in-show winner.

All customer responses and ratings are tabulated and provided in a confidential



An Open Letter to our many Friends, Colleagues, Customers, and Partners

Rarely do so many landmark events happen at once.

In this case, we at Uyemura are celebrating our best year, extraordinary success in a new market that has seemingly limitless potential, and an important evolution in our Senior Leadership Team.

Personally, I have taken a new role, with a 3-year agreement that allows me to focus exclusively on primary accounts, and manage international relations. This was an important element of the company's 5-year plan. For me, as founder and President of Uyemura USA, it is a long-anticipated opportunity to work intensely in two arenas where my 33 years with this extraordinary company can best serve its long-term goals – and mine.

Taking the role of President and CEO is Mark Eonta. This is a well-deserved appointment on what is his 10th anniversary of service to Uyemura. Most recently, Mark was our Vice President, Sales.

I expect Mark's technical skills and sales experience to be central to our success in adapting processes to solve customer issues, and to energizing our many strategic partnerships.

My agreement began this month, with potential re-negotiation in 2025. I will continue work from my office at corporate headquarters in California. Mr. Eonta will work between headquarters and our Technology Center in Connecticut.

The success of our development efforts promises to make the next two years, in particular, truly transformational for Uyemura. I look forward as always, to your thoughts, your counsel - and your friendship.



General Motors aims to tackle the global semiconductor shortage with new designs built in North America, president Mark Reuss said.

Isola announced its I-Tera MT40 circuit materials support multilayer PCBs for military- and commercial-grade low-Earthorbit (LEO) satellites.

OnlineComponents.com, an authorized e-commerce distributor of electronic components, has joined the Nexar ecosystem of companies that provide solutions needed to help design, source, and manufacture a PCB.

Schweizer Electronic has founded a sales division in the US and named Robert Davenport to head sales.

Sunstone Circuits was named as one of the Healthiest Employers of Oregon for the ninth consecutive year.

Taiflex Scientific disclosed plans to invest more than \$70 million to expand flexible copper-clad laminate production capacities at its plants in China and Taiwan over the next two years.

TRS Capital has acquired a majority stake in Alta Electronics, a supplier of interconnect products headquartered in Canada.

Ultra Librarian has teamed with Nexar, a business unit of Altium, to offer CAD libraries via the Octopart search engine.

The US Department of Defense is issuing Al ethics guidelines for tech contractors.

Zuken seeks abstracts for its annual user conference to be held in San Antonio in June.

Zuken and SnapEDA announced a new capability that provides eCADStar users with direct access to SnapEDA's online library.

Zuken released SAP Engineering Control Center interface, enabling the integration of its CR-8000/DS-CR and E3.series/DS-E3 engineering systems into SAP S/4HANA, SAP's ERP system.

CA People



Indium promoted Cristian Tudor (top left), to senior applications engineer, and Angelo Marques has been appointed design for excellence (DfX) specialist in Europe. Tudor joined Indium as an applications engineer in 2000 and is based in Romania. Margues has over 25 years' automotive electronics experience in new product introduction and process optimi-

zation.

report to the participating company.

The SEAs recognize four categories of EMS providers based on revenues (under \$20 million; \$20 million to \$100 million; \$101 million to \$500 million, and over \$500 million).

Equipment, material or software supplier awards will be presented in each of the following categories: component storage systems; automation and handling equipment; cleaning processing or materials; device programming equipment; dispensing; pick-and-place; repair and rework; screen printing; test and inspection; materials (solder, encapsulants and adhesives); soldering equipment; automation/manufacturing software (not ERP/MRP); and supply-chain/ERP/MRP software.

Non-manufacturing service providers will be honored in the following categories: test laboratories; recycling, cleaning or other non-manufacturing process providers; and design service bureaus. Reps or agents and/or distributors will also be honored.

CIRCUITS ASSEMBLY will honor winners in-person on the show floor at SMTA International on Nov. 2, 2022, at the Minneapolis Convention Center in Minneapolis, MN. Awards and reports will be distributed there. Participants will also receive their report as an Excel file after the show.

"Datest offers testing, engineering, analytical, and other value-added services, all geared to speed, flexibility, and results. We need a mechanism for obtaining meaningful feedback from customers on a regular basis. We also share that feedback with our AS9100 auditor. The CIRCUITS ASSEMBLY Service Excellence Awards are ideal for capturing those honest reactions that make us a better company," said Robert Boguski, president, Datest.

For more information, visit https://circuitsassembly.com/ca/editorial/serviceexcellence-award.html.

The deadline to enter is Apr. 5. To register, visit https://na.eventscloud. com/2022sea. (CD)

Elin Electronics Files for IPO

DELHI - Electronics manufacturer Elin Electronics has filed for an initial public offering. The company's IPO comprises equity shares of face value of Rs 5 (US\$0.067) each, comprising a fresh issue aggregating up to Rs 1.75 billion, and an offer for sale of up to Rs 5.85 billion.

Currently, eight individual promoters hold 38.69% and other selling shareholders own 52.51% stake in the company.

Proceeds from the fresh issue will be used to the extent of Rs 800 million to repay/ prepay debt and Rs 489.7 million for funding capital expenditure for upgrading and expanding existing plants.

Revenues from operations increased 9.8% year-over-year to Rs 8.6 billion in fiscal 2021 primarily due to increased consumer purchases of home and personal appliances aided by the relaxation of Covid-19-led restrictions. Net profit grew 26.8% to Rs 348.6 million for fiscal 2021. (CD)

IPC: Material and Labor Costs Remain Large **Issues for Electronics Supply Chain**

BANNOCKBURN, IL - Material and labor costs continue to be two of the largest issues facing the electronics supply chain, according to an IPC report. Nine in ten electronics manufacturers report rising material costs, and nearly three-fourths report rising labor costs, the association says.

Ease of recruiting workers remains difficult, with 57% reporting it has gotten worse in the last month. Seventy-two percent of North American firms report ease of recruiting workers is declining, while 37% of firms in APAC and 43% of those operating globally report the same.

Conversely, 35% of firms operating globally report ease of recruiting workers



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Bright Machines announced cofounder and CEO Amar Hanspal is stepping down and cofounder Lior Susan has been appointed interim CEO.

Creation Technologies named Farid Anani vice president/general manager.



KIC promoted **Robert Baxter** to customer success manager.

Kimball Electronics appointed **Douglas Hass** chief compliance officer.



MicroCare named Ray Bellavance vice president, Global Sales & Marketing. He joins the company with nearly 30 years' experience selling industrial chemicals and tools, including

MicroCare products.

Virtex Enterprises appointed Michael Maloof business development manager - Medical Sector.

CA Briefs

The Air Force Research Laboratory has tasked NextFlex with finding ways to attract students who might not otherwise consider a technical or scientific career path.

Aurelius Technologies (ATech) expects to raise \$18 million from an IPO on the Malaysia exchange to fund expansion of its EMS business.

Bittele Electronics expanded its suppliers to include **Quest Components** and **TME**.

Bright Machines appointed **Fenwick Group** manufacturers' representative for customers in France.

China has quietly enacted a new set of laws – first the Data Security Law in September, followed in November by the Personal Information Protection Law – that go even further by demanding not just access to private data but also effective control over it.

Compal Electronics dismissed reports that claimed it was shutting down TV assembly lines in Taiwan.

Flex completed its previously announced \$540 million all-cash acquisition of Anord Mardix from private equity firm Bertram Capital.

Fluidra Australia has expanded its manufacturing and warehouse facility, and an electronics assembly area is under construction as part of the integration of Fabtronics, acquired last year.

Foxconn confirmed plans to make New Taipei a hub for its software research and development center. Foxconn also reportedly is working with Saudi Arabia to create is improving, whereas 6% of firms in North America and Europe report the same. Among firms in APAC, ease of recruitment is holding steady at 51%.

While order flow remains positive, higher costs are hurting profit margins, with 58% of electronics manufacturers reporting orders are expanding, says IPC. Forty percent report profit margins are declining, and 19% report profit margins are improving.

Eighty-two percent of manufacturers in North America indicate labor costs are rising vs. 59% among firms operating in APAC, where, along with European firms, labor costs are more likely to be holding steady, says IPC.

Ninety-eight percent of North American manufacturers indicate rising material costs compared to 90% in Europe, 88% in APAC, and 78% among global manufacturers.

Fifty-three percent of firms in North America report declining inventory available to customers, while 30% of firms in Europe, 29% of firms in APAC, and 26% of those operating globally are currently experiencing declines.

At the same time, 30% of European manufacturers indicate inventory available to customers is rising, with the diffusion index in Europe no longer indicating a state of contraction.

Two-thirds of manufacturers report their government is not invested in the electronics industry's success. Only 20% of North American manufacturers agree their government is invested in the success of the electronics manufacturing industry, compared to higher agreement among manufacturers in Europe (38%); APAC (57%); and those operating globally (57%).

Similarly, 13% of manufacturers in North America agree their government is adequately helping the EMS industry transition to the factory of the future, whereas 37% of firms in Europe, 41% of global firms, and 50% of firms in APAC feel the same.

Fifty-six percent of North American manufacturers expect backlogs to rise in the next six months, compared to 28% among firms in Europe, where 60% of firms expect backlogs to remain flat.

Thirty percent of global manufacturers and 21% of manufacturers in APAC expect ease of recruiting to rise in the next six months, while 9% of manufacturers in North America and 4% of manufacturers in Europe anticipate the same.

Eighty percent of North American firms anticipate rising labor costs in the next six months, compared to 55% among firms in Europe, where 41% are expecting labor costs to remain flat.

Fifty-seven percent of global manufacturers, along with 55% of APAC manufacturers, expect capacity utilization to rise in the next six months, compared to 30% among firms in North America.

Eighty-eight percent of North American manufacturers expect material costs to rise in the near future, compared to 67% in Europe. European firms are more likely to indicate material costs will remain stable (31%), while firms in APAC are more likely to anticipate further decline (7%).

Thirty-six percent of North American manufacturers expect inventory available to customers to decline, while 13% of firms in Europe anticipate the same. (CD)

Latécoère to Acquire EMS Firm Malaga

TOULOUSE, FRANCE – Latécoère has entered into a definitive agreement to acquire electronics manufacturer Malaga Aerospace, Defense & Electronics Systems for an undisclosed sum. Malaga provides PCBs for high-reliability applications across defense (~80% of sales), commercial aviation and industrial end markets (~20% of sales). The firm employs 100 staff in Spain.

Latécoère provides electrical wiring interconnection systems.

Thierry Mootz, CEO, Latécoère, said in a press release: "MADES is a marketleading company with effective management and first quartile operational and customer performance. Following the acquisitions of SDM in Mexico and TAC in Belgium, this is the third acquisition since the capital increase completed in August.

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a joint venture responsible for building EVs, possibly involving BMW.

Foxconn Interconnect Technology has invested \$10 million in Autotalks, an Israel-based V2X (Vehicle-to-Everything) communication solutions provider.

Google Quantum AI researchers and their colleagues reveal they have created time crystals using Google's Sycamore quantum computing hardware.

Hyundai and **Kia** have selected **Siemens** as strategic partner for engineering and product data management through NX software and the Teamcenter portfolio.

Interconnect Solutions completed the acquisition of cable assembly and wire harness company **Tri-Tek Electronics**.

Kitron shut down production Dec. 7 in Zhenhai after authorities imposed a district-wide lockdown because of a Covid-19 outbreak.

LeeMAH Electronics installed a **Juki** G-Titan screen printer.

NeuronicWorks is expanding its operations to offer fully integrated, turnkey, custom box assembly services, in addition to the firm's design, engineering and prototyping services.

OSM Group opened a production facility for consumer electronics and industrial products in the Philippines.

Precision Graphics will invest \$5.1 million in a new electronics manufacturing plant in Snow Hill, NC.

Qualcomm expects chip sales to **Apple** to dwindle to a trickle in the coming years but predicted brisk growth in chips for autonomous cars.

Rakon India is among those investing in new electronics manufacturing facilities in Karnataka.

Scope Industries said it will divest its oil palm plantation to focus solely on its electronics manufacturing services business, according to reports.

Specialty Coating Systems acquired **Comelec**, provider of Parylene, atomic layer deposition and multilayer coating services, for an undisclosed sum.

Stellantis expects major revenue gains in part due to new interfaces for next-generation vehicles developed in collaboration with **Foxconn**.

SVI Public Co. finalized its acquisition of a 100% stake of **Tohuku Pioneer (Thailand)** for an undisclosed sum on Nov. 30.

EMS company **Syrma SGS Technology** filed for an IPO in India.

MADES is developing our position in the US defense market segment and will create significant synergies within Latécoère's interconnection systems division, as well as reinforcing our number one position for avionic racks.

Closing is subject to a number of commercial and regulatory conditions, including approval by the Spanish Council of Ministers. (CD)

Lacroix Gains Majority of Firstronic

GRAND RAPIDS, **MI** – Lacroix has signed an exclusive agreement for the acquisition of a majority stake in EMS firm Firstronic. The group's equity stake, first acquired in 2017, will increase to 62% from 12.5%.

Concurrently, private equity firm Bpifrance will take a 26% stake. John Sammut will remain CEO of Firstronic and will retain 4% of share capital, while COO Jochen Lipp will take an equity stake in Firstronic of 3%.

"We have had a stake in Firstronic for almost four years, during which time we have been able to observe the commitment and know-how of Firstronic's teams and the strong potential synergies between our respective entities," said Vincent Bedouin, CEO, Lacroix. "Together with keeping in place a highly experienced management team, which has been able to grow the business at a rapid pace, these elements convinced us that a combination would be mutually beneficial and incorporating Firstronic largely facilitated."

Firstronic serves tier-one customers primarily in the automotive, industry and healthcare sectors in North America. The company has production sites in Michigan and Mexico and 1,300 staff.

In 2020, Firstronic posted revenue of \$87 million, almost 20% of Lacroix's revenue. Strong growth is expected across both indicators for the 2021 financial year, with a trajectory of \$140 million in revenue and EBITDA above 9%. The deal should immediately prove accretive within the upcoming financial year. (CD)

Delta Electronics to Acquire Universal Instruments for \$89M

TAIPEI – A subsidiary of Delta Electronics will acquire Universal Instruments for \$88.9 million, Delta announced on Dec. 18. The transaction is subject to certain closing conditions, and is expected to generate substantial synergies through the companies' respective R&D operations and global customer base.

Universal Instruments is a North America-based OEM of electronics placement equipment. Delta Electronics, founded in 1971, is an OEM of switching power supplies and thermal management products. Following the aforementioned transaction, Universal Instruments will continue operating under its original management team.

"By adding Universal's precision automation machine offering and leading technologies to our highly diversified industrial automation portfolio, we can offer customers total solutions capable of enhancing the productivity and carbon footprint of their production lines," said Ping Cheng, chief executive, Delta Electronics.

Conklin, NY-based Universal Instruments has more than 500 patents and close to 30,000 systems delivered. The deal includes Universal Instruments' Advanced Process Lab (APL), which assists customers in each phase of the products' lifecycle (prototyping, process development, analytics, and advanced assembly). (MB)

Thurlby Thandar Instruments, a UKbased electronic testing instrument manufacturer, named **TestEquity** authorized distributor in North America. Vitrox named EMC3 Group sales channel partner in Florida.

VVDN Technologies has begun ODM work on tablet PCs for Indian and global OEMs.



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EVERYONE NEEDS STORAGE				
Trends in the US electronics equipment market (shipments only)	AUG.	% CH/ SEP.	ANGE Oct.	YTD%
Computers and electronics products	0.3	0.6	-0.2	6.1
Computers	-1.4	-4.3	0.9	2.2
Storage devices	-1.6	0.1	-2.4	31.0
Other peripheral equipment	-1.7	2.6	-0.6	4.8
Nondefense communications equipment	0.7	-0.1	0.2	7.7
Defense communications equipment	-2.5	1.7	2.1	3.9
A/V equipment	-1.8	10.0	-3.3	-1.6
Components ¹	1.0	3.3	1.0	6.3
Nondefense search and navigation equipment	-0.7	-0.1	0.7	2.7
Defense search and navigation equipment	-0.6	-0.8	0.3	2.6
Medical, measurement and control	1.2	-0.2	-0.1	6.4
'Revised. *Preliminary. ¹ Includes semiconductors. Seasonally adjus Source: U.S. Department of Commerce Census Bureau. Dec. 3, 202	ted. 1			

US MANUFACTURING IN	IDICES				
	JUL.	AUG.	SEP.	OCT.	NOV.
PMI	59.5	59.9	61.1	60.8	61.1
New orders	64.9	66.7	66.7	59.8	61.5
Production	58.4	60.0	59.4	59.3	61.5
Inventories	48.9	54.2	55.6	57.0	56.8
Customer inventories	25.0	30.2	31.7	31.7	25.1
Backlogs	65.0	68.2	64.8	63.6	61.9
Source: Institute for Supply Management, Dec. 1, 2021					

KEY COMPONENTS						
	JUN.	JUL.	AUG.	SEP.	OCT.	
Semiconductor equipment billings ¹	59.2%	49.8%	37.8%	35.5% ^r	41.3% ^p	
Semiconductors ²	29.2%	29.6%	30.0%	27.6% ^r	24% ^p	
PCBs ³ (North America)	1.15	1.29	1.48	1.25	1.15	
Computers/electronic products ⁴	5.26	5.27	5.26	5.27 ^r	5.28 ^p	
Sources: ¹ SEMI, ² SIA (3-month moving average growth), ³ IPC, ⁴ Census Bureau, ^p preliminary, ^r revised						

Semi Equipment Sales to Top \$100B for 1st Time

TOKYO – Global sales of semiconductor manufacturing equipment by original equipment manufacturers were expected to reach a new high of \$103 billion in 2021, surging 44.7% from the previous industry record of \$71 billion in 2020, SEMI said in mid December.

The market is expected to further expand to \$114 billion by 2022.

"Crossing the \$100 billion mark reflects the global semiconductor industry's concerted and exceptional drive to expand capacity to meet strong demand," said Ajit Manocha, president and CEO, SEMI. "We expect continuing investments in the digital infrastructure buildout and secular trends across multiple end markets to fuel healthy growth in 2022."

Wafer fab equipment segment sales are expected to grow 12.4% in 2022 to about \$99 billion.

Hot Takes

- Semiconductor sales are finishing 2021 up more than 20% at \$550 billion after growing 10.8% to \$464 billion in 2020. (SEMI)
- The electronic component sales sentiment index for November was down 8.3 points sequentially to 111, and is expected to fall below 100 in December for the first time in 18 months. An index below 100 suggests a contracting market. (ECIA)
- More Wi-Fi 6 devices will ship in 2022 than 5G devices, to the tune of at least 2.5 billion Wi-Fi 6 devices versus roughly 1.5 billion 5G devices. (Deloitte)
- Global AR/VR device shipments in 2022 will reach 12.02 million units, up 26% year-over-year, with Oculus and Microsoft the leaders in the consumer and commercial markets, respectively. (TrendForce)
- Inventory-to-sales for new vehicles in the US is 0.389, which means the auto sector can only cover 12 days of sales with current inventory levels. (IPC)
- Recruiting workers remains difficult, with 57% of companies reporting it has gotten worse in the last month. Seventy-two percent of North American firms report ease of recruiting workers is declining, while 37% of firms in APAC and 43% of those operating globally report the same. (IPC)
- Some 58% of electronics manufacturers report orders are expanding, while 40% report declining profit margins, and 19% report improving margins. (IPC)
- Ninety-eight percent of North American manufacturers indicate rising material costs compared to 90% in Europe, 88% in APAC, and 78% among global manufacturers. (IPC)
- Global shipments of traditional PCs are forecast to reach 344.7 million units in 2021, up 14%. (IDC)
- The gaming console market will generate \$81 billion in 2022, up 10% from 2021. (Deloitte)
- Global shipments for wearables grew 9.9% during the third quarter, reaching 138.4 million units. (IDC)
- The 90-day moving average sales at North American EMS companies fell 4.4% year-over-year in October. Shipments fell 0.8% sequentially. October orders rose 40% year-over-year and 22% from the previous month. (IPC)
- **IT spending in India** is forecast to total \$101.8 billion in 2022, an increase of 7% from 2021. (Gartner)
- By 2025, 30% of critical infrastructure organizations will experience a security breach that will result in the halting of an operations- or mission-critical cyber-physical system. (Gartner)
- IC growth will climb 11% in 2022, following a 26% jump in 2021. (IC Insights)
- The worldwide market for smart home devices grew 10.3% year-over-year in the third quarter of 2021, with more than 221.8 million device shipments. (IDC)
- The global flexible electronics market is projected to reach \$61 billion by 2030, expanding at a CAGR of 8.5% from 2021 to 2030. (Precedence)

Strained Communication

Working unconventional hours in remote locations disrupts business more than material shortages.

AS WE ENTER the third year of our pandemic-altered world, more chains are strained than just supplies. With people working remotely during odd hours, changing careers, or stepping out of the workforce altogether to care for loved ones, the basic chain becoming strained is communication.

Communication has been transitioning over the past couple decades. Time, culture and technology have dramatically transformed. Long gone are the storied two-martini business lunches where colleagues, customers and suppliers met, broke bread and discussed one-on-one issues that needed ironing out. Over the past decades, face time (not FaceTime) with any business client has become extremely difficult to arrange. Today with Covid, meeting face to face is all but impossible for many. Long-changing trends compounded by recent events have had a negative impact on the ability to communicate effectively, which in turn has strained the quality of relationships in too many cases.

For years, a typical customer service or salesperson would spend so much time on the phone with clients, they were jokingly referred to as having "cauliflower ear." The ongoing constant chatter between people – most business, but some social – helped build strong relationships. How times have changed. The phonesavvy businessperson and bonding over long lunches are no more. Over the past two decades, email has become the communication vehicle of choice. And the pandemic scattered employees, customers, suppliers – everyone – to remote offices, usually in their homes, hopefully with a quiet room from which to log on to Zoom, GoToMeeting and WebEx.

But with all these advancements in communication methodology, communication itself is collapsing. People working unconventional hours in remote locations don't communicate as often, nor to as many people, as they did when reporting to work in a shared workspace: the office. Colleagues aren't together. New employees have in some cases worked for a year or more without seeing their peers. What impact does strained communication have on building or maintaining relationships? Plenty! In our contemporary, highly digital, pandemic-impacted world, the word "relationship" doesn't mean what it used to, in part because we are not communicating like we used to.

As communication becomes less frequent and consistent, so do the understanding and commitment between person and person, company and company. All business is basically an interpersonal relationship. As people drift apart, or are no longer able to bond in the first place, mutual understanding, commitment and trust all too often fall by the wayside. This is less of a problem when all is well, but during a multiyear pandemic that has globally impacted all aspects of business and life, it safe to assume many, if not most, activities we are used to are not going well.

Problems crop up, and that's when the value of proactive communication - true relationships - is fully realized - or sorely missed. Especially in our current world, when problems crop up, by not having consistent, proactive, clear communication with employees, suppliers and customers, relationships among those parties become strained. When strains begin, the result becomes a de facto confirmation there is no relationship. When relationships become too strained, shortsighted misunderstanding leads to decisions to cut bait with the supplier, customer or employee and move on. In almost all cases, that is exactly what you should not want to happen. Cutting bait and replacing relationships with new, untried ones because no one took the effort to effectively communicate is a proven recipe for failure.

Everyone has customers or suppliers with problems – some self-inflicted, some accidental. In every case, what is needed to quickly and effectively resolve those problems is the ability to rely on crisp, effective communication with a reliable and understanding supplier, customer or employee relationship. Relationships demand enduring, proactive communication that flows both ways. Communication is the catalyst that enables relationships to develop and flourish, and lack of communication can begin the downward spiral that ends relationships.

This is why it is essential for management to be acutely aware of how communications are taking place in all areas of the business, especially now when so much of the workforce has been displaced to work remotely, or with new employees joining the organization who may not have been appropriately onboarded with the expectations of how and how frequent their communication efforts should occur.

Relationship means mutual respect, taking the good with the bad and rewarding a job well done, while also, in a nonpunitive way, communicating when pricing or service needs to be addressed. If we do not reground ourselves on communicating with our customers, suppliers, employees and employers during

continued on pg. 19

PETER BIGELOW is president and CEO of IMI Inc.; pbigelow@imipcb. com. His column appears monthly.



Supply Chain Pressures in 2022

How prepared is your organization?

HERE WE ARE in January 2022 with a future fraught with more uncertainties than any other during my six decades in the PCB, IC fabrication and assembly industries.

Business is strong despite shortages in labor and parts. Prices are rising, dramatically in some cases. Profits are being squeezed. Rapid government changes in travel restrictions and worker conditions seem endless due to the continuing evolution of the pandemic.

Supply chains are under pressure from a variety of events and circumstances. These include some brief power shutdowns at plants that produce wafers and PCBs in China, chip and other component shortages, shipping issues with a backlog of over 100 cargo ships carrying, for example, container loads of copper-clad laminates anchored off the Southern California coast waiting to be unloaded. The battery industry is gobbling up copper supplies. Major consumers are buying into chipmakers who can guarantee their needs. This affects those who cannot, causing them to scramble for new sources.

Not only are ICs in short supply, especially for automotive needs with the increase in the manufacture of EVs and hybrids, but substrates are needed for their mounting and connection to the outside world. As a result, major automotive companies in Japan, the US, and Europe have curtailed production in several factories to the tune of several million vehicles in the coming year.

We have seen some companies redesign the printed circuits to accommodate available chips when the delivery of the ones originally ordered became uncertain.

Because not every application needs the latest and greatest chips with <10 or 12nm nodes, a scramble is on to expand production of chips with less stringent specifications, including larger feature sizes. This has created a demand for and a shortage of refurbished "older" equipment.

A new focus is on semi-additive and additive circuit manufacturing. New technologies in these fields are gaining attention and some traction in the US, while others across the Atlantic are in the advanced development and field test stage. These will require new standards and design skills. There are also major advances in the use of AI and XR for equipment design and system use, as well as support services.

Another emerging technology on the horizon reduces energy consumption by 80% or more in some electronics assembly (and other) applications with the use of photonics to replace IR or laser heating of parts for soldering, disc separation, and resin curing (e.g., protective coatings or solder masks), while providing reduced factory footprints. This technology will be demonstrated live at IPC Apex Expo 2022.

The aforementioned creates the need for not only locating and training new workers, but also upskilling existing employees. Private companies and trade associations around the world alike are putting a major effort into this. Some are focusing on individuals, like PCEA and SMTA, others such as the MittelStands Campus are focused on midsize companies. These groups are becoming more affiliated with each other.

All this brings to mind these questions:

- Did you check the security of your supply chain when you made your business forecasts for the year?
- How prepared are you for rapid changes?
- What contingency plans have you made?
- What relationships do you need to build or solidify? With customers, suppliers and/or employees?
- What new cooperative activities do you plan to initiate?
- Are there competitors with whom you can cooperate?
- How strong is your relationship with all your suppliers?
- Do you have alternate sources for key needs?
- Can any of your customers provide the parts you need to assemble their boards or make their electronic packages?
- Can you reach out to the OEM that will be the final customer for support in meeting their present and future needs?
- What are you doing to upskill your employees?
- Is there a need or opportunity for shared resources?
- How will you evaluate new products/processes?
- How can you offset shrinking margins?
- Is there a possibility of cooperative buying to strengthen your purchasing power?

More questions will arise as new challenges and opportunities occur.

Meanwhile, as we look around the world, we learn Meiko Electronics will build a new major PCB production and R&D facility in the newly completed Yamaguchi Industrial Park in Northern Japan.

Japan appears to be aggressively active in reshoring and solving some of its supply chain woes by subsidizing half of TSMC's \$8.8 billion planned fab there. Ford is one of the recent automotive companies to take direct action to secure its future IC supply chain. It has a new agreement with Global Foundries. Did you

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know today's cars now use up to 1,000 or more chips?

The PRC (China) will start the construction of eight new chip fabs in 2022. Don't expect this to be any help to those in the Americas. It's interesting to note, even though TSMC has a major effort in Arizona, its chairman Morris Chang said, "It would not be a possible task to rebuild semiconductor supply chains in the US due to high costs." Is that a challenge? Or even true?

Some new help is on the way, especially for individuals and smaller companies with limited budgets. Effective this month, the Printed Circuit Engineering Association (PCEA) is acquiring staff and assets of an organization with over 2.5 million annual engagements with printed circuit engineers, designers, fabricators and assemblers around the world. The acquisition includes two industry-specific trade shows (PCB West and PCB East), the PCB2Day workshops, Printed Circuit University, the dedicated online training platform, and more. Current PCEA affiliations are said to include the EIPC (European Institute of Printed Circuits), the SMCBA (Surface Mount & Circuit Board Association), the FED (professional association for design, circuit board and electronics production), ECEDHA (Electrical & Computer Engineering Department Heads Association) and the SMTA (Surface Mount Technology Association). ROI, continued from pg. 17

a perpetual pandemic when they are most in need of support, ultimately the relationships built over many years will founder.

In a world where escalating levels of communication technology are available, and in a jolted world where demands on the supply chain to remain competitive are under severe constraints, isn't it now, more than ever, that we need to really understand what our customers, suppliers and employees need? If so, then we need to make sure we are committed to communicating in all ways possible, clearly, concisely and consistently, so relationships do not become further strained, and we all achieve mutual success.

Relationships have enabled our industry to grow, prosper and survive. Face-to-face communication, phone calls, emails and virtual meetings are essential now more than ever to propel our individual businesses and the entire industry to even greater success in the future. \Box

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THE STARK CHOICES of organisms are to adapt, move or die. Our electronics sometimes tough it out so we can do our jobs or simply have a good romp on our favorite ride. No matter the purpose, extreme weather puts an electrical system to the test.

Whether the element is sand, saltwater, sunshine or perhaps a lack of thereof, many dangers age a system prematurely. Most faults caused by the environment are single-component failures. Okay, a part failed. Why? What is the root cause, and what can we do to prevent it from becoming part of a larger trend? Answering that two-part question is the gist of reliability engineering.

What broke is not always evident. Cosmetic damage or a burn scar may point the way if you're lucky. In most cases, diagnosis is not that easy. Check connectors first, while the board-level investigation usually centers around the FETs that bring power to the device that is out of spec or failing altogether. Somewhere in there a tiny junction has burned up. The repair and return unit or perhaps field service technicians are a good source of reliability anecdotes.

Shock and vibration over time will make anything rattle itself to pieces. We can run into unexpected issues with resonant frequencies. Remember the footage of the Tacoma Narrows Bridge. "Galloping Gertie" came down, as the roadway itself was wind-tossed into 30' waves. The same thing happens on a smaller scale and at higher frequencies all around us. Something will begin to rattle in the wind until it breaks off.

Spread out components to relieve heat buildup. What separates high-reliability PCB footprints from standard ones? You'll see the difference in the size of the solder pads. Expect more room for the toe fillet. This often increases the personal space around the component, while providing additional metal-to-air interface area for convective heat dissipation. The additional spacing created by the extra metal may not seem like much, but on aggregate has been shown to reduce junction temperatures.

Derating for system robustness. The other thing that separates high-reliability footprints is simple. Stuff them with components that are better than good enough. Twice as good is a high bar, and a good place to start when it comes to derating components. If a 50V cap is sufficient, go for the 100V version.

Chunky hardware with closer spacing isn't just for the steampunk effect. Plan a few mounting holes in the middle of the board, rather than just the corners. You've seen a heat map. The hot spot isn't on the edges. As a practical matter, a gratuitous hole here or there could be a bargaining chip as the board evolves into something more crowded than originally planned. You know what they say about plans.

Commercial- versus industrial-grade components. It was easy to distinguish the TTL packages of yesteryear. The high-reliability units had a device number "54," rather than the "74" used on commercial versions (**FIGURE 3**). LS stands for low-power Schottky, which predates the even lower-power CMOS architecture. This example is a stand-in for the universe of components that follow this technology path.

JR. is a career PCB designer experienced in military, telecom, consumer hardware and, lately, the automotive industry. Originally, he was an RF specialist but is compelled to flip the bit now and then to fill the need for highspeed digital design. He enjoys playing bass and racing bikes when he's not writing about or performing PCB layout. His column is produced by Cadence Design Systems and runs monthly

JOHN BURKHERT





FIGURE 1. While this overnight accumulation looks tame to some, moisture is an archenemy of electronics (and other metal objects).



FIGURE 2. The car suffers in the midday sun, and I come along and demand it envelop me in a cocoon of frigid air. Like it or not, that's hard on the equipment.

Operating ambient temperature range and package comparison: 54 = -55°C min., 125°C max. Packages: CDIP, LCCC, CFP 74 = 0°C min., 70°C max. Packages: PDIP, SOIC

Ceramic packages withstand a greater range of temperatures than plastic ones. No surprise high-reliability packages are not always the smallest available. It's a paradigm that carries through connectors down to passives. Get those commits early and nurture them so the part pipeline is there when you need it. Mil-spec parts are an upgrade whether the board is Class 3 or Class II commercial, so it's about cost and availability.

Use adhesives and conformal coatings to prevent unintentional disassembly. For everything to stay put, a shaker table will be part of your life. These instruments of mechanical terror are specially designed to shake other smaller things to the point of failure. You can only imagine how overbuilt a shaker table must be to outlast whatever is bolted down on its base plate.

When the dust settles, the weakest link(s) will be revealed, and additional actions can be taken. During the preproduction trials on the Pixel laptop, we had a connector that would not stay put after the 3' drop test. We hope you never give your laptop a 3' drop onto concrete, but if you do, a little bracket holds the USB connector in place.

Riding around on the roof of a car is another challenge you should never have to face. Putting a Lidar detector up there, on the other hand, can be loads of fun (FIGURE 4). Simultaneous location and mapping (with the somewhat unfortunate acronym SLAM) require an immense amount of processing while jostling around through rain and sleet. The connectors, in particular, are well overbuilt, especially when you're looking for a place to put that ethernet port. Nonetheless, a bead of glue around the base is an insurance policy. Post-assembly coatings make rework next to impossible but also protect the devices from failure, making it a good idea for space-bound projects. Use heavier copper to give the boards some backbone. Not sure if anyone besides those in the PCB industry use copper weight as the significant variable to determine its thickness, but here we are. Take 1 oz. of copper, keeping in mind it is very malleable, and shape it into a 1' square of even thickness. That's 1 oz. copper and typically about as much as would be used for the outer layers, while the innerlayers typically get half that.

Both inner- and outer layers can be plated up. One result of this is an increase in the minimum trace width and spacing geometry. The thicker the copper, the coarser the line-to-line pitch becomes. At the extreme, an entire base plate of copper with no circuit pattern can be incorporated into a board. That could be a solid copper bottom layer or as a central metal core. For a local effect, a so-called coin can be embedded as an integral heat sink.

Shock mount electronics inside a cage within a cage. Flight cases offer a standard 19" equipment rack-mount isolated from a secondary outer case that ensures the contents are not subjected to sudden g-forces from being loaded and transported. Something is better than nothing when it comes to bolstering the unit against the expected use-case.

Depending on where you want to go and what you want to do, your electronics must be hardened against failure. We are often the cause. Who hasn't dropped their phone? The reliability lab focuses on finding root causes of failure. Take whatever measures are necessary and prudent for the perils the gear is likely to face.

Sometimes, reparability will suffer for the effort of making it bulletproof. The motivation is to reduce or eliminate repairs in the first place. Fail fast and go to mass production with the most solid product you can put out there. Your customers will then put it to the test so you can continue the cycle of continuous improvement.



FIGURE 3. This hex inverter circuit plays out on different footprints, starting with DIP packages, and then SOIC became the surface mount version for the plastic package. The underlying silicon underwent several iterations, and the high-reliability versions are on their own package outlines. (Source: Netsonic)



FIGURE 4. A car roof is a good place to be out in the elements. Any outdoor location will do, while motion will amplify the effects.



Printed Circuit Engineering Professional

The comprehensive curriculum specifically for the layout of printed circuit boards

The Printed Circuit Engineering Professional curriculum teaches a knowledge base and develops a competency for the profession of printed circuit engineering layout, based on current technology trends. It also provides ongoing reference material for continued development in the profession. The 40-hour course was developed by leading experts in printed circuit design with a combined 250 years of industry experience and covers approximately 67 major topics under the following headings: Basics of the profession, materials, manufacturing methods and processes; circuit definition and capture; board layout data and placement; circuit routing and interconnection; signal-integrity and EMI applications; flex PCBs; documentation and manufacturing preparation; and advanced electronics (energy movement in circuits, transmission lines, etc.). Class flow: Books sent to students prior to an instructor lead review. This is followed by an optional exam with a lifetime certification that is recognized by the PCEA Trade Association.

The course references general CAD tool practices and is vendor-agnostic. The instructor, Mike Creeden, CID+, has 44 years of industry experience as an educator, PCB designer, applications engineer and business owner. As Technical Director of Design Education at Insulectro, he helps OEMs and fabricators achieve design success for best material utilization. He has served as a Master Instructor for the CID+ IPC Designer Certification program, was a primary contributor to the CID+ curriculum, and founded San Diego PCB Design, a nationally recognized design service bureau.

For Information or Registration: www.linkedin.com/company/pce-edu/

Upcoming Class Openings: More added each month! February 7-11 March 7-11



AUTHORS



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Printed Circuit Engineering Professional

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The Billion-Dollar MISTAKE

Stop designing products guaranteed to fail EMC testing. by DANIEL BEEKER

Au: This article emphasizes the need to concentrate on design of transmission lines, or the "spaces," instead of the "wires." The industry focus has been on the movement of charges in the wires, which only occurs because the electric fields are moving. The energy is carried by the fields, not the displacement current. My apologies to the EM physicists for oversimplifying these concepts, but this approach will increase the chances of success for most designs.

Engineering teams worldwide are facing increasingly difficult challenges to design electronic products and achieve good signal integrity and compliance. However, the status quo is to expect the design to fail EMC testing not once, but three, four, or as many as five times. Each time the design is sent to be retested, there is little confidence in success. This cycle is expensive in both the time it takes to redesign the product and the cost of expediting fabricating the new PCB and assembly. Add this to the cost of retesting the product, and the numbers add up very quickly. This expense and delay in product certification are not in the budget or the schedule. The cost not only directly affects the bottom line of the electronic supply company, but also affects the customers waiting for the product. Instead of designing the next big thing, teams are trying to fix the current one. As a result, billions of dollars are lost each year designing products that are expected to fail.

What is wrong here? The billion-dollar mistake.



FIGURE 1. Is this how current really flows?

The billion-dollar mistake is rooted in the misunderstanding of the nature of electronic energy. One drawing is to blame.

FIGURE 1 shows a battery connected by wires to a light bulb. The arrows are supposed to show current flow. From this, the wires started to be called "conductors," since the energy flowed in the wires. The current flowed in a loop, so the idea this was a circuit was born. If this were true, then as soon as the switch was closed, the energy would be instantly seen at the load, and there would be no such things as signal integrity or EMC problems. There would also be no such thing as radio because the energy is the same in an electrical system or air. There would also not be any life on earth, as light from the sun would not travel here without the wires.

The perspective from this simple drawing has set the tone and philosophy for PCB design. The focus has been on current flowing in the conductor. The result has been a steady increase in failure to pass EMC requirements as the IC geometries grew smaller and switching frequencies increased.

Why did this happen? Recall the scenario of a frog in a pan of water. As the water temperature rises, the frog does not notice until it is too late. The electronics industry behaves much the same way, to its detriment. This incorrect perspective now costs the industry billions of dollars every year.

Ralph Morrison taught me the importance of language. In this case, incorrect language set the stage for bad design practices. It became the norm to design the conductors, connecting the battery or power source to the load. As long as the speed of the switch was relatively slow, this appeared to be the correct path. For earlier devices, this perspective was not so bad that it caused failures, but it has led to the creation of design rules that make it increasingly difficult to pass certification.

The Real Picture

The wires are not the primary energy conductors; they form boundaries, much like the banks of a stream. The main energy does not flow through the wires; it travels through the space between the wires. This space, or dielectric, is the primary conductor. The energy is carried by the moving EM fields in the dielectric, not electron flow in the wires. Proper perspective for current flow is the amount of field moving past a point in the transmission line.

Field stored in the left side does not move (FIGURE 2A). As



FIGURE 2A. Field behavior in four steps. Field stored in the left side does not move.



FIGURE 2B. As the switch starts to close, the field starts to move.



FIGURE 2C. The switch is closed, so the field moves into the new space.



FIGURE 2D. The switch is open, so the field stops moving from the left.

the switch starts to close, the field starts to move (FIGURE 2B). The switch is closed, so the field moves into the new space (FIGURE 2C). The switch is open, so the field stops moving from the left (FIGURE 2D).

Field behavior is simple to understand. When stored between two conductors, separated by a dielectric, the field stays put. Once the switch is closed, the field moves sequentially into the new space, like water moving into a hose from a faucet. Once the switch is opened, the field from the source stops moving because the two spaces are no longer connected. The field behavior after the switch is determined by what is at the other end of the space.

Simple rules of triplets can explain field control (FIGURE 3). You need three things to store field: two conductors separated by a dielectric. Electronic systems have only three types of components: conductors, dielectrics and switches. You can only do three things with electromagnetic field: store it, move it, or convert it into kinetic energy.

This misconception has led to design practices that almost guarantee failure. The cost to the industry is staggering. When a typical project fails EMC testing, it has to be redesigned, remanufactured and retested under pressure to get it done quickly. These redesign cycles usually involve minimal changes, and the results are often disappointing. The cost can range from tens of thousands to hundreds of thousands of dollars, and weeks to months of delay. There is typically no budget for either the funds or the time, and the impact on the business is huge.

Imagine this on a global scale: thousands of design teams spending time and money redesigning products instead of working on new ones, all because of a simple mistake in language.

To call this a billion-dollar mistake is an understatement.

DANIEL BEEKER is senior principal engineer, automotive field applications engineering, NXP Semiconductors (nxp.com); daniel.beeker@nxp.com.

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FIGURE 3. The rule of triplets.

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State-of-the-Art Technology Flashes

Updates in silicon and electronics technology.

Ed.: This is a special feature courtesy of Binghamton University.

Next-gen chips will be powered from below. As

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The INTEGRATED **ELECTRONICS** ENGINEERING **CENTER (IEEC)** at Binghamton University is a New York Center of Advanced Technology (CAT) responsible for the advancement of electronics packaging. Its mission is to provide research into electronics packaging to enhance our partners' products, improve reliability and understand why parts fail. Research thrusts are in 2.5/3-D packaging, automotive and harsh environments. bioelectronics flexible and additive electronics. materials for packaging and energy storage, MEMS, photonics, power electronics. sensors, embedded electronics, and thermal challenges in electronic packaging. More information is available at binghamton.edu/ieec.

transistors continue to be made thinner, the interconnects that supply them with current must be packed closer, which increases resistance and power. In processors, both signals and power reach the silicon from above. Arm researchers have developed a technology that separates those functions, saving power and making more room for signal routes. The signals travel along the copper traces of a PCB into a package that holds the SoC, through the solder balls that connect the chip to the package, and then via on-chip interconnects to the transistors. These interconnects are formed in layers called a stack. It can take a 10- to 20-layer stack to deliver power and data to the billions of transistors on today's chips. (*IEEC file #12450, IEEE Spectrum*, 9/2/21)



Using liquid metal to turn motion into electricity, even underwater. North Carolina State University researchers have created a soft, stretchable device that converts movement into electricity and works in dry and wet environments. The heart of this energy harvester is a liquid metal alloy of gallium and indium. The alloy is encased in a hydrogel with the water containing dissolved salts (ions). The ions assemble at the surface of the metal, which induces a charge in the metal. Increasing the area of the metal provides more surface to attract a charge. This generates electricity, which is captured by a wire attached to the device. Researchers found that deforming the device by only a few millimeters generates a power density of approximately 0.5 mW/m⁻², comparable to popular classes of energy harvesting technologies. (IEEC file #12449, Science Daily, 8/28/21)

Precision 2-D patterns could lead to next-gener-

ation electronics. Technical University of Denmark researchers have taken the art of patterning nanomaterials to the next level. This precise patterning of two-dimensional (2-D) materials offers a novel route to next-generation computation and storage, which can deliver better performance and much lower power consumption. One of the most significant recent discoveries within physics and material technology is 2-D materials such as graphene. Graphene is stronger, smoother, lighter and better at conducting heat and electricity than any other known material. But perhaps the most distinct feature of 2-D materials is their programmability. The properties of these materials can be dramatically changed by creating delicate patterns in them. (*IEEC file #12492, Materials Today, 9/24/21*)



Researchers develop woven lithium-ion batteries. Fudan University researchers have developed highperforming woven lithium-ion fiber batteries that can be woven into textiles and other materials. While such fiber batteries have been produced previously, it was thought that this type of battery internal resistance is too great to be used as a practical power source. The team showed the resistance of such fibers is not linear and instead follows a hyperbolic cotangent function relationship, meaning the internal resistance of such batteries levels off as battery length increases. The battery fibers have an energy density of 85.69WHr/kg, which is significantly higher than standard fiber batteries. The fibers are constructed by depositing lithium

teries. The fibers are constructed by depositing lithium manganate particles onto carbon nanotubes, separated from a silicone-coated carbon nanotube sheet via a gel electrolyte. (*IEEC file #12451, Electropages, 9/2/21*)

Add the speed of GaN to the thermal conductivity of diamond. Osaka City University researchers have bonded gallium nitride to a diamond substrate at room temperature and demonstrated the bond can withstand heat treatments of 1,000°C, making it ideal for the high-temperature fabrication process of GaN-based devices. Attempts have been made to create a GaN-on-diamond, using some form of transition or adhesion layer, but the additional layer interfered with thermal conductivity. High-temperature (500°C) direct wafer bonding was a possibility, but thermal mismatch cracked the bonded result. The answer was "surface-activated bonding" (SAB) atomically cleaning and activating the surfaces so they react when brought into contact with each other. This technique is a route to high-performance power semiconductors. *(IEEC file #12457, Electronics Week-ly, 9/9/21)*



New optical "transistor" to speed computation up to 1,000 times, at lowest switching energy possible. Skoltech and IBM researchers have created an extremely energy-efficient optical switch that could replace electronic transistors in a new generation of computers manipulating photons rather than electrons. In addition to direct power saving, the switch requires no cooling and is really fast. At 1 trillion operations per second, it is between 100 and 1,000 times faster than today's top-notch commercial transistors. The new switch conveniently works at room temperature and therefore circumvents all these problems. The switch could act as a component that links devices by shuttling data between them in the form of optical signals. It can also serve as an amplifier, boosting the intensity of an incoming laser beam by a factor of up to 23,000. (*IEEC file #12479, Semiconductor Digest, 9/22/21*)

In-situ diagnosis of solder joint failure by means of thermal resistance measurement. It is very important to develop a reliable method to detect cracks in solder joints. When a solder joint cracks, parts of the solder are replaced by air gaps, leading to an increase of the thermal resistance. As a result, the detection of the changes of the thermal resistance could give the information of crack ratio in the solder joint. Tokyo Institute of Technology researchers have developed a nondestructive and in-situ crack detection method based on the measurement of thermal resistance. This study indicates the thermal resistance from heat source to cooling plate of a sample will not only be affected by crack ratio but also the crack's relative location and the heat source. The relationship between thermal resistance and crack ratio of a given solder area is examined experimentally and numerically on FET samples with different solder areas. (IEEC file #12473, Microelectronics Reliability, 8/1/21)

Technology for downscaling transistors could advance semiconductor design. Purdue University researchers have developed "Cascade Field Effect Transistor" (CasFET) technology, which could help design transistors that are smaller, use less power and switch from on to off at smaller applied voltages. Hence, this could lead to better and more powerful central processing unit generations, which can compute more operations with less energy. The key aspect is the superlattice perpendicular to the transistor's transport direction, which permits switchable cascade states. CasFET does not require band-to-band tunneling, so designers are able to develop faster-switching and more energy-efficient transistors. (*IEEC file* #12472, *Semiconductor Digest*, 9/20/21)



Compact amplifier could revolutionize optical communication. Chalmers University researchers have developed a unique optical amplifier expected to revolutionize both space and fiber communication. The new amplifier offers high performance and is compact enough to integrate into a chip millimeters in size and does not generate excess noise. The new amplifiers offer a level of performance high enough that they can be placed more sparingly, making them a more cost-effective option. They work in a continuous wave (CW) operation rather than only a pulsed operation. The technology is useful in a range of applications, such as space communication and in fiberoptic cables. (*IEEC file #12475, Science Daily, 9/21/21*)

Higher signal processing possible by ultra-strong squeezing of light. Singapore University of Technology researchers have developed a temporal compression system that demonstrates the ability to squeeze light in time by a 11-fold compression of light in time could prompt a crucial paradigm for light generation in advanced metrology, imaging, and high-speed optical communications. The system permits an equivalent increase in the number of bits transmitted by light in a fiberoptic network. It provides orders-of-magnitudes smaller footprint than existing benchtop com used for generating short pulses in ultrafast optical signal processing. The two-stage design features a dispersive element and nonlinear component integrated on the same chip providing high compression. (*IEEC file #12477, Laser Focus World, 9/22/21*)



Market Trends

3-D nano-inks push industry boundaries. Michigan Technological University researchers have created a way to make a 3D-printable nanocomposite polymeric ink that uses carbon nanotubes (CNTs). This revolutionary ink could replace epoxies in additive manufacturing and is more versatile and efficient than casting. Adding low-dimensional nanomaterials such as CNTs, graphene, metal nanoparticles and quantum dots permits 3-D-printed materials to adapt to external stimuli, giving them features such as electrical and thermal conductance, magnetism, and electrochemical storage. What they have done differently is use polymer nanocomposites and a printing process that doesn't sacrifice functionality. *(IEEC file #12486, Science Daily, 9/24/21)*

Integrated electronics trends to drive IME market to \$1.5 billion by 2032. In-mold electronics (IME) enables electronic functionality to be embedded within molded and thermoformed plastic components. With the integration of capacitive touch, lighting, and even haptics, along with size and weight reductions of up to 70%, IME is an efficient approach to making curved touch-sensitive interfaces. IDTechEx forecasts IME to be a \$1.5 billion market by 2032, with applications mainly within the automotive and consumer sectors. Greater integration of electronics within 3D structures is an ever-increasing trend, representing a more sophisticated solution compared to the current approach of encasing rigid PCBs. IME facilitates this trend by enabling multiple integrated functionalities to be incorporated into components with thermoformed 3-D surfaces. (IEEC file #12484, Printed Electronics World, 9/22/21)

Holographic windscreen enables in-car head-up display. WayRay has developed an automotive heads-up augmented reality display that uses a large part of the windscreen, and positions virtual objects at different apparent distances. It turns the entire windshield into a virtual world where information about the vehicle, navigation, infotainment, and the surroundings can be shown while blending with the real world. Its red-green-blue lasers are mounted remotely and connected by optical fiber to a "picture-generating unit" from which light travels in free space to the windscreen. Inside the windscreen are functional layers including a holographic polymer film. The concept is to display different types of information at different apparent depths, from dashboard-type data in the near-field, to the vehicle's ADASproposed travel path stretching into the far distance, highlighting real objects of interest seen through the windscreen. (*IEEC file* #12461, *Electronics Weekly*, 9/7/21)



Solar cells with 30-year lifetimes for power-generating windows. University of Michigan researchers have developed a transparency-friendly solar cell design that could marry high efficiencies with 30-year estimated lifetimes, which may pave the way for windows that also provide solar power. These devices, used on windows, turn a building into a power plant. While silicon remains king for solar panel efficiency, it isn't transparent. For window-friendly solar panels, researchers have been exploring organic materials. These materials are known generally as "non-fullerene acceptors" to set them apart from the more robust but less efficient "fullerene acceptors" made of nanoscale carbon mesh. The team has already increased the transparency of the module to 40%, and they believe they can approach 60%. (*IEEC file #12468, Science Daily, 9/14/21*)

3-D-printed copper windings for electric motors. ExOne and Maxxwell Motors researchers have successfully proved a new concept for 3-D printing a high-efficiency copper e-winding design for electric motors using a binder jet system. The new process eliminates many of the challenges that come with traditional manufacturing of copper coils for electric motors. In binder jetting, machines bond layers of metal powder with a binding agent before final sintering in a furnace. The technology excels at making complex metal parts with excellent mechanical properties. (*IEEC file #12481, Design Fax, 9/17/21*)



Market for fully printed sensors will reach \$4.9 billion by

2032. Printed and flexible sensors constitute the largest printed electronics market outside of displays, and the market for fully printed sensors will reach \$4.9 billion by 2032. This growth is despite the sustained displacement of its largest market: printed glucose test strips. Market growth of the overall category is enabled by the rise of many new applications. Printed sensors span a diverse range of technologies and applications, ranging from image sensors to wearable electrodes. Each sensor category seeks to offer a distinctive value proposition over the incumbent technology, with distinct technological and commercial challenges on route to widespread adoption. Most important is the increasing adoption of IoT and Industry 4.0 because they will require extensive networks of often wire-lessly connected low-cost and unobtrusive sensors. *(IEEC file #12482, Printed Electronics World, 9/15/21)*

Intelligent robots pick, prune in the peach orchard. Georgia farmers produce 130 million pounds of peaches every year. Workers around the orchard are tasked with pruning, thinning, and picking. Georgia Tech Research Institute researchers are testing a new idea to have a robot do all three. They developed an intelligent robot using AI and sophisticated navigation to handle the tasks of removing branches, finding good peaches, and removing them from a tree. The robot uses both LIDAR and GPS to self-navigate through the orchard. The LIDAR system determines distances by targeting an object with a laser and measuring the laser beam's return time, while the GPS measures locations. *(IEEC file #12483, NASA Tech Briefs, 9/21/21)*



Recent Patents

Electrical interconnect structure with radial spokes for improved solder void control (assignee: Infineon Tech.) patent. no. 20210233839. An electrical interconnect structure includes a bond pad having a substantially planar bonding surface, and a solder enhancing structure that is disposed on the bonding surface and includes a plurality of raised spokes that are each elevated from the bonding surface. Each of the raised spokes has a lower wettability relative to a liquefied solder material than the bonding surface. Each of the raised spokes extend radially outward from a center of the solder enhancing structure.

Filled through silicon vias for semiconductor packages (assignee: Semiconductor Components Industries) patent. no. 11,075,306. Implementations of semiconductor packages may include a wafer having a first side and a second side, a solder pad coupled to the first side of the wafer, a through silicon via (TSV) extending from the second side of the wafer to the solder pad, a metal layer around the walls of the TSV, and a low melting temperature solder in the TSV. The low melting temperature solder may also be coupled to the solder pad through an opening in a base layer metal of the solder pad.

Printed circuit board assemblies with engineered thermal paths (assignee: Anaren Inc.) patent. no. 20210243880. A printed circuit board (PCB) having an engineered thermal path and a method of manufacturing are disclosed. In one aspect, the PCB includes complementary cavities formed on opposite sides of the PCB. The complementary cavities are in a thermal communication and/or an electrical communication to form the engineered thermal path, and each cavity is filled with a thermally conductive material to provide a thermal pathway for circuits and components of the PCB. The method of manufacturing may further include drilling and/or milling each cavity and filling the cavities.

Package substrates with magnetic buildup layers (assignee: Intel Corp.) patent. no.11081434. The present disclosure is directed to systems and methods for improving the impedance matching of semiconductor package substrates by incorporating one or more magnetic buildup layers proximate relatively large diameter, relatively high capacitance, conductive pads formed on the lower surface of the semiconductor package substrate. The one or more magnetic layers may be formed using a magnetic buildup material deposited on the lower surface of the semiconductor package substrate. Vias conductively coupling the conductive pads to bump pads on the upper surface of the semiconductor package substrate pass through and are at least partially surrounded by the magnetic buildup material.

Chip-last wafer-level fan-out with optical fiber alignment structure (assignee: Ayar Labs) patent. no. US2021 /018049. A redistribution layer is formed on a carrier wafer. A cavity is formed within the redistribution layer. An electrooptical die is flip-chip connected to the redistribution layer. A plurality of optical fiber alignment structures within the electro-optical die is positioned over and exposed to the cavity. Mold compound material is disposed over the redistribution layer and the electro-optical die. A residual kerf region of the electro-optical die interfaces with the redistribution layer to prevent mold compound material from entering the optical fiber alignment structures and the cavity. The carrier wafer is removed from the redistribution layer.

PCB to dielectric layer transition w/controlled impedance and reduced crosstalk for quantum (assignee: IBM Corp.) patent no. 11102879. A transition between a printed circuit board (PCB) and a dielectric layer with controlled impedance and reduced and/or mitigated crosstalk for quantum applications are provided. A quantum device can comprise a microwave quantum circuit on a dielectric substrate and a PCB comprising a via that comprises a transmission line. A wirebond between the transmission line of the PCB and a transmission line of the microwave quantum circuit operatively couples the microwave quantum circuit to the PCB. The via comprises a defined characteristic impedance. The wirebond provides a microwave signal connection between the PCB and microwave quantum circuit.

Printed wiring board islands for connecting chip packages (assignee: Intel Corp.) patent no.11,134,573. A printed wiring board island relieves added complexity to a printed circuit board. The printed wiring board island creates an island form factor in the printed circuit board. Coupling of a semiconductive device package to the printed wiring board island includes a ball-grid array. The ball-grid array can at least partially penetrate the printed wiring board island.

What PDN TARGET IMPEDANCE Means for PCB Designers

A noisy PDN can easily become a strong parasitic EMI antenna. by RALF BRÜNING

High-speed circuits are used almost everywhere in electronic applications today.

As a result, the importance and mechanisms of impedance (herein the meaning of PCB trace impedance – typically referred to as "characteristic impedance") for signal integrity have been widely discussed and seem to be generally understood by PCB designers.

Simply put, PCB trace impedance is a measure of the resistance that a circuit opposes to a current once a voltage is applied. So far so good. But the concept of impedance is also used in PCB design to describe the behavior of power distribution systems/power distribution networks (PDS/PDN). And this PDN impedance is becoming more of a headache for PCB designers as IC vendors define increasingly tight so-called "target impedance limits" that a design must meet (a few milliohms over a broad frequency range).

Are you sure what the term PDN impedance means for you and what to pay attention to when designing a PDN? Let's look at what PDN impedance and target impedance are and take a stab at explaining their importance for the design of modern high-speed digital boards.

The Relationship of Impedance, Capacitance and Inductance

The theory of electronics plays an elementary role in analyzing impedance issues, just to mention here Ohm's law, Kirchhoff's laws, and for inductance, Faraday's laws. But even without diving in deeply, design engineers know that for board traces the characteristic impedance "Z0" is directly related (lossless case here, for simplicity) to the trace inductance (L) and the trace capacitance (C), or in formula definition:

$$Zo = \sqrt{\frac{L}{c}}$$

Hence, trace capacitance depends directly on the trace construction within the board: trace width, copper height, and the trace's distance to a reference layer acting as a return path. The dielectric constant "" of the surrounding insulation material also has its impact. Knowing this, it can be rather simple to predict the effects of certain physical construction changes on the trace impedance value by analytical formulas.

For closely coupled traces and trace geometries with etching and copper roughness impact, however, such a prediction can become complicated. Design engineers should always keep in mind the relationship between capacitance and impedance is somehow inverse, which means if "C" increases, "Z0" decreases and vice versa. But how does this apply to power distribution systems?

Power distribution systems typically comprise a combination of larger (and/or smaller) copper areas together with power traces, PDN vias, and many small connection stubs to carry energy from the power sources (bucket converters, VRMs, or PMICs) to the active circuits (ICs) – with some discrete components (capacitors, resistors, inductors) in between. How and where does impedance come into play?

Introducing PDN Target Impedance

As clock and data frequencies increase and high-speed boards become densely populated with increasingly power-demanding integrated circuits (pin counts rising to over 1,000), ensuring a noise-free power distribution from the source to the sinks becomes a major challenge for the design engineer.

Typically, many IC buffers on a board simultaneously change their state. These fast-switching devices cause ripple voltages that propagate through the entire power distribution network and create noise peaks. These vary in frequency and location on the board. As we learned in school, energy will never just disappear. Therefore, the noise (= energy) can easily disturb any surrounding high-speed devices and circuits. Ripple voltages can also be strong EMI sources, creating highimpact parasitic EMI antennas through conductive coupling.

In switching mode, where there are voltages and current

flows, the ratio between these two values forms the impedance of a PDN, like the simplified one in **FIGURE 1**. For the sake of simplification, only the plate capacitance of the planes is shown, just as not all different inductances are included in the figure either.

One approach to ensuring the proper operation of highspeed systems while maintaining the required performance is to control the power delivery network impedance over a certain frequency range (FDTIM = frequency domain target impedance method). This can be achieved by carefully designing the structure of the power distribution network and accounting for the total PDN capacitance and all various inductances. The overall capacitance number goes beyond the plate capacitance of the power-ground overlap areas and includes bulk capacitance of the large capacitors, all the decoupling capacitance and, at the end, the embedded capacitance within the IC packages and IC die itself.

The most straightforward approach to explain the impedance of a PDN is:

 $Z_{PDN} = \Delta I / \Delta V$

If we take a closer look at the frequency behavior (see FIG-URE 2), it becomes clear that any PCB power delivery network will show some degree of capacitive behavior at lower frequencies while this capacitance decreases due to the resistance of the power-bus in series with all the load components and its

return path, and then the inductive behavior typically dominates. Figure 2 shows all impedances vs. frequency for an NXP iMX55 CPU for a DDR3 power rail of an automotive ECU for all the CPU power pins.

The impedance is affected by the physical separation within the power rail in the board stackup. As frequencies increase, the mutual inductance between the different circuits on the board cause the impedance of the power distribution network to increase. Due to various effects, the impedance of such a structure shows many peaks (resonances and anti-resonances). At higher frequencies, the impedance often negatively influences the input behavior of the



FIGURE 1. Simplified schematic structure of a PDNX.



FIGURE 2. Impedance vs. frequency (Z(f)) of a PDN of an NXP iMx5 CPUX.

ICs, which is highly undesirable, especially in the frequency range in which the ICs are supposed to operate.

Target Impedance Values in PDN Design

The knowledge and control of the target impedance have become a standard approach for proper PDN design, especially when designers must meet the given IC vendor or application specs. A target impedance, by definition, sets a limit on the highest impedance the power rail on the die may be exposed to in its connection to the PDN.

Different formula approaches, all based on Ohm's law, state that the ratio of voltage to current results in the resistance (= impedance). For a PDN, the voltage in these formulas is the supply voltage in relation to the maximum ripple ([D]V) on the power supply, which ICs are allowed to accept. (IC vendors have this information.) In its simplest form, the target impedance can be described as:

$Ztarget = \frac{Vsupply * \% rippetolerance}{0.5 * Imax}$

Hence, the target impedance can be understood as a limit of the current/voltage ratio to ensure that the [D]V from Eq. 2 does not exceed the desired ripple voltage limits. If the PDN impedance stays below the calculated value, even the worstcase transient current from the IC die generates a small rail voltage noise, which is still acceptable for operation.

> The impedance waveform of a power delivery network should ideally be without larger peaks within the frequency band in which the ICs operate. This is the fundamental guiding principle in the target-impedance-based design approach of PDNs. Another matter of concern is the relevant bandwidth. For digital signals, the bandwidth com-

> > prises all frequencies between the clock and the knee point on a frequency curve, which can in a rule-of-thumb approach be defined as 0.35 divided by the fastest signal transient rise/fall time.

> > If all the harmonics of digital signal resonate at the same frequency, the transfer function for the return signal in a ground plane

is rather flat, which is what we are looking for. For a really complex PDN, every occurring impedance peak is created by a parallel RLC circuit. The characterizing terms for such impedance peaks are:

- Parallel resonant frequency
- Characteristic impedance (and the q-factor, not discussed here)
- Peak impedance.

The parallel resonant frequency defines the frequency at which the inductive reactance

equals the capacitive reactance. This frequency point can be calculated from:

$$f_{res} = \frac{1}{2} \pi * \sqrt{L * C}$$

When a transient voltage occurs at the resonant frequency of the peak, the amplitude of the resulting voltage swing may exceed the nominal voltage given by the target impedance equation. To further complicate the matter, often there are further impedance peaks (multiple resonances and anti-resonances) over a wider frequency range to deal with.

Not every peak that exceeds the target value means the system is not working. However, the peaks could lead to non-deterministic IC power failures during system operation. This opens a Pandora's box for debugging such hardware failures. But even if the peak stays below the impedance limits, the circuit may not be perfectly safe, so countermeasures may be required to lower the impedance or shift occurring peaks in frequency.

First Aid Kit to Lower PDN Impedance

The idea behind FDTIM is to ensure the PDN design meets the target impedance and the values for the relevant frequency range stay below the given limits. Yet, this is easier said than done. A PCB usually contains dozens of active components, often several hundred capacitors and inductors with all their parasitic characteristics (e.g., ESL and ESR of the capacitors). Other parasitic inductors on the different PDN elements (e.g., pads/land patterns, vias, and traces) can also heavily affect PDN impedance values.

To lower the impedance of the PDN, engineers can tweak two general things: reducing the inductance and/or increasing the capacitance of the PDN. The placement and value of decoupling capacitors play an important role in such an optimization, as this will affect both the capacitance and the induc-



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tance of the PDN. Placing the capacitors on the same layer as the IC supply pins, for example, minimizes the inductance. Unfortunately, this is often not possible for space or manufacturing reasons. Nevertheless, if resonance peaks are revealed in a PI analysis, the copper shapes of the PDN most likely must be modified to eliminate these peaks efficiently.

Unfortunately, given the complexity of today's PDNs and all the parasitic effects, analyzing a circuit layout for PDN impedance can hardly be done with a good old pen and a sheet of paper. Furthermore, PCB CAD tools cannot handle target impedance issues simply by defining a design rule or adding an attribute to a power supply network, even if this is desirable for the design engineer.

Instead, advanced engineering tools like numerical PI solvers are needed. Such simulators have been available on the market for many years. An easy exploration and verification of power distribution systems are possible as an integral part of the PCB design process. In lowering the power distribution network impedance across the required range of frequencies, potential EMI issues can be eliminated too.

If such an analysis reveals resonance peaks in a PDN exceeding the target impedance, corrections can be engineered in a virtual sandbox through the parametric study capabilities of some ECAD tools. Such corrections, for instance, include adding virtual decaps, changing values and ESL of the capacitors, or even turning them off without the need for physical design changes in the tool.

Conclusion

This concurrent PI analysis approach helps PCB designers avoid overengineering a PDN. An overly cautious approach typically results in adding redun-

dant capacitors and extra validation hours, which translate into unnecessary costs.

As a final reminder, digital engineers should always keep in mind the situation is often worse than initially thought (Murphy's law). Power integrity issues such as impedance resonance peaks negatively influence the signal integrity behavior of boards, and in their nature as a (rather very large from the physical size of the structure) LC-resonator, a noisy PDN can easily become a strong parasitic EMI antenna. This underlines the importance to keep the PDN impedance number under control. \Box

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FIGURE 3. Example of IC vendor target impedance limits (source: Qualcomm).



FIGURE 4. Impedance mask definition to check IC vendor rule compliance using the Zuken PI Simulator.

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THIN FOIL PRINTING in Today's Miniaturized World: Do Printing Rules Change?

A series of experiments test the well-known area ratio rule. by CHRYS SHEA, GREG SMITH and RAY WELCH

A stencil aperture's area ratio (AR) is a simple calculation that divides the area of the aperture opening by the area of its wall. It was derived in the 1990s and compares the adhesive forces of the solder paste deposit on the PCB pad with the adhesive forces of the solder paste on the stencil walls. For the material to transfer efficiently, the forces holding it to the pad must overcome the forces holding it to the aperture walls. Therefore, calculating the relative areas represents the relative adhesive forces affecting solder paste release.

The amount of solder paste released from an aperture is referred to as transfer efficiency (TE) and expressed as a percent of total aperture volume. Stencil or solder paste release characteristics are often illustrated by plotting TE against AR.

AR guidelines were originally set at 0.66 as a minimum to ensure good (>80%) TE. Many of these original guidelines have been relaxed due to improvements in solder paste, stencil materials and nanocoatings. With good materials, equipment and tooling, and robust printing practices, apertures with ARs as low as 0.50 can often be printed in production on 4-mil thick stencil foils with excellent results.

Maintaining ARs of 0.50 or greater can be difficult for the stencil designer. Miniaturization is now driving finer and finer features, which, in turn, is driving thinner foils to meet classic AR design rules. This raises the question: Do classic design rules apply in the case of thin foils?

Experiment

Design. A simple 2 x 2 factorial experiment was devised using the print-to-fail (PTF) patterns of the SMTA Miniaturization Test Vehicle¹ shown in **FIGURE 1**.

The PTF patterns have pads that are square, circular or rectangular, solder-mask- and non-solder-mask-defined, in widths of 3 to 15 mils. Solder-mask-defined (SMD) pads are also referred to as simply "mask-defined"; non-solder-maskdefined (NSMD) pads are also referred to as metal-defined or copper-defined. Each pad's corresponding apertures are either the same shape as the pad (S) or are square/rectangular with radiused corners (R). There are 32 datapoints on each print. Each dataset is made up of 20 prints, for a total of 640 datapoints for each combination of shape, definition, size and aperture geometry in the database.

Four stencils were tested: 2- and 3-mil thickness, with and without nanocoating.^{2,3}

The solder paste used in this test was Indium 8.9 HF Type 5-MC. The powder particle size distribution was the standard $15-25\mu$ m diameter. Type 4 was tried but showed too much variation on thin foils to be considered acceptable; therefore, the results for the Type 5 solder paste are analyzed and presented.

Execution. Print tests were performed in Koh Young America's demo room in Duluth, GA, using the following equipment set:

- Printer: MPM Momentum BTB
- Support tooling: Quick Tool; three modules



FIGURE 1. Print-to-fail patterns and aperture shapes.

- Clamps: EdgeLoc with retracting top foils
- Squeegees: MPM FP100, 250mm length
- Stencils: 2- and 3-mil BlueRing Nano-Slic Gold and Uncoated Fine Grain (Slic) stencils
- SPI: Koh Young 10µm aSPIre3
- SPI height threshold: 20µm The print parameters were:
- Speed: 30mm/sec
- Pressure: 7.0kg
- Separation speed: 5.0mm/sec
- Separation distance: 3.0mm
- The understencil wipe parameters were:
- Speed: 30mm/sec
- Sequence: wet/vac/vac or wet/vac/vac/dry
- Frequency: 1 (after each print)

Each test run began with four to six knead strokes to ensure the solder paste reached its working viscosity and two to seven setup prints to verify proper print performance and paste alignment before running the 20 data-producing prints. Execution time for the tests were approximately 30 minutes each, with continuous printing, under wiping and inspection.

Analysis. Data were exported to a .csv file and imported to Excel for manipulation. A pivot table was created to review the solder paste volumes, TEs and CVs. Appendix A (online) has details on the data manipulation methods.

Process capability and the coefficient of variation. The coefficient of variation (CV, CoV or CofV) is calculated as the standard deviation of a population divided by its mean. Applied to solder paste deposits, CV represents the spread of the volume, height, area or offset data. Because the average volumes of solder paste deposits vary based on many input variables, basic standard deviations should not be used to evaluate different distributions of data. Expressing the variation as a percent of the average normalizes it for better comparison.

As solder paste deposits become smaller, minimizing their variation becomes more critical:

- As passive devices get smaller, they are more prone to positional, rotational or tombstone-type defects related to print quality.
- As integrated circuit packages get smaller and leadless, they are more prone to head-in-pillow, insufficient solder joints, voids and intermittent opens related to print quality.

Controlling the variation in print volumes limits the opportunities for defective solder joints and their associated rework or failure costs.

A widely accepted guideline for solder paste deposit CVs is:

- <10%: preferred</p>
- 10-15%: acceptable
- >15%: unacceptable

These guidelines are based on statistical process control (SPC) principles. Assuming a normal distribution of data as seen in **FIGURE 2**, 99.7% of the data should fall within +/-3 standard deviations of the mean. If we apply a typical SPI control limit of +/-50%:



FIGURE 2. Normal distribution as it relates to solder paste volume variation.

- CVs of 10% will produce 99.7% of deposits within +/-30% of the target volume, leaving plenty of room for outliers or special causes of variation.
- CVs of 15% will produce 99.7% of deposits within +/-45% of the target volume, leaving little room for variation.
- CVs of 16.7% or higher will produce deposits outside the control limits, indicating an out-of-control process.⁴

In this study, CVs were analyzed first to distinguish datasets worth investigating from those that were not. Datasets with CVs of 15% were reviewed prior to inclusion into the database.

Disqualification of the smallest deposits. Upon review of the data and PCBs, 3- and 4-mil deposits were removed from the results. Their CVs were all greater than 15%, and inspection of the PCBs revealed many of the NSMD pads less than 5 mils were missing from the bare PCBs. This did not come as a surprise, as features that size present challenges to fabricators, which were granted waivers for features 5 mils or less.

The pivot table results of the different combinations of foil thickness, coating, pad shape and pad definition and the calculated CVs can be seen in Appendix B (online).

Unacceptable levels of variation were demonstrated by the 3- and 4-mil feature sizes; further statistical analysis was



FIGURE 3. Missing pads in PTF test patterns.

performed on the data from pads 5 mils and larger.

Results

The SPC run charts shown in **TABLE 1** illustrate the effects of pad definition. There is a sharp contrast in print variation between the solder-mask-defined and copper-defined pads. In the best-case printing scenario of solder-mask-defined square pads, the CV of 12% indicates 5-mil features can be printed-repeatably using a 2-mil coated foil; the CV of 11% indicates the same for a capability with a coated 3-mil foil.

The CVs for copper-defined pads were over 20% for both 5- and 6-mil features. The process of printing on copperdefined pads did not show preferred capability (CV<10%) until feature sizes of 7 mils, even with square pads, which performed better than round ones.

The transfer efficiencies also vary greatly between solder-mask- and copper-defined pads. Solder-mask-defined pads offer better gasketing than copper-defined ones, and limit the amount of "squeeze out," or excess solder paste to transfer from the aperture to the PCB.

FIGURES 4 and **5** show the contrast in TE between the two pad designs for the 2- and 3-mil foils, respectively.

Regardless of foil thickness, the TE curves both show the same trends regardless of pad or aperture shape; for mask-defined pads, TEs showed typical behavior, but on copper-defined pads, excess paste was the rule rather than the exception.

On solder-mask-defined pads, TE is approximately:

- 70% at 5 mil
- 80% at 6 mil
- 90% at 7 mil
- 96% at 8 mil

These are all reasonable transfer rates with preferred or acceptable CVs.

On copper-defined pads, TEs averaged:

- 140% at 5 mil
- 140% at 6 mil
- 130% at 7 mil
- 125% at 8 mil

These TE rates, coupled with highly unacceptable CVs on copperdefined pads most likely indicate a lack of good gasketing between the pad and the stencil.

The run charts also show unanticipated spread in the data for prints 3, 13 and 19. The effects are more pronounced on the smaller features. This will be discussed in detail in the discussion section addressing pad definition.

The main effects plot shown in **FIGURE 6** demonstrates the influence of the individual factors on print volume repeatability. The axis values have been omitted to focus on the relative impact of each and the inputs that minimize it.

The leading factor influencing print repeatability was the stencil coating. Feature size was a close second, followed by pad definition. With lesser influence, the 2-mil foil produced more consistent print volumes than the 3-mil foil. Pad shape and aperture corner type had negligible influence on print variation.

Discussion

Top factors in variability. As indicated in Figure 6, stencil

TABLE 1. Pad Definition Effects

	Ball D	iameter	
	Avg.	Largest	
	20	25	
5 Ball Rule	5x Avg.	5x Largest	Aperture Width
	100	125	
		125 = 5 mil	
3-Ball Rule	3x Avg.	3x Largest	Foil Thickness
	60	75	
	60µm = 2.4	75µm = 3 mil	



FIGURE 4. TE chart for 2-mil coated foil.



FIGURE 5. TE chart for 3-mil coated foil.



FIGURE 6. Main effects plot and Pareto diagrams.

coating is the top factor in minimizing variation. It is also obvious in the side-by-side comparisons of TE and CV in Appendix B, which show the coating provides better print repeatability (lower CV) for every pad design configuration.

Although not quantified, cleanability was a considerable factor noticed during the testing. It was observed that the coated stencil released the paste to the automatic underwiping system far better than the uncoated one. The thin layer of smeared solder paste particles and flux left behind on the stencil after auto wipe likely factored into its poorer print results.

The influence of pad size – the bigger the feature, the easier it is to print – is related to AR, but does not necessarily follow general AR rules.

Pad definition. FIGURE 7 shows a basic diagram comparing the two methods of designing PCB solder pads. Non-soldermask-defined (NSMD) pads are etched onto the PCB at their nominal size. It is not uncommon, however, to find pads overetched – or undersized – by up to 2 mils.

FIGURE 8 further describes features of the different types of pad definition. Given that smaller pad sizes are more susceptible to overetching, growing the copper size by 6 mils makes it much easier for the fabricator to etch; even it if gets overetched by (an acceptable) 2 mils, there is still room for the solder mask to encroach on all sides. When all edges of the pad are covered with solder mask, the mask provides an excellent gasketing surface for the stencil, resulting in less variation in print quality and, typically, slightly higher volumes.

When pads are metal-defined, they are naturally harder to

gasket to than mask-defined pads, but their propensity to be overetched exacerbates the gasketing problem. Poor gasketing of NSMD pads leads to excess solder paste deposition, as seen in Figures 4 and 5.

Another deleterious effect of overetched PCB pads is their impact on true AR. Recall that AR is calculated as the ratio of the area of the aperture opening to its walls. This calculation is based on the assumption the aperture opening fully contacts the PCB pad. When the pad is smaller than the stencil aperture, it does not offer as much area for the solder paste to stick to, thereby reducing the true AR and introducing additional variation to the process.

Traditional pad design, especially for BGAs, generally trends toward NSMD pads, because the solder mask relief enables molten solder to wrap around the edges of the pad, giving the solidified joint more shear strength than with SMD pads (Figure 8). For larger BGAs with feature sizes that are more easily printed and experience greater displacement during thermal expansion, NSMD pads are still generally preferred, but in the case of very small features, mask defining them can add shear strength between the pad and PCB due to the larger area of the pad and the reinforcement of the mask.

As mentioned, the fabrication notes for this test PCB allow a waiver for pads 5 mils and smaller. Inspection of the incoming PCBs showed many were missing their 3- and 4-mil NSMD pads (Figure 3), and some of the 5-mil NSMD pads were barely visible. The run charts in Table 1 show excessive noise for print numbers 3, 13 and 19, particularly on the NSMD pads. The issue appears to resolve as the feature sizes get larger, and only appears on the smallest SMD pads. The source of the noise in these three prints could likely be attributed to overetch of the pads on those specific PCBs.

Aperture shape. Aperture shape had very little impact on print quality. This appears to contradict prior data generated on larger

feature sizes and generally accepted design rules r e l a t i n g to radiusing aperture corners to improve paste release and repeatability.



FIGURE 7. Comparison of PCB pad definition.







FIGURE 9. The effect of rounding aperture corners as aperture sizes shrink.



FIGURE 10. AR of small features increases dramatically as the foil gets thinner.

Typically, stencil manufacturers put a 2-mil radius on square apertures, and often apply the "squircle" aperture to round pads. At feature sizes under 8 mil, the radius is 25% of the side length of the square. As the squares get smaller, and 50% of their side length is part of the corner radii, the squircle shapes become more circular than square, as seen in **FIGURE 9**, and the performance difference becomes relatively inconsequential.

Pad shape. In a trend similar to the contradictory nature of the aperture shape results, pad shape had very little influence on print variability. The advantages of square pads (from a print perspective) also appear to dwindle as their size shrinks.

The area ratio rule. Area ratios increase as foil thicknesses decrease, but with foils less than 4-mils thick the difference is more dramatic (FIGURE 10).

An 8-mil feature size has an AR of 0.50 on a 4-mil foil, 0.67 on a 3-mil foil, 1.0 on a 2-mil foil! Similarly, the AR for a 6-mil feature climbs from 0.5 on a 3-mil foil to 0.75 on a 2-mil foil!

With respect to print volume variation, size was a greater factor than AR. In many cases of mask-defined pads, variation was acceptable or preferred for features 5 mils and larger.

With respect to TE, pad definition had a far greater effect on print capability than AR.

In the best cases of SMD pads and coated stencils, 5- and 6-mil features were the smallest to print successfully – on both 2- and 3-mil foils. The lowest AR of this combo was 0.42, and the highest was 0.75. However, in other scenarios, acceptable printing wasn't achieved until 8- or 9-mil feature sizes, with much higher ARs.

The area ratio rule of 0.60 or higher cannot be applied to all situations when using thinner foils. Considering foil thickness has four times the influence of aperture size on AR (the algebraically reduced AR calculation for circles is D/4t, where D is the diameter of the circle and t is the foil thickness and similar for squares as S/4t, where S is the side length of the square and t is the foil thickness), AR may no longer be the best overall indicator of solder paste release.

In this test, pad size and definition are the key design factors, and stencil coating is the key manufacturing factor. Size may be related to the three- and five-ball rules (yet to be discussed), but pad definition is related to design. Having the correct pad contact area to produce a true AR scenario and the benefit of good gasketing makes the biggest difference in printability of these fine features with thin foils.

When considering stepping a 4-mil stencil down to 2 or 3



mils to accommodate fine features, note in these tests, both the 2- and 3-mil coated foils printed relatively comparably. Given similar results between the two thicknesses and faced with a choice, an assembler might consider stepping down to 3 mils as opposed to 2 mils, as it would result in a more robust stencil with a longer production life.

Three-ball rule. The three-ball rule states a stencil's thickness should be at least three times the diameter of the *largest* ball. A common corollary states it should be at least three times larger than the *average* ball diameter. It is illustrated in **FIGURE 11**.

The Type 5 solder paste had most of its particles in the $15-25\mu m$ range. Assuming the largest is $25\mu m$ and the median is $20\mu m$, both scenarios can be theoretically tested:

- 3*25=75µm, or 3 mil
- 3*20=60µm, or 2.4 mil.

The thinnest foil to produce good prints was 2 mils. Again,

it appears pad design and stencil coating enable this capability. For the uncoated stencils, the 2 mil printed better than the 3 mil for SMD pads; for the coated stencils, the 2- and 3-mil foils both printed comparably on the SMD pads.

The three-ball rule does not appear to apply to SMD pads in this test, perhaps because the mask definition creates a "well" that effectively increases the depth of the aperture with respect to solder paste filling, but does not negatively influence release from the aperture.

Five-ball rule. The five-ball rule states a stencil's minimum aperture width should be at least five times the diameter of the largest ball. As with the three-ball rule, an existing corollary states it should be at least five times larger than the average ball diameter (FIGURE 12). printing, these data indicate the largest ball diameter should be applied. It can only be applied to SMD pads, however, as NSMD pads produced unacceptable print volume variation.

Conclusions

In the context of solder paste stencil printing, reducing variation has always been as important as maintaining high transfer rates. However, in leading-edge electronic miniaturization, where excess variation is the root cause of most soldering problems, it is arguably more important than average paste transfer rates. This analysis reviewed transfer rates, actual volumes and variation, with the focus on factors that minimize variation.

Factors that minimize variation can be grouped into two distinct categories: design and manufacturing.

With respect to product design, solder-mask-defined pads and the sizes of those pads had the largest influence on

repeatability. SMD pads are easier for PCB fabricators to make and easier for SMT assemblers to print. It is highly recommended any PCB features smaller than 8 mils should be mask-defined (when using a Type 5 solder paste), and as pad sizes get smaller, the positive effects of mask defining the pads become more obvious.

With respect to manufacturing, coating the foil with the flux-repelling ceramic nanocoating has the largest influence on reducing variation. In fact, on non-soldermask-defined (NSMD) pads, uncoated stencils were not capable of meeting the preferred CV metric of <10% for any features 8 mils or smaller, and in only one situation met the acceptable value of <15%. Uncoated stencils were also very difficult to clean using automatic underwipe.

Foil thickness appeared to have a considerable effect

To ensure good aperture fill, the thinnest foil that can be successfully printed is 3X the diameter of: The largest T5 solder particle 25 µm 25 µm 3 mil Solder Mask Defined pads printed well with coated stences all the way down to 2 mils! The three-ball rule does not seem to apply

FIGURE 11. The three-ball rule.



FIGURE 12. The five-ball rule.

So again, assuming the largest particle has a 25µm diameter and the median has a 20µm diameter, both scenarios can be theoretically tested:

- 5*25=125µm, or 5 mil
- 5*20=100µm, or 4 mil

The finest feature to print successfully on SMD pads was 5 mils. Even in the best-case scenario, the 4-mil pads demonstrated too much variation to be considered valid data worth analyzing.

To interpret the five-ball rule with respect to thin foil

on print variation; however, a very profound effect was seen on the uncoated stencils, and a detailed review of the actual results between 2- and 3-mil coated foils is extremely close with respect to both actual volumes and CVs.

With respect to traditional guidelines of the area ratio rule, the three-ball rule and the five-ball rule, some principles may still apply, and some may not.

In the context of SMD pads and coated stencils, an AR of 0.6 or higher can be applied to the 2- and 3-mil stencils. Both

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fell a little shy of 80% TE goals, but met CV goals of <10%, indicating viable processes that could likely be optimized with further statistical analysis of the stencil design and processing parameters.

The three-ball rule was tested with both the largest and average-sized solder particle and did not comply with the 3x guidance. It predicted minimum foil thicknesses of 3.0 and 2.4 mils, respectively, for the largest and average-size particles. The thinnest foil to print successfully was 2 mils thick, thinner than the rule predicts. It should be noted again the difference between SMD and NSMD pads was pronounced, and successful printing occurred on the SMD pads. SMD pads may offer an advantage in aperture filling due to the extra depth they provide, but do not offer a disadvantage in paste release, which is based on stencil wall contact.

The five-ball rule may still partially apply. The finest feature to print repeatably was 5 mils, or 125μ m, exactly 5x the diameter of the largest ball, and only with coated stencils.

None of the 4-mil features printed repeatability, even when mask-defined and with a coated stencil.

DfX Takeaways

- The best thing designers can do to improve the producibility and reduce the cost of miniaturized electronics is to soldermask-define the PCB pads.
- The best thing a PCB assembler can do to limit variation and improve yields is to nanocoat the foils, no matter how thin they are.

Potential Future Work

Similar tests using the same solder paste formulation⁵ have been performed with Type 4 solder paste and 4-mil foils. Those tests have indicated the T4/4 mil combination repeatably prints (CV<10%) NSMD pads down to 10 mil, and SMD down to 9 mil and, in some cases, 8 mil. Because the data were generated on different equipment sets at different locations and times, the data are not directly comparable. Ideally, however, a consistent data set that compares performance of T4 with 4-mil foil and T5 with the 4-mil foil can help determine the best print scenarios for features in the 6- to 10-mil size range.

Smaller particle sizes present greater reflow challenges. If possible, on future print tests, a few extra boards should be printed at the end of the test and reflowed to help determine fusion (non-graping) characteristics of the solder paste and the possible effects of inerting the reflow environment.

Ultimately, feature sizes will continue to shrink, and technology will continue to develop. Type 5.5 and 6 solder pastes will probably be tested in the near term, as will newer foil materials that can retain specific print properties with lower profiles.

Type 5 solder paste presented underside cleaning issues with uncoated stencils in this test. In other tests, it has also presented similar issues in offline stencil cleaning and misprinted board cleaning. Studies comparing the cleanability of wet T4 and T5 solder pastes would be beneficial to prepare for the inevitable transition to finer powders as electronic assemblies continue to shrink. \Box

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A Guide to Make One Perplexed

Or how the metaverse will save us, one contorted axiom at a time.

AMBROSE BIERCE, OF sainted memory, is known for a *Devil's Dictionary*, a cynic's primer on human behavior, laid out in Noah Webster style.

Pity he strayed into hostile territory in banditinfested Northern Mexico in 1913, never to be seen again. Maybe someone lurking in the sagebrush took offense at imagined slights in the *Dictionary*. People are so thin-skinned.

Pity also that he lived one hundred years too soon. Bierce missed his moment. Obfuscation has exploded, rivaling worthless college degrees (or maybe because of them). A euphemistic pandemic with no known vaccine, for which we need a new dictionary, has infiltrated our lexicon. Straight talk in professional settings is frowned upon, covertly if not overtly. Blunt talk is often memorable and career-threatening. Verbal mush is benign and soon forgotten. As the author of the Bartleby column in the Nov. 20, 2021, edition of *The Economist* noted, concerning contemporary biz-speak, "People rarely say what they mean, but hope that their meaning is nonetheless clear. Think Britain, but with paycheques. To navigate this kind of workplace, you need a phrasebook."

In 2021, you need a big phrasebook. Facility with fluff has become no less a survival skill for shop floors as in corporate boardrooms or the financial press. One can fake profundity without the bothersome obligation to prove the rightness or efficacy of one's statements. The heads just keep on nodding.

Give examples, you say. Fair enough; navigate, we will. Herewith is a modest sampling. Thanks to Frances Stewart for the inspiration.

"**Pivot**," *N*. As in, "We are experiencing an unprecedented iconic transformational existential pivot in our business."

What they really mean: S--t happens. Under cover of Covid-19, we've been able to complete the personnel and procedural housecleaning we've been wanting to do for years. Thanks, Covid. Act of God, indeed.

"Meta-," *N*. From the Greek "beyond," as in metaphysics; or metamorphosis; or metaverse. As in, "We are experiencing an unprecedented iconic transformational existential pivot in our business to the metaverse."

What they really mean: We are changing the subject, while hoping you don't notice. We are so beyond caring what you think of our behavior prior to October 2021, not that we ever really cared in the first place.

For context, see "Gaslight," V. As defined by The Urban Dictionary and other sources, "to persistently and repeatedly feed false information to an individual in the hope of compromising and thereby casting doubt on their memory or perception of certain events or statements, thus invalidating them or neutralizing their worth, and therefore, their impact to a discussion or argument."

For example, "Social media companies have a very dim and condescending view of human nature and people's memories, rendering those people prone to monetizing. Thus are fortunes built."

Or, "I've always loved electric vehicles and lithium batteries, especially now that I can make a fortune building peripherals to that business, and burnishing my green credentials simultaneously, thus validating me to my kids and to potential new wives of a crunchy disposition." Some EV drivers are '80s Beemer Jerks transplanted to the 2020s. It's still all about the angles. Some play them better than others.

What they really mean: Facts aren't facts, and bad behavior is like relativistic physics; i.e., it all depends on your point of view, thus excusing everything.

For reference see Orwell, George: 1984.

Memo to 2020s version of '80s Beemer Jerks: You still can't take it with you when you die. Perhaps the metaverse will rectify that deficiency.

Enough about generalities. Back to Earth. What about the shop floor, where most of us (at least those of us reading this publication) spend a fair amount of our lives?

"**Issues**," *N*. As in, "Due to issues with our supply chain, we are unable to provide you with a date when we'll be shipping you our hundred-piece flying probe project, which we told you in August needed to be tested and completed by you by December 24, so we may make our year-end, as well as our OEM's yearend. (For reference see transformational existential pivots above, etc.)"

What they really mean: That decision by management (now retired) in 2014 to go to one Chinese source for prototypes and preproduction builds has blown up in our face. The low cost seemed like a good idea at the time. Groupthink made it a no-brainer. What could possibly go wrong? We have MBAs and (therefore) can read spreadsheets! Thank goodness the bonus checks cleared long ago.

Or, "We are unable to complete this assembly due to issues on our production line."

What they really mean: We were so preoccupied

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with installing and tweaking Industry 4.0 sensors in our pickand-place line that we overlooked the deterioration of several dozen feeders needing replacement. Scrap rate took a big jump upward. That's a crisis. We need a means to get to the bottom of this! Meanwhile, keep the line moving over the weekend to make up for lost shipments. Oh, and that 10TB of production data? Just set it over there in the CMMC section of the server.

Or, "We have issues with China. We're going to try the same thing in Vietnam."

What they really mean: We're slow learners.

"Kanban," *N.* As in, "Our Six Sigma system, modeled on GE, now operates on a finely honed Kanban basis all the way across the Pacific. Our suppliers must adhere to this system and get Black Belts certifying that adherence. There can be no disruptions. This is how we will operate going forward. What works for aircraft engines should translate just fine to circuit boards."

What they really mean: Our suppliers finance our inventory. What they also really mean: Financial engineering beats making stuff. Just in time.

"Going forward," N. See "Kanban" above.

As in, "Going forward, our life coaches and emotional mentors will facilitate a results-driven, immersive relational experience that is at once authentic, empathizing, and humanizing, thereby forging an organic symbiosis that resonates with our own cocreating space and our awesome competitive positioning of our corporate DNA."

What they really mean: Tomorrow, the next day and the next day after that, we'll do stuff differently. What we did before didn't work. Let's try something new (like getting a new HR manager).

What they *really*, really mean: Never rely on one syllable when multiples will do.

"Circle back," *N*. As in, "I want to circle back to that awesome slide six of your 400-slide PowerPoint detailing management's 68-point plan for employee empowerment and better officing."

What they really mean: I have nothing better to do than fill up time with meaningless digressions.

And: Asteroids circle back too. Ask the dinosaurs.

"Space," *N.* As in, "I hope this finds you well. I am very impressed with the <u>competitive positioning</u> your company has achieved within the NDT space in the Bay Area region. I believe your business may be a strong fit with what we are looking for at Amoeba Private Equity and would love to discuss the future of your company."

What they really mean: If you're dumb enough to buy our BS and talk to us, we're unscrupulous enough to want to lowball you with an insulting offer to buy your company. For reference see "Mark, easy."

"I hope this finds you well." As in, see "Space" above.

What they really mean: Faux-disarming expression of sin-

cerity, conveying warmth where there is none. (For context, see "Gaslight.") Sales technique used to address a perceived need to fill empty space with vapid verbiage. Emails with this query often begin with the salutation "Hey," conveying additional false intergenerational familiarity.

"Survey," *N.* As in, "Could you please complete this survey about your onboarding experience with our purchasing staff in Bangalore. If you would be so kind as to give our diligent staff members ratings of five on a scale of one to five, they will be most grateful and will have no need for remedial tutelage. Have a Nice Day, Your Malaysia-Based Onboarding Team for Cyclops Corporation. (Our Eye is Always on Quality.)

What they really mean: Please help us keep our jobs from the hordes who are vying to replace us. This recurring pestilence we inflict on all new vendors should be enough to discourage all but the most pathologically motivated from wanting to sign up and become vendors. We have better things to do than waste time with onboarding. Our engineers should learn to live with the existing Chinese supply chain and Kanban rules.

"Vendor," *N*. As in, "The vendor says we should scrap this board design and restart it after a proper DfT analysis."

What they really mean: Vendors dispense stale sandwiches. That's how we view our supply base.

"Thought Leader," *N*. As in, "Please attend our worldwide webinar on Industry 4.0 solutions to climate challenges to the electronics supply chain. Climate reality thought leaders will be present to enable a results-driven, evidence-based, action-oriented, accountability-sustaining dialogue."

What they really mean: Klimawirklichkeitsgedankenführer!

Sounds like an officer in the Waffen SS. Does the Leader proclaim the Truth from a marble balcony for added effect? By derivation, does that make those of us beneath the rhetorical balcony thought followers? How is that indistinguishable from lemmings?

"Ignorance." *N*. As in, "Our success rides on the ongoing ignorance of our members, customers, suppliers, clients, constituents. God forbid they venture to ask questions." This is never spoken or written in an email. It is merely, and firmly, understood.

What they really mean: Careers are made and lost on recognition, mastery and exploitation of this, the strongest, most irresistible force in the universe.

Notwithstanding all that precedes, I rest my case and base my life on one last definition.

"Meliorism," *N*. "The belief that the world tends to

improve, and humans can aid its betterment."

Despite ourselves.

Heaven help us all.

I'll wager Ambrose Bierce would agree. \square

Connecting the Dots: Lean and Field Service

A process for addressing RMA for multi-factory production.

IN A NORMAL business environment, the electronics manufacturing services (EMS) industry has more variation than that of a Lean original equipment manufacturer (OEM). This doesn't mean EMS providers are disorganized. It simply highlights the challenges of an environment where customer inputs dictate supplychain choices, processes and validation methodologies that would normally be optimized to minimize variation at a Lean OEM. Pandemic restrictions, supplychain shortages, logistics constraints and demand prilate of 2021 here.

spikes of 2021 have caused further variation at EMS providers and customers. However, those challenges serve as incentive to increase Lean discipline.

Past columns have highlighted Lean Six Sigma core tools such Gemba and the DMAIC process that help identify and correct quality issues that develop in manufacturing operations as project assumptions change. Lean Six Sigma is helping create an empowered, edu-

cated workforce at SigmaTron, capable of rapidly addressing unanticipated challenges found in today's production environments. That said, defects can escape the factory or be induced by activities once product leaves the factory. Focusing on this area can have a long-term impact on eliminating another set of defect opportunities: *muda* (waste) and cost.

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In SigmaTron's model, field-service engineers work with customers that have higher volume or more technically sophisticated products to determine the root cause of field returns. While the company is achieving industry-standard low defect rates on some of its highest volume programs, even that low percentage generates monthly returns when the printed circuit board assembly (PCBA) count is in the millions.

Initially, this model focused on customers in the consumer products sector. In 2021, however, it was expanded to include industrial sector customers meeting the volume and/or complexity criteria.

In most cases, customers have multiple factories. Regular field engineer visits are scheduled with the factories receiving SigmaTron-manufactured product. In the consumer products area, manual functional test sets that mirror those used for final pack validation audits prior to shipment from SigmaTron are located at each customer factory. This process will likely be replicated with industrial customers where appropriate. When the engineers visit, all line-rejected products are 100% tested on those functional testers. Normally these would become products subject to return material authorization (RMA) processing and returned to the proper SigmaTron factory for process-

"OVER 50% OF RMA PRODUCT IS BEST ADDRESSED At the customer, Saving two legs OF shipping cost."

ing and analysis. Having the field engineers check these before they are returned saves time and cost for both SigmaTron and the customer. Reason: The return analysis shows that more than 50% of the failures are caused by something other than component and workmanship failures in the SigmaTron process. Instead, these types of failures are no trouble found, unintentional customer-induced damages, shipping or customer handling prob-

lems, ESD or electrostatic damage, design or design for manufacturability related issues, and testing capability or testing technical limitation issues.

In short, over 50% of RMA product is best addressed at the customer, saving two legs of shipping cost. In this example, the field engineers work with the customer to either reclassify the no-fault-found product as good or correct the root cause issue at the customer assembly location so they can be immediately addressed. This contributes to fewer overall failures going forward.

Typical issues that drive these types of RMAs include:

Improper cabling at complete end-product assembly

- Test errors in volume testing
- Improper voltages applied during assembly or testing
- Shipping-related damage

Handling or ESD damage issues during higher-level

continued on pg. 44

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Robert Boguski President, Datest

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2022

Avoid Green Solderable Finishes

A look at solder mask contamination on pads.

THIS MONTH WE look at solder mask contamination on pads. FIGURE 1 is a very, very bad example that never

should have made it to the customer. Solder mask residues are visible on the surface and around the edge of the pad. There is also a level of solder mask undercutting.

and would have shown complete nonwetting during

soldering. This would have led to a bad day in the

office for the assembly engineer or, more important,

This would not be acceptable per any standard

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the shop floor staff. We have presented live process defect clinics at exhibitions all over the world. Many of our Defect of the Month videos are available online at youtube.com/user/mrbobwillis. Find out how you can share our new series of Defect of the Month videos to explain some of the dos and don'ts with your customers via CIRCUITS ASSEMBLY: https://bit.

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FIGURE 1. Solder mask residues.

Seeing is Believing, continued from pg. 42

assembly at the customer

■ Inclusion of components not robust enough for the design.

Once a root cause has been identified, the field engineering team works with the customer to eliminate the condition that caused it.

In the case of no-fault-found units, the team will send it back to the customer's line for another test. If the unit continues to test bad on the line and good in the manual functional test, the line's testers are evaluated for software or fixture issues.

If no production handling or component issues are identified in PCBAs that tested good prior to leaving SigmaTron's factory but now fail all tests at the customer's factory, shipment, packaging or design may be evaluated.

In the case of design issues, the team may suggest a shortterm fix while an engineering change is in development.

Should the issue be component- or EMS-production-related, the team works with suppliers or the associated SigmaTron factory to correct that root cause, and Lean Six Sigma teams within purchasing or the factory may be involved in the corrective action process.

The result is both improvement in quality and cost. While the actual PCBA RMA numbers are relatively small, the analysis process corrects otherwise hard-to-identify issues that would likely continue to cause defects. Most important, this collaborative approach helps the EMS and customer teams develop closer working relationships that can contribute to a focus on eliminating inefficiencies in the product realization process.

ESHELF

MACHINES	MATERIALS	TOOLS	SYSTEMS	SOFTWARE

OTHERS OF NOTE

HIROSE TF43SW FLEX CONNECTOR

TF43SW series hybrid flexible printed circuit/flat flexible connector has power contacts capable of handling 12A and 0.5A signal contacts. Is 1.2mm high with 4mm mounting depth. For use with FPC/ FFC standard thickness of 0.3mm (+/-0.03mm). Has 66 contacts with 0.5mm pitch and length of 47.88mm. Retention tabs prevent unintended actuator separation.

KICAD 5.1.12 EDA SOFTWARE

KiCad 5.1.12 contains bug fixes and other minor improvements. Fixed bugs since 5.1.10 can be found on KiCad 5.1.11 milestone page. Is made from 5.1 branch with cherry-picked changes from development branch. Packages for Windows, macOS, and Linux available or will be soon.

TECHNIC TECHNIPAD IS 7070

TechniPad IS 7070 nitrate-free immersion silver, for 5G applications, replaces silver nitrate with silver complex. Process provides controlled deposition of thin, pore-free silver without aggressive copper attack. Is half thickness of nitratebased immersion silver.

Hirose hirose.com

ROHM LTR100L SHUNT RESISTORS

LTR100L series have power of 4W in 3264 size (3.2mm x 6.4mm)/1225 size (0.12" x 0.25") by revising resistor materials and applying terminal temp. derating. For current detection in motor control and overcurrent protection circuits for industrial and consumer applications. Come in $10m\Omega$, $47m\Omega$, and $91m\Omega$ versions.

KiCad

kicad.org

UCAMCO FAULTSTATION V2021.09 ET SOFTWARE

FaultStation v2021.09 electrical test software loads new error code types and assists in diagnosing faults. Provides improved views for assistance in faultfinding process. Upgrades include Testpoint view windows; handling of new error types produced by ATG and Gardien machines; support for L and M log files and barcodes.

Technic

technic.com

VISHAY IHVR-4025JZ-3Z VERTICAL-MOUNT INDUCTOR

IHVR-4025JZ-3Z comes in 10.25mm x 6.4mm x 10mm 4025 case size. Optimizes inductance and minimizes DCR for increased efficiency in DC/DC converters. Offers temp. operation up to +155°C for computer, server, telecom, and industrial applications. Uses airflow while reportedly enabling 50% lower DCR down to 0.130mΩ and higher rated current up to 112A.

Rohm Semiconductor

rohm.com

Ucamco	
ucamco.con	n

Vishay

vishay.com





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EUROPLACER INTELLIGENT FREE-FORM FEEDER

Intelligent freeform feeder is alternative to taping loose components. Eliminates one process step and reduces possibility of human error. Comprises pair of trays, each featuring nine separate cells to hold different components. These are dropped into 25mm x 18mm cells without need for orientation or alignment.



VISION ENGINEERING VE CAM DIGITAL MICROSCOPE

VE Cam compact digital microscope comes in two variants with differing fields of view: VE Cam 50 (50mm FOV) and VE Cam 80 (80mm FOV). Includes features available on EVO Cam II. Is standalone and doesn't require PC, keyboard or mouse. With Wi-Fi screen sharing, results can be shared wirelessly to smart devices and displays with screen mirroring. Features 10 user-programmable presets and six hotkeys for one-touch access to most commonly used presets and configurable interface, which allows most commonly used settings to be shown on the screen. Is for PCB examination, PCB debug activities, discovering imperfections, and to trace problems in industrial applications.



FUJIPOLY SARCON SPG-70A TIM

Sarcon SPG-70A thermal interface material is a high flow rate, high heat transferring compound that exhibits a thermal conductivity of 7.0W/m°K and has lowest thermal resistance among Fujipoly's dispensable SPG products. When applied between heat-generating components and nearby heat sink or spreader, it fills gaps as small as 0.2mm. Has excellent vibration absorption capabilities and requires no heat curing. Comes in 30cc syringes or 325cc cartridges.

Vision Engineering

visioneng.com

Europlacer

europlacer.com

OTHERS OF NOTE

INDIUM CW-305 FLUX-CORED WIRE

CW-305 halogen-free flux-cored wire permits post-soldering residue removal with warm water wash. Residue removal reportedly can be delayed up to 48 hr. without affecting ionic cleanliness or visual PCB appearance. For handsoldering applications where high flux strength and ability to clean with water are required.

MARVIN TEST SOLUTIONS ATEASY 2021 TEST SOFTWARE

ATEasy 2021 automates test and evaluation of components, boards, subassemblies and systems. Supports 64-bit software components. Revamped integrated development environment UI and code editor updates, including beautify code, parameter suggestion, and auto-completion improvements. Is 100% backward compatible with all previous versions.

ADVANTEST T5221 MEMORY TESTER

T5221 performs high-throughput functional testing of NAND flash devices with accurate timing, repeatability and failure detection. Data transfer speeds more than five times faster than predecessor; improves production efficiencies for wafer sorting, built-in self-testing and wafer-level burn-in. Optimized for use with a multi-wafer prober.

Indium Corp.

indium.com

TRIO MOTION SCARA ROBOTS

SCARA robots provide high-performance robot control, motion control, and machine automation from single controller. Designed for pick-and-place, assembly and dispensing. Four robots extend from 400mm arm range and 3kg max. load capacity to 700mm arm range and 6kg max. load capacity. Individual servo motors for high cyclic throughput and repeatable precision.

Trio Motion Technology triomotion.uk Marvin Test Solutions marvintest.com

Goepel Electronic

goepel.com/en

GOEPEL FLEX LINE 3-D AXI

Flex Line 3-D inline x-ray has variable belt conveyor that can transport small/ light and large/heavy assemblies. Is built around fixed position DUT image acquisition technology; provides image data without blurring during 2-D, 2.5-D and 3-D x-ray inspection. Granite-based six-axis system implements high-speed movement of image acquisition components with repeatability. Handles DUT up to 610mm x 508mm with max. weight of 15kg.

Advantest

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Fujipoly America

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WISCONSIN SMALL BATCH OVEN

Electrically heated small batch oven is used for curing coating on aluminum parts at 65°C to 70°C. Has max. temp. of 500°F. Normal op. temp. is 185°F. Chamber dimensions are 4' x 3' x 4'. Body is constructed with efficiency panel seams.

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In Case You Missed It

Artificial Intelligence

"APOLLO: An Automated Power Modeling Framework for Runtime Power Introspection in High-Volume Commercial Microprocessors"

Authors: Zhiyao Xie, et al.

Abstract: Computer engineers at Duke University have developed a new AI method for accurately predicting the power consumption of any type of computer processor more than a trillion times per second, while barely using any computational power itself. Dubbed APOLLO, the technique has been validated on real-world, high-performance microprocessors and could help improve the efficiency and inform the development of new microprocessors. (MICRO-54: 54th Annual IEEE/ACM International Symposium on Microarchitecture, 2021, https://dl.acm.org/doi/10.1145/3466752.3480064)

Assembly Materials Reliability

"Reliability Analysis of SnAgCu Lead-Free Solder Thermal Interface Materials in Microelectronics"

Authors: Mathias Ekpu

Abstract: Thermal interface materials (TIMs) are used in electronic devices to bridge the topologies that exist between a heat sink and the flip-chip assembly. Therefore, this study aims to investigate the reliability of SAC 405 and SAC 396 solder alloys in a microelectronics assembly. In this paper, SAC 405 and SAC 396 were used as the TIMs. The model, which comprises the chip, TIM and heat sink base, was developed with Ansys finite element analysis software and simulated under a thermal cycling load of between -40° and 85°C. The results were based on the total deformation, stress, strain and fatigue life of the lead-free solder materials. The analyses of the results showed SAC 405 is more reliable than SAC 396. This was evident in the fatigue-life analysis, where it was predicted it took about 85 days for SAC 405 to fail, whereas it took about 13 days for SAC 396 to fail. Therefore, SAC 405 is recommended as the TIM of choice compared to SAC 396. (Soldering & Surface Mount Technology, October 2021, www.emerald.com/insight/content/ doi/10.1108/SSMT-07-2020-0033/full/html)

This column provides abstracts from recent industry conferences and company white papers. Our goal is to provide an added opportunity for readers to keep abreast of technology and business trends. "Influence of Pad Surface Finish on the Microstructure Evolution and Intermetallic Compound Growth in Homogeneous Sn-Bi and Sn-Bi-Ag Solder Interconnects"

Authors: Yaohui Fan, et al.

Abstract: Low reflow temperature solder interconnect technology based on SnBi alloys is being considered as an alternative for SnAgCu (SAC) solder alloys to form solder interconnects at significantly lower melting temperatures than required for SAC alloys.

Microstructural evolution after reflow and aging, especially of intermetallic compound (IMC) growth at solder/pad surface finish interfaces, is important to understanding fatigue life and crack paths in the solder joints. This study describes intermetallic growth in homogeneous solder joints of SnBi eutectic alloy and SnBiAg alloys formed with electroless nickel-immersion gold (ENIG) and Cu-organic surface protection (Cu-OSP) surface finishes. Experimental observations revealed that, during solid state annealing following reflow, the 50nm Au from the ENIG surface finish catalyzed rapid (Ni,Au)Sn₄ intermetallic growth at the Ni-solder interface in both Sn-Bi and SnBiAg homogeneous joints, which led to significant solder joint embrittlement during fatigue testing. Intermetallic growth of (Ni,Au)Sn4 was decreased by Ag alloying of eutectic SnBi solder and was completely eliminated by changing the metallization from ENIG to Cu-OSP on the board side of the assembly. The reduction in (Ni,Au)Sn₄ growth rate with Ag additions is attributed to changes in grain boundary wetting of the IMC by Bi with Ag alloying. (Journal of Electronic Materials, October 2021; https://link.springer.com/ article/10.1007/s11664-021-09256-1)

Others of Note

University of British Columbia researchers have created what could be the first battery that is both flexible and washable. In addition to watches and patches for measuring vital signs, the battery might also be integrated with clothing that can actively change color or temperature. (www.sciencedaily.com/ releases/2021/12/211209095637.htm)

Facebook revealed a haptic glove designed to give the wearer sensations that mimic the weight and feel of real objects when they are handled in virtual space. Slip on this glove, and you can be convinced you're holding the real thing (or something close to it), even when the object is entirely digital. (www.wired.com/ story/facebook-haptic-gloves-vr/)

Washington University (St. Louis) researchers have designed a new processing-in-memory (PIM) circuit that brings the flexibility of neural networks to bear on PIM computing. The circuit has the potential to increase PIM computing's performance by orders of magnitude beyond its current theoretical capabilities. (www.sciencedaily.com/ releases/2021/12/211209082557.htm)



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