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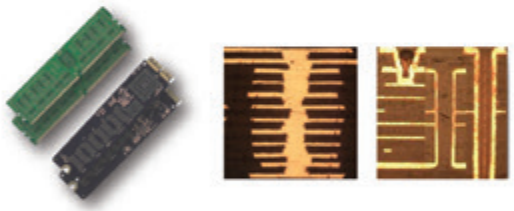
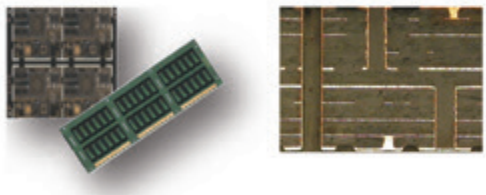
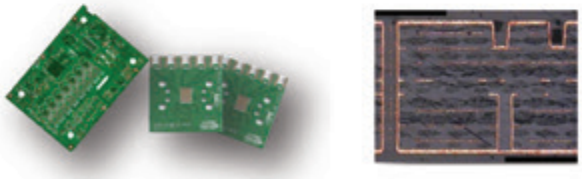


IOT / Build-up Board



Semiconductor TEST B'd
& 5G Network System



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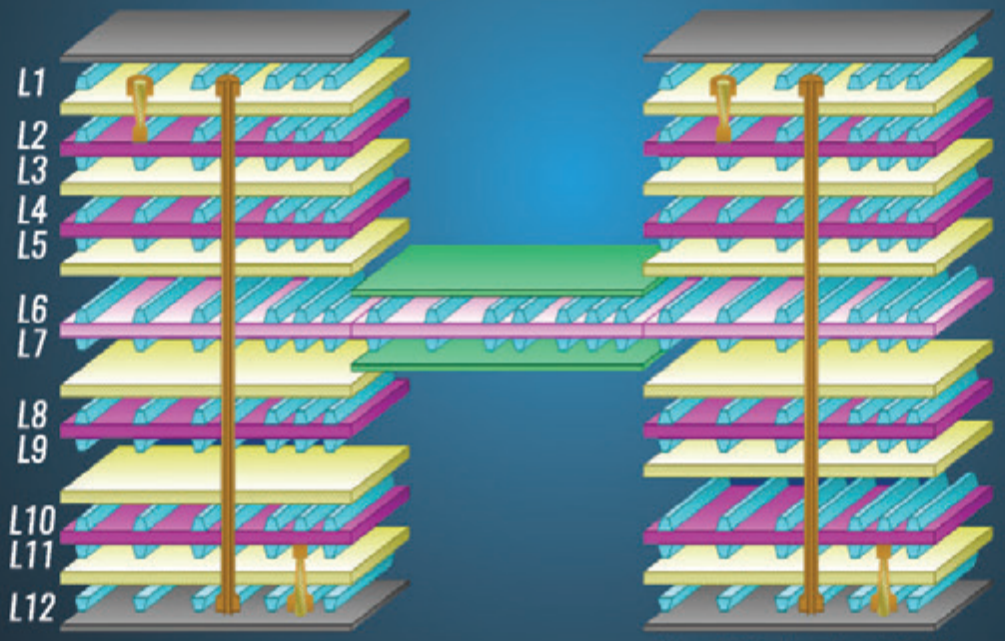

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MIKE BUETOW
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Content is King

WHY DOES SIEMENS want a content company?

In an era where new packages are coming online quickly, and the number of parts available is staggering – major original component manufacturers can have more than 100,000 items on their line card – human management of all this takes supernatural powers.

And that begins to explain why Siemens is paying $700 million (what?!?) for Supplyframe and its platform for component data, sourcing, and trends.

Indeed, the real value Supplyframe brings is not just access to spec sheets and parametric data, but real-time data trends. What's available? What's ramping in demand? And for how long? Supplyframe says it can aggregate use patterns across its 10 million-engineer-strong database to determine answers to these and related questions. It can also drill down by sector and geography to ascertain which components are ramping or stagnating in demand. There's obvious value in that. That scale is impressive.

Now, one could argue that even real-time data are reactive, whereas what the supply chain needs is predictive, as in forward-looking. No word as to the degree Supplyframe customers have been bowed by the intense and building pressure on component inventories over the past nine months. We'd like to know.

But for design engineers, there's unquestionable value in being able to access all these data in their preferred CAD environment. To that end, Siemens has already moved to add Supplyframe data to its Xpedition and Pads Pro lines.

As a review of the relatively recent history shows, ECAD companies have long known this, as the battle for content ownership has been ongoing for years. Almost a decade before being bought by Siemens, Mentor purchased PCB Matrix, previously known as PCB Libraries, which focused on land pattern calculators and library generation. In the era of Big Data, that move seems almost pedestrian in hindsight.

In 2015 Altium bought Octopart, significantly upping the ante due to the latter's integrated sourcing capability. In 2016, EMA, the primary distributor of Cadence's ORCAD tools, acquired Accelerated Designs.

Those all were smaller acquisitions. By snatching up the notably larger Supplyframe, Siemens has considerably raised the stakes. (The deal is set to close this quarter.)

Your serve, ECAD industry.

Whither Altium. The ECAD space continues to be interesting. Autodesk's bid for Altium in June – declined so far – took me by surprise. In retrospect, it probably shouldn't have.

As I've noted many times, I fully expect Altium to be acquired. It's just I was looking more in the direction of Dassault and PTC. I should have kept Autodesk in my field of view, especially after it acquired Eagle five years ago. Perhaps I was lulled to sleep, as that was a small acquisition, and Autodesk hasn't made much of a push since to burrow into the ECAD space.

The proposal was hefty, valuing Altium at $3.91 billion. That's not much lower than Siemens paid for the considerably larger and more profitable Mentor Graphics in 2017. Yet Altium thinks it can do better.

It just might. Autodesk's bid prices each Altium share at AU$38.50, a 41.5% premium over Altium's closing price on Jun. 4 and a premium of over 47.4% to the one-month volume-weighted average price. Prior to the offering, however, Altium's stock had peaked at a 52-week high of AU$39.34 last October. At $38.50, Autodesk was actually underbidding a bit.

An Autodesk-Altium merger wouldn't immediately change the face of the ECAD industry. Altium would still run neck and neck with Zuken for third place in revenues behind Cadence and Mentor, but it would give Altium the backing of an industry leader in 3-D CAD, and accelerate the inevitable MCAD-ECAD merger.

Passings. On a sad note, Intercept founder Steve Klare passed away in June. The company in the 1990s had some promising tech, especially for RF, but couldn't muster the scale needed, and rejected acquisition attempts. It's been essentially nonexistent in the market for most of the past decade. Still, if you believe like we do that innovation moves fastest in a crowded market, the loss of a company – not to mention a genius engineer – is always a sad day.

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@mikebuetow

P.S. By the time you read this, Printed Circuit University, our online education platform, featuring tutorials on a range of printed circuit design, fabrication and assembly matters, will be live. Take a look at printedcircuituniversity.com. You may recognize many of the instructors from our PCB East and PCB West conferences. Registration for the latter, which takes place in October at the Santa Clara Convention Center, is now open at pcbwest.com. Check out the program beginning on page 17.

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PCDF People

L3Harris named **Michael Ingham** associate manager PCB design.

Intercept Technology founder **Steve Klare** has passed away.

Microcraft named **Garrett Harding** North American sales manager.

PCDF Briefs

CCI Canadian Circuits installed a **Schmoll** Modul drilling/routing system.

Denkai America plans to expand its electrodeposited copper foil operations in South Carolina with a $14 million investment that will create 10 new jobs.

Element Solutions has made a binding offer to acquire **Coventya Holding** in an all-cash deal of €420 million (US$509 million).

EnviroLeach Technologies said continued research and development of its patented gold recovery technologies has resulted in improved efficiencies and significantly reduced reagent costs.

Factories in the Guangdong Province manufacturing hub were told by power suppliers to cut electricity usage by curbing operations, as rising power consumption amid hot weather strains the region's power system.

Fortify and **Rogers** announced a partnership to enable additive manufacturing of low-loss dielectric materials for RF devices and electronics.

Fujian Lanjian Group will build a PCB fabrication plant in the Dongtai Industrial Park in Fuzhou City, Fujian Province, China.

Isola has completed the final phase of construction of its 118,000 sq. ft. facility in Chandler, AZ.

Kunshan Dongwei Technology, a maker of PCB electroplating equipment, begins trading on the Shanghai stock exchange STAR market on Jun. 16.

MKS Instruments has made an offer to acquire **Atotech,** Reuters reported in mid-June, citing confidential sources.

Rogers filed patent infringement proceedings in Germany through a subsidiary against **KCC** and its German subsidiary alleging infringement of certain Rogers' patents relating to direct bonded copper substrate materials.

Schweitzer Engineering Laboratories in June broke ground on what will be a 140,000 sq. ft. printed circuit board factory in Moscow, ID.

Siemens' Deal for Supplyframe Has Immediate ECAD Implications

MUNICH – As buyers worldwide scrambled for hard-to-find components amid rising order books, Siemens in May showed its hand: a $700 million deal to acquire Supplyframe. The acquisition, which is expected to close in the current quarter, gives the OEM a leg up in offering a comprehensive path for engineers and buyers to source and design-in parts with the benefit of real-time knowledge of use trends – and possible shortages.

But while Siemens ultimately plans to apply Supplyframe's platform across a range of markets and domains, it first plans to tackle EDA integration, incorporating certain Supplyframe technologies into its PCB design flows. In doing so, Siemens said, it will offer its PCB designers real-time visibility into global supply chains and other functionalities, aiding everything from schematic design to factory floor manufacturing.

A.J. Incorvaia, senior vice president of the Electronic Board Systems, Siemens Digital Industries Software (DIS), and Richard Barnett, chief marketing officer for Supplyframe, spoke about the planned integration with PCD&F/CIRCUITS ASSEMBLY in June.

AJ Incorvaia

Richard Barnett

As anyone who has looked up from their comic book knows by now, supply-chain matters are front and center. Therein lies much of Supplyframe's value, the company says, because it helps customers mitigate inventory and related issues. Supplyframe was founded in 2003 to drive decision-making capability among product engineers and the rest of the sourcing and supply chain. Its founders came from the distribution side. "We have a unique business model because we help component suppliers and distributors transform their digital go-to-market and also help the end-customers, such as EMS and global OEMs, to drive greater intelligence in the decisions they are making, for strategic sourcing and supply chain," Barnett said.

Supplyframe does this both through its internal component sourcing database and by scraping others. Component data, for instance, comes from IHS Markit, and parametric data from suppliers. "We have 180 APIs (application programming interfaces) with every major distributor globally for real-time data, and look at engineer component search data by industry and geography to get additional metadata," Barnett said.

Through its acquisition of Mentor, Siemens has chip design and analysis, board design and analysis, manufacturing controls and throughput tools, such as digital twin software. The synergies in the latest deal, says Incorvaia, lie in helping companies understand the right productions, pricing, and so forth. And while the major EDA companies have historic partnerships with various third-party design content providers – and in some cases, have purchased those companies for themselves – the amalgamation of Siemens and Supplyframe has the potential to significantly expand that position.

"This has impacts on both the buy and sell side," he said. "For component manufacturers, it ensures they provide their customers with the right parts at the right time, and it helps the design side ensure they are optimizing their bills of materials."

He noted Siemens is already using Supplyframe's technology with Siemens' circuit board design tools to provide customers with information to streamline the product development cycle.

Supplyframe claims access to some 10 million engineers worldwide. The existing Supplyframe customer relationship agreements are not expected to constrain the ability of Siemens to market its other tools directly to those prospects. Still, notes Incorvaia, Siemens' HyperLynx and Valor tools already work in third-party flows.

Great designs require more than good tools.

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CA People

Alternative Manufacturing named **Jim Barry** vice president, sales and marketing. He has held top executive roles with Strataflex, Eltek USA, and other manufacturing companies over more than 30 years in the industry.

August Electronics announced **Paul Crawford** as chief executive.

BTU International promoted **Rob DiMatteo** (top left) to general manager, and BTU promoted **Bob Bouchard** to director of sales – Americas. DiMatteo has close to 30 years of experience in sales management, customer support and product development and has extensive knowledge of BTU's customer base and end markets, including SMT and high-temperature applications. Bouchard has more than 25 years of related experience, most recently leading BTU's marketing team and previously in process engineering.

Innovatech Associates named **Jacqueline Chase** senior sales manager.

Computrol appointed **Michael Fric** process engineer and **Rose Scott** A&E manager.

Flex promoted **Doug Watson** to rework process engineering manager.

ICAPE promoted **Kathy Mazet** to chief operating officer.

Indium named **Michael McNamara** director – operations general manager engineered solder materials & EHS.

Libra Industries appointed **Paul Bore** to senior director of operations and lead of the EMS company's Precision Machining Center.

Libra Industries named **Andrew Williams** senior vice president of business development. He has more 30 years' experience in business development in contract manufacturing, including executive positions at Jabil, Sanmina and Kimball Electronics.

National Circuit Assembly hired **Steve Abeyta** as senior account manager. He has more than 20 years' experience in contract manufacturing, in the factory, supply chain management, sales, quoting, and quality control.

Virtex named **John Karskosi** business development manager.

"We won't want to be only in those internal flows … customers are going to mix and match various tools and Supplyframe fits very nicely."

Siemens is already at work embedding Supplyframe's component data into its Xpedition and Pads Pro ECAD as a plug-in. That data include real-time access to pricing, availability, compliance and lifecycle directly accessible from schematic capture or layout, plus links to component supplier datasheets.

"That gives designers the ability as they are creating the schematic to assess the risks of that part, the pricing, the availability," said Incorvaia. "As you saw with Siemens' NX and TeamCenter integrations, we will have as much of that tech as we can bring to an engineers' fingertips, so they can make use of it in their own design environment without leaving that design environment. Users won't need to learn a new UI.

"This integration is close to market, [and] we anticipate there will be a number of synergy projects" going forward, Incorvaia said. He added he thinks the deal will enhance Siemens' existing relationship with Digikey.

Incorvaia deferred on the question of how much of a premium Siemens ECAD or Valor customers will pay for access to the Supplyframe data. He said Supplyframe will operate as a standalone business segment inside Siemens DIS, with chief executive Steve Flagg reporting to Siemens DIS CEO Tony Hemmelgarn. "We tend to keep acquisitions as standalone entities, although there will be a close tie to the existing companies. Like with Mentor, we keep the business segments the same," he explained.

It appears Siemens is pushing toward an all-in-one software solution. One question, then, is this: Is that what customers want? Or will there be market pushback because certain customers don't want to be overly dependent on any single supplier? Incorvaia believes product development has grown so complex, it screams for a finely-tuned integrated solution.

"What we are finding is the problems are getting so large, as customers go through this digital transformation, where they have to worry about product complexity and ensure the software they have is the latest version and works with the other latest versions, making sure they can acquire the parts they need and move seamlessly into manufacturing. These problems are becoming so large, customers are looking for a partner that can help them uniquely solve their problems. Sometimes customers have manufacturing that's in-house; sometimes it's external; sometimes there are specific regulatory requirements they can meet …. They want a partner that can help them through the entire development process, not just the electronics. They have to worry about the mechanical, lifecycle, and electronics early on when spec'ing the product that the architecture can last, and they are meeting the initial requirements. They are looking for a vendor that can help them solve that entire problem. We see customers coming to us looking for a partner, versus looking to build a flow of best-in-class tools."

"We see the same patterns," Barnett added. "There's really a shift in leadership with these people who experienced the global chip shortage, who are looking for ways to drive greater intelligence to mitigate the impact to a longer-term root cause. It's challenging for a lot of these organizations."

Can we reach the point where component analysis might be shared company to company, even anonymously? Barnett thinks it depends on how component analysis is defined, but adds that third-party validation is already how peer communities are learning and testing their design strategies. "Leading component suppliers are trying to engage design engineers with the right content at the right time. Also, sharing the supply market context for component parts and tracing the digital twin from design through manufacturing is now a critical dimension of key part selection decisions such as, 'How do I design in alternate suppliers or components, so I am empowering my CM to work within that BoM and adjust to supply market conditions?' Those are the things we think about when we try to tie component design and use."

Both sides point to potential to expand well beyond electronics into areas both larger (mechanical) and faster-growing (additive). "We feel that the Supplyframe technology can help Siemens with our marketplace strategy. We believe that in the future

the infrastructure and technology that Supplyframe has can be used in other areas, for example, mechanical design and additive manufacturing," Incorvaia said.

"We ask, 'How do you derive greater intelligence from design to sourcing?' " said Barnett. "And on a global basis, we consider the context of new design cycles, and develop SaaS solutions for component suppliers and distributors on the sell side and sourcing agents on the buy side. Our Direct-to-Source Intelligence network includes lots of different properties in different areas. Moving into mechanical is even bigger than just EDA." (MB)

AT&S to Open 1st SE Asia Production Plant

LEOBEN, AUSTRIA – AT&S will invest RM8.5 billion (US$2.1 billion) to open its first production plant in Southeast Asia. The new campus in Kedah, Malaysia, will produce high-end printed circuit boards and IC substrates, creating some 5,000 jobs.

Construction at the Kulim Hi-Tech Park is scheduled to begin in the second half of 2021. Commercial operations are targeted for 2024.

"After very intensive location scouting globally, Malaysia has emerged as the country in which we want to push ahead with our More than AT&S strategy," said AT&S CEO Andreas Gerstenmayer. "AT&S brings the latest generation of high-end technologies to the country and builds up a completely new technology sector. Besides manufacturing high-tech products, a significant amount of R&D activities will be executed at this new location. Malaysia can benefit its position as a technology country and can strengthen the region as a high-tech manufacturing hub in Asia." (CD)

Summit Interconnect Acquires Eagle Electronics

ANAHEIM, CA – Summit Interconnect continued its acquisition run in June with the purchase of Schaumburg, IL-based printed circuit board fabricator Eagle Electronics. The acquisition provides a significant and targeted expansion into the high-performance, quick-turn commercial prototyping market and extends Summit's operational footprint into the Midwest US, Summit said in announcing the deal.

Eagle's management team will stay in place, Summit told PCD&F. No financial terms were disclosed.

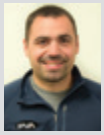
In a press release, Shane Whiteside, president and CEO, Summit Interconnect, said, "Eagle is an impressive operation with an experienced and highly capable management team. The acquisition aligns Eagle's extensive prototyping experience and commercial market reach with Summit's differentiated production capabilities. We are particularly impressed with their consistent investments in advanced technology capability, resulting in an equipment set that closely resembles our other Summit factories. The new capabilities that Eagle brings will further strengthen our ability to serve our customers in both high-performance commercial and defense markets, as well as broaden our relationships with key suppliers."

Eagle was founded in 1979 and provides advanced prototype printed circuit boards to the industrial, communications, medical, automotive and military markets. Its 50,000 sq. ft. plant in the Chicago suburbs is ISO 9001:2015, U.L. and ITAR certified.

Summit is the second-largest PCB fabricator in North America in terms of onshore revenue. (CD)

Fralock Buys Flex Circuit Maker Lenthor

VALENCIA, CA – Fralock Holdings in late May announced the acquisition of Lenthor Engineering, a privately owned manufacturer of flex and rigid-flex printed circuits.



PVA promoted **Kyle Mackenzie** to director of manufacturing. During his nearly 15-year tenure with PVA, he started as an assembly technician and then worked as assistant director of manufacturing.

CA Briefs

AQS purchased a **Nordson X-ray** Assure x-ray component counter.

Bennett Pump purchased a **Kurtz Ersa** Versaflow 3/35 wave soldering oven.

Bright Machines named **Restronics** manufacturers' representative in New York, New Jersey, Florida, and the Southeast US.

Computrol implemented the **Insituware** Vision MARK-1 handheld diagnostic tool.

Deswell acquired two **Panasonic** SMT placement systems and two **HaiTian** new generation 800 tons injection molding machines.

Dynamic Source Manufacturing selected a **Mirtec** MV-6 Omni AOI.

Edison Partners announced leading a $15 million growth capital investment in **MacroFab,** an investment that includes funding from **Altium.**

Essemtec named **Advanced Process Technologies (APT)** manufacturers' representative in Puerto Rico.

Foxconn is in talks to buy a stake in **Dagang NeXchange.** It also has struck a multibillion-dollar electric-vehicle partnership with **PTT** in Thailand, and is partnering with **Formosa Plastics** on EV manufacturing.

GYS installed a **BTU** Pyramax 100A reflow oven.

Infinitum Electric will double its roughly 30-person workforce during the next six months after obtaining $40 million in new funding for electric motor design, which uses PCBs to replace the iron and copper components.

Intel's CEO said it could take several years for a global shortage of semiconductors to be resolved, a problem that has shuttered some auto production lines and is also being felt in other areas, including consumer electronics.

Javad EMS has incorporated the **MODI** Incoming Goods Scanner into its process.

JEDEC established JEP181, a neutral file, XML-based standard for electronics cooling simulation for the microelectronics industry.

continued on pg. 44

Terms of the deal, which was financed by Arsenal Capital Partners, were not disclosed.

Lenthor provides design, fabrication and assembly services to the defense and aerospace, medical device, industrial, telecom, and semiconductor industries.

"Lenthor's advanced capabilities in flexible circuit design and manufacturing, and its leading position in high-value market segments make it a perfect complement to Fralock's core business," said Marc Haugen, CEO, Fralock. "We believe that Lenthor's expertise and strong executive team, as well as its strong strategic customer relationships, especially in our overlapping market segments, makes Lenthor an excellent addition to our expanding engineered materials solutions platform."

Fralock's applications are used in a variety of ways that impact our lives, including equipment used to manufacture semiconductors, medical treatment, imaging and patient monitoring devices, and defense applications, satellite and spacecraft components. The acquisition will enable Fralock to expand its market position and better serve its existing end-markets from the products created by Lenthor, the companies said in a press release.

Lenthor has more than 160 employees and is the third-largest flex circuit manufacturer in the US.

Established in 1967, Fralock Holdings is a design, engineering and manufacturing company serving the aerospace, defense, medical, life science, semiconductor and other high-reliability markets. Its companies include Fralock, Career Technologies USA, Mapson Engineering, Oasis Materials, Oasis Precision, Stratemet and Ceramic Tech. (MB)

Annual CIRCUITS ASSEMBLY EMS Awards Program Opens – with a Twist

ATLANTA – CIRCUITS ASSEMBLY has opened free registration for its annual Service Excellence Awards (SEAs) for electronics manufacturing services (EMS) providers.

Now in its 30th year, the SEAs honor companies in contract electronics manufacturing for excelling in the critical area of customer service. This year, winners will be determined through an industry-wide voting process.

The SEAs recognize four categories of EMS providers based on revenues: under $20 million; $20 million to $100 million; $101 million to $500 million; and over $500 million.

CIRCUITS ASSEMBLY will honor winners during a virtual ceremony in February 2022.

"There are literally thousands of EMS companies in the world, making it an industry at once highly competitive and difficult to create differentiation," said Mike Buetow, editor in chief of CIRCUITS ASSEMBLY. "The SEAs are a golden opportunity for the best-in-class assemblers to separate themselves from their competitors, using the endorsement of their own customers as the differentiator."

For more information visit circuitsassembly.com/ca/editorial/service-excellence-award.html. To register for free, visit surveymonkey.com/r/8TCZN57.

The deadline to register is Aug. 13, 2021. (CD)

Note Acquires iPro in UK, Extends Greentech Thrust

STOCKHOLM – Note in June acquired all shares in UK-based iPro Holdings, a box-build manufacturer of electronics-based products for greentech, medtech and industrial uses.

Note will pay GBP 7 million ($9.92 million) upfront in cash for iPro, a sum that could rise based on future performance. The price corresponds to an acquisition multiple of approximately 3.5 EBIT. Haddenham, Buckinghamshire, UK-based iPro has revenue of SEK 320 million ($38.7 million), employs 100 staff, and had an operating margin in line with Note's during the past 12 months.

Owner Martin Deas will continue as managing director.

In a press release, Note said the respective companies have similar business models based on long-term customer collaborations, high quality and strong delivery performance.

iPro is in a strong growth phase with several ongoing projects in the electric vehicle (EV) and e-mobility markets. The deal strengthens Note's growing position in greentech. The growth and profitability of iPro is developing positively, as a consequence of the high demand for charging products for electric vehicles, Note said.

The acquisition represents pro forma growth over the past 12 months of approximately 17% and an increase in operating profit (EBITA) of around 16%. Together with nearby plants in Windsor and Stonehouse, Note's sales in the UK amounted to just over SEK 500 million ($60.5 million) pro forma for the past 12 months.

"The size of the British EMS market is approximately at the same level as the entire Nordic market," says Johannes Lind-Widestam, CEO and president, Note. "We are very pleased to complete this acquisition, which significantly strengthens our position in the UK. The growth in iPro is strong, and the company has many exciting customers and new projects. We are already seeing a significant recovery in demand in the UK market as well and look forward to further develop the operations of iPRO together with current customers, staff and management." (MB)

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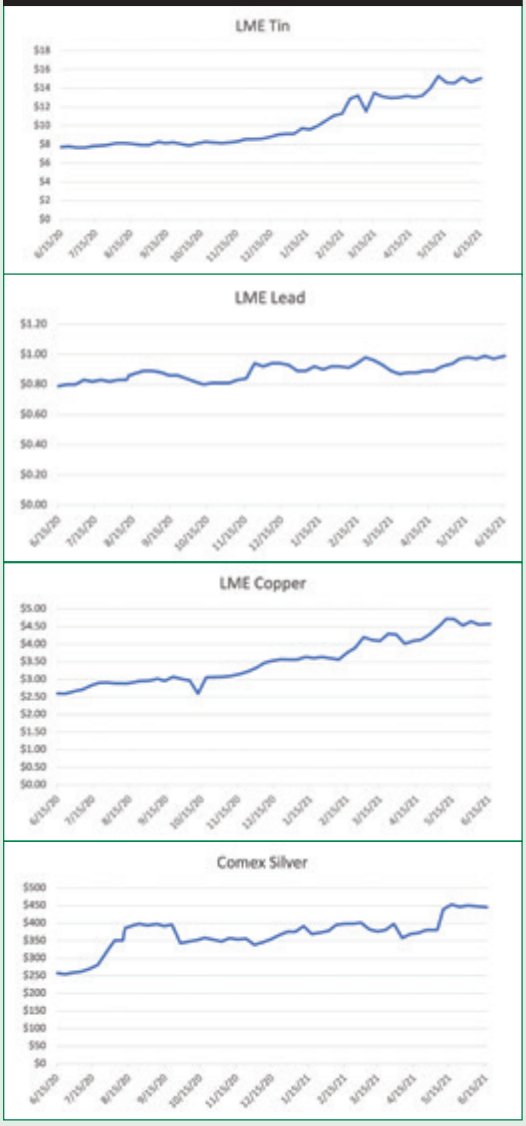

US MANUFACTURING INDICES

	JAN.	FEB.	MAR.	APR.	MAY
PMI	58.7	60.8	64.7	60.7	61.2
New orders	61.1	64.8	68.0	64.3	67.0
Production	60.7	63.2	68.1	62.5	58.5
Inventories	50.8	49.7	50.8	46.5	50.8
Customer inventories	33.1	32.5	29.9	28.4	28.0
Backlogs	59.7	64.0	67.5	68.2	70.6

Source: Institute for Supply Management, June 1, 2021

KEY COMPONENTS

	DEC.	JAN.	FEB.	MAR.	APR.
Semiconductor equipment billings[1]	7.6%	29.8%	32.4%	47.9%[r]	49.5%[p]
Semiconductors[2]	9.55%	13.2%	14.7%	17.8%[r]	21.7%[p]
PCBs[3] (North America)	1.10	1.14	1.29	1.22	1.16
Computers/electronic products[4]	5.11	5.12	5.20	5.18[r]	5.16[p]

Sources: [1]SEMI, [2]SIA (3-month moving average growth), [3]IPC, [4]Census Bureau, [p]preliminary, [r]revised

PACKING IT IN

Trends in the US electronics equipment market (shipments only)	% CHANGE FEB.	MAR.	APR.	YTD%
Computers and electronics products	-1.0	0.9	0.8	8.2
Computers	0.9	-3.1	0.3	2.6
Storage devices	2.6	0.9	7.5	27.0
Other peripheral equipment	-1.0	-5.1	11.6	15.8
Nondefense communications equipment	-1.4	0.9	-2.2	14.3
Defense communications equipment	0.9	-1.3	-4.4	4.7
A/V equipment	-10.7	-1.8	1.4	0.0
Components[1]	-0.8	0.7	-0.4	8.2
Nondefense search and navigation equipment	-4.3	-1.3	4.1	0.7
Defense search and navigation equipment	-2.6	0.2	1.7	2.6
Medical, measurement and control	-1.0	1.2	0.9	9.3

[r]Revised. *Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: U.S. Department of Commerce Census Bureau, June 4, 2021

Hot Takes

- **Taiwanese PCB makers** saw combined first quarter output value in Taiwan and China surge 27% year-over-year to NT$173.4 billion (US$6.1 billion). (TPCA)
- **Wearable device shipments** reached 105 million units in the March period, a 34% increase from a year ago and the first time first quarter shipments topped 100 million units. (IDC)
- **The electronics industry** saw strong production growth in 2020, and the first quarter 2021 was a record quarter compared to a year ago. Still, capital equipment spending is increasing, and growth should continue if shortages do not hold back the industry. (TechSearch International)
- **Semiconductor manufacturers** worldwide are on track to boost 200mm fab capacity by 950,000 wafers, or 17%, from 2020 through 2024, to reach a record high of 6.6 million wafers per month. (SEMI)
- **Three-month shipments by North American EMS companies** rose 11.5% year-over-year in April, falling 11.9% sequentially. Orders rose 22.6% year-over-year during the same period but decreased 14% from the previous month. (IPC)
- **PC shipments** are expected to grow 18% in 2021 to 357 million units. PC growth is expected to drop 2.9% in 2022, but the overall five-year CAGR remains positive at 3%. (IDC)
- After a steep drop in 2019, **memory IC sales** rebounded 15% in 2020, and stronger DRAM pricing is expected to lift total memory revenue 23% this year to $155 billion. From 2020 through 2025, the total memory market will grow at a CAGR of 10.6%. (IC Insights)
- **Worldwide smartphone shipments** are likely to reach 650 million units in the first half, and 1.32 billion for the year, up 6.4%. (Digitimes Research)
- **The worldwide semiconductor shortage** will last through this year and not recover to normal levels until the second quarter of 2022. (Gartner)

A Rising Inflation Tide Can Sink All Boats

The cycle of higher unemployment and prices must be broken.

I AM NOT an economist, but having been around the block more than a few times over the past decades, it sure looks like financial déja vu!

My career started in the mid-1970s. At that time, the economic arena was swirling from extraordinary events that, together, created the perfect storm for hyperinflation. The aftermath of the US political crisis Watergate, staggering gas lines and shortages caused by the rolling Middle East oil embargos, and questionable Federal Reserve tactics led us to double-digit inflation. At that time, I was pricing administrator for a division of a global electronic connector manufacturer. Among my responsibilities was keeping the multi-thousand-part price book up to date. This task historically was done once every one or two years. In the environment we were in, however, I was updating prices two to three times each year!

It's with this perspective I find myself trying to read the proverbial economic tea leaves of where we are headed in 2021 and beyond.

The past couple years, like in the mid-70s, have been filled with extraordinary events. Washington has been in gridlock; tariffs are finally resulting in shifts in where product is produced and shipped; a pandemic has displaced millions of workers and sent more home to work. Manufacturing facilities are reducing onsite staff, resulting in lower output and product shortages. Governments are responding with economic stimuli in the form of direct cash to citizens, enhanced unemployment benefits for those out of work, and low-cost loans to business and industry.

The common denominator in both eras is a series of extraordinary events that prompted society and especially government to react. With no playbook to follow, the responses might best be characterized as stabs in the dark, with the intent of thwarting the current crisis – hopefully while not creating another.

But many differences exist between then and now. Take technology, for instance. In the '70s great strides were taken to develop chips to advance the "integrated circuit." PCBs became the platform of choice and wire-to-wire circuits were replaced by through-hole technology. Software and firmware became linchpins to harness all electronics so they could be more readily available as useful tools.

More important was where these new technologies were applied. Apple introduced the first truly "personal" computer, touching off a race to bring phenomenal computing power to the masses. The vast majority of this technology was developed to make people more productive. Ledgers gave way to spreadsheets, which could be updated and manipulated far more easily than a person with a calculator or adding machine. Ditto word processing as it advanced from the typewriter to PC-based software. And databases could be created and stored on an individual desktop, not in the bowels of the IT department.

Back then technology increased worker productivity. The new technology was expensive; however, the higher cost was offset by increased productivity – a hallmark that our industry has been at the forefront of since its infancy. By increasing user productivity, technology contributed to ending hyperinflation. That's where the difference between then and now appears so pronounced. Much of the technology being developed today does not make people more efficient but instead cuts the cost of a task or process by replacing humans doing basic or even complex tasks with machines driven by artificial intelligence (AI).

The pandemic created high unemployment all while technology is being developed to reduce the need for employees, thus magnifying the number of people who are unemployed. If government one way or another steps in to subsidize the unemployed, providing the wherewithal for people to buy products, creating shortages, that's one of the causes of inflation. Inflation then raises the cost of hiring people, hence making AI more affordable, which displaces even more employees, and the spiral continues.

Virtually every industry is reporting price hikes at record rates, and those increases typically are well in the double digits. Industry colleagues I speak with now rate rising inflation as a concern on par with the inability to find competent employees, even when unemployment is at high levels. The problem is real, and if not dealt with wisely could mushroom into a prolonged period of high inflation.

What does this have to do with economics? Returning to the "normal" economic cadence in which people are working and factories are running is critical to avoid long-term high inflation. Hopefully, as the pandemic eases and society embraces a return to "normal," those on the employment sidelines, whether because of caution, fear or government incentives, will choose to join the job market and fill the many open positions. Filling the huge number of open job requisitions may enable capacities to increase and ease the shortages of critical materials and components – all of which may contribute to easing inflation. Conversely, if our current state continues, we may relive the era when prices increased double digits every year, and shortages were the norm rather than the exception. ▫

PETER BIGELOW
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Don't Let Perfection Be the Enemy of a Perfectly Good PCB

How well does your incoming inspection team know the acceptability standards?

DOES YOUR PCB quality team inspect to pass or inspect to fail? Knowing the difference between what is rejectable in a printed circuit board and what is a nonissue is more important than ever.

Skyrocketing costs, shortages of copper and fiberglass materials, and longer delivery times mean remakes are not available as quickly as before. Rejecting PCBs for things that don't affect the form, fit or function of the final project is simply bad business.

To be clear, I am not advocating acceptance of substandard product. IPC-A-600 standards are clear as to what is good and what is not. But thanks to lack of training or misinterpretation of industry specs, incoming PCB quality inspectors are turning away perfectly good commercial-grade boards that then must be remade.

The main culprit in this cycle of unnecessary PCB rejection and remake costs is management, which fails to provide adequate training to incoming inspectors and instills in them a fear of releasing bad product to the manufacturing floor.

At one high-mix EMS customer of mine, inspectors are so sensitive to any possible issue, they routinely send rejection notices over even the slightest blemish in the solder mask. This leads to a lot of time spent on calls back and forth, then additional paperwork, and *then* a hefty freight bill for the remakes. In the end, the very same boards that were rejected are accepted, and a lot of time and money has been wasted.

Another one of my customers recently rejected a large, heavy PCB for a slight corner ding. The photos made the issue look worse than it was, and the impression given was the entire lot was affected. The boards were returned.

Of the 10 boxes returned, all but three had the original factory seal, meaning the product inside was never inspected. And of the three boxes that were inspected, only one package of boards had the issue for which the entire shipment was rejected. The dings were minor and, according to IPC, acceptable "as is." The PCBs were cleaned up, repackaged, and immediately returned. The request for the supplier corrective action was respectfully declined, citing the IPC specification that the boards were acceptable. The supplier offered to send the relevant specs to the customer, but the customer declined, saying it understood the specs. If the customer did indeed have a strong understanding of the specs, the boards would have never been returned in the first place, and UPS would not have become even richer than it already is.

No PCB fabricator wants to accept the return of boards unnecessarily, as I am sure no PCB assembler wants to delay its customer over a nonissue. The time, money and paperwork required to resolve a nonissue is a burden that can usually be resolved with a couple phone calls.

But that resolution can't happen without proper training. One owner of a PCB assembler told me he didn't "want an hourly employee releasing bad product to the floor, causing tens of thousands of dollars in scrap."

But by not giving that employee enough training to recognize the difference between a perfect PCB and a perfectly good one, the owner is likely costing his company even more in monthly revenue with boards that are needlessly scrapped, which prevents shipment of finished assemblies.

I've often seen an OEM overrule its EMS provider over a nonissue on a circuit board. Yes, OEMs want quality product, but they also want that quality product delivered on time. It looks bad for the EMS to cause delays that could have been prevented with additional training for inspectors.

How well does *your* incoming inspection team know the IPC "acceptability" standards? Those standards define what is an acceptable PCB that does not need to be rejected for minor flaws that do not affect the performance of the board. In other words, they are designed to prevent the perfect from becoming the enemy of the good.

Training sites around the world offer help to PCB inspectors to sharpen their ability to recognize nonconforming conditions. Many are tied to the IPC-A-600, "Acceptability of Printed Boards" certification program, which "describes the preferred, acceptable, and nonconforming conditions that are either externally or internally observable on printed boards." In addition, organizations such as SMTA and publications such as this one host informative seminars (both online and in-person) about what is acceptable and what is not.

And don't forget industry trade shows like PCB West (coming in October to the Silicon Valley). Plenty can be learned from industry experts on the acceptability issue.

Investing in additional training for incoming PCB inspectors is worth the time and money. Being able to make the proper call when a board issue presents itself will allow your operation to consistently produce quality product in a timely manner and make your company a trusted partner for its customers. ❑

GREG PAPANDREW has more than 25 years' experience selling PCBs directly for various fabricators and as founder of a leading distributor. He is cofounder of Better Board Buying (boardbuying.com); greg@boardbuying.com.

Component Placement is a Game of Compromises

Getting all the parts and processes aimed in the same direction.

PRINTED CIRCUIT BOARD technology never sleeps. At this very moment, engineering teams are working out ways to increase circuit density with finer-pitch devices. When it comes to placing these components on a PCB, the margin of error shrinks along with the pin pitch. Let's look at how we can enable these parts on the assembly line.

The first step in mass production of a PCB assembly is preparing the board to take components. The boards may be baked in an oven prior to starting the assembly process. Although they are packed in sealed containers with a little bag of desiccant, the sponge-like dielectric materials still absorb water one molecule at a time. Prebaking releases the steam that could interfere with reflow soldering.

Ideally, all parts on a board will use the same type of technology and will be roughly the same class of components in terms of pin-pitch and other physical aspects **(FIGURE 1)**. Tall and heavy components plus small and light ones are not a good mix. Tall ones create so-called shadows where the surrounding area doesn't get as hot during soldering.

Most component datasheets include instructions for soldering. There could be a suggested paste type specified down to the granularity of the particles. There will likely be a graph that shows the thermal profile that gives the best results. It starts with a preheat ramp-up to near-reflow temperature, then a spike into the soldering temperature, followed by a cooldown period. Overlaying all the thermal curves for the components on a particular board will show similar but not exact matches for the recommended process window.

Your assembly house has a sweet spot for yields. A perfect board for them has all components in the same orientation. They would all be surface mount and on the same side of the board. Components with hidden leads would be avoided or given extra space as a "courtyard" for a rework nozzle to make full contact with the board surface. It's more efficient if the assembler does not have to desolder a bunch of passive components, but some of them really want to be near a specific pin.

Fine-pitch components. Fine-pitch devices, if used, have a pair of local fiducial marks to permit the pick-and-place head to register its exact location for more accurate placement. These fiducials are in addition to board-level fiducials and could be shared among devices if there is symmetry among them. Ideally, every component faces the same cardinal direction with distinct and uniform polarity marks. The real world doesn't work that way, but it is a goal. In 30 years of PCB layouts, I have never once had all the caps and resistors in the same orientation, let alone all the polarized components. The idea is to get a feel for how the components want to be placed for the best performance and settle on one general direction that uses that angle whenever possible.

Now you have your nearly perfect layout with the board ready for assembly. The next step is solder paste application. Depositing solder paste on the PCB must be precise and repeatable. Smaller boards or those with intricate outlines will require an assembly subpanel.

Meanwhile, larger boards usually incorporate component-free zones along the edges for placement and soldering processes. Typically, we're looking at a 5mm-wide strip of component-free real estate along the longer edges of the board for the machines to grip. Tooling holes facilitate repeatable and unmistakable orientation for fabrication, stencil, pick-and-place, and test fixturing. Three alignment holes provide that kind of assurance.

Let's circle back to the boards, with an assembly subpanel in addition to the larger fabrication panel. Consider the orientation of the components before choosing which edges require assembly rails. Surface mount and through-hole components both have a preferred direction of travel through the soldering station. The main point is to prevent solder bridges and other defects, as we will cover next.

Passive components prefer to go through the oven broadside (sideways) to the process flow. This way, both pads see the same temperature profile at the same time. If one side reflows and solidifies before the other, there is a greater likelihood of defects like cold solder and disturbed solder. Cold solder has a dull finish and lacks the fillet that indicates proper wetting. Disturbed solder has irregular contours that suggest some movement of the component during the critical transition when solder changes from a liquid to a solid. Those are two defect classes that lead to latent defects, the worst kind of defect.

Improperly placed components could also lift from one of the pads like a drawbridge, which we call "tombstoning." I've had cases where ceramic and wire-wound components actually broke due to the stress of different thermal profiles. These defects occurred because one end of the capacitor/inductor was close to the edge of the board, while the other pin was inboard. The edges get much hotter, with the temperature rising and falling faster, while the board is

JOHN BURKHERT JR. is a career PCB designer experienced in military, telecom, consumer hardware and, lately, the automotive industry. Originally, he was an RF specialist but is compelled to flip the bit now and then to fill the need for high-speed digital design. He enjoys playing bass and racing bikes when he's not writing about or performing PCB layout. His column is produced by Cadence Design Systems and runs monthly.

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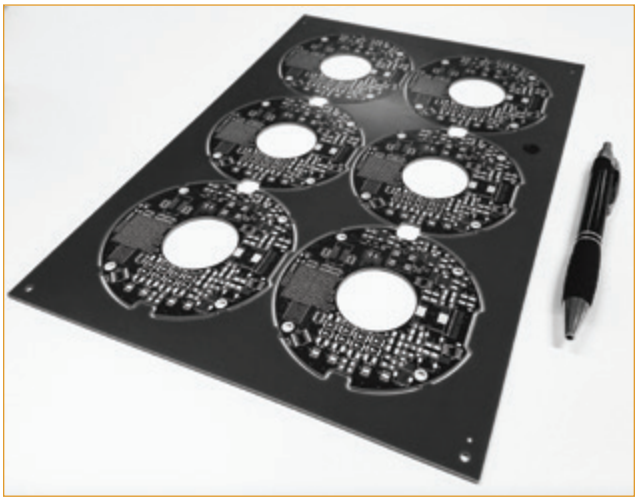

FIGURE 1. Board outlines determine how much of the material is lost for processing. Sticking with SMD components helps narrow the number of steps required.

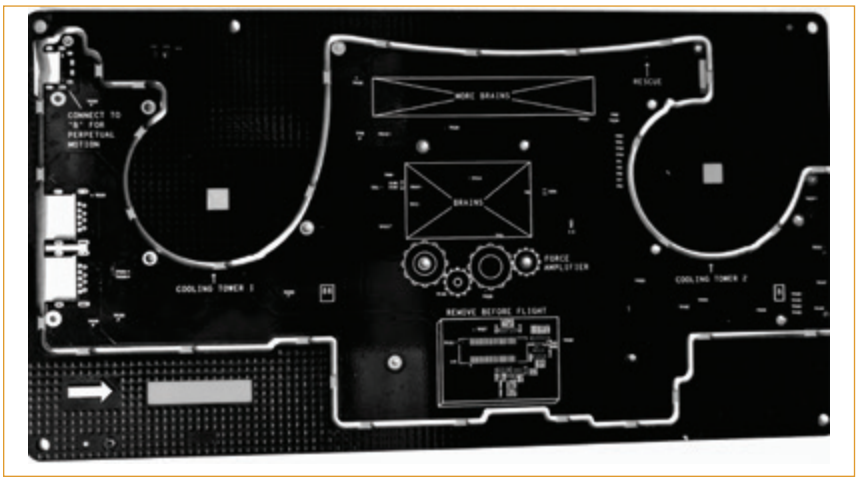

FIGURE 2. Even if the board is big enough to process alone, a pair of long, straight edges aren't always possible, so material must be added for a one-up panel. Note the break-off area is used to show the direction of travel on the conveyor belt.

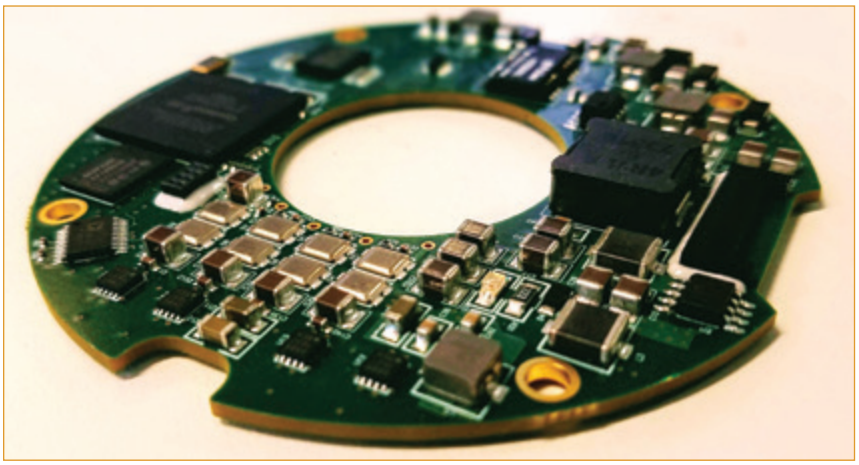

FIGURE 3. Populated and depanelized version of Figure 1. Note the connectors are secured with adhesive because of the expected environment.

in the reflow oven.

The key element to a reliable placement is the space between components. We want the shortest possible RF paths, so that is the first consideration. Wide busses also demand close proximity between drivers and receivers. Almost all decoupling caps will benefit from being near the associated power pin. Crystals should be kept on a short leash. It seems every little component would like a spot right next to the main chip.

Even so, the more breathing room a component has, the longer its expected time until degradation and failure. Close but not crowded? How about selectively separated as required for coexistence and thermal management. So many factors pull us in different directions. Smart placement makes all the participants equally nervous and none of them overly so.

Sharing your work along the way is more important than ever. Arriving at the end of the design cycle with a product that everyone can buy into is the main goal. The last thing we want is for the board design to become the giant ship that gets stuck in the canal. That's what it's like when various factions are still working out their differences.

Getting buy-in on placement is harder than getting it for the complete design. I usually submit the first placement with the receive and transmit chains hooked up. All the components are colorized by their schematic pages. The reference designators are neatened up, even though there will be some churn for sure. At least some of it survives until tape-out.

The more you can do to grease the skids for that day, the better. Successful designers juggle a lot of data to deliver something that goes through the assembly line with a minimum of manual operations. Understanding the end-use and how it all goes together helps us improve our products while staying in the sweet spot. ▫

PCB Engineering on the Move

Get your skills in order, as the industry is ramping once more.

IN THIS MONTH'S column, I examine the PCB engineering job outlook and evaluate the career moves we are making. Next, I switch over to PCEA Chairman Steph Chavez, who points out important attributes our personal development should include to keep our edges sharp. Again, I am happy to provide our readers with a growing list of events coming up in 2021.

PCEA Updates

The pandemic came upon us like a supersonic jet – unseen and unheard until it passed over. It compressed the atmosphere of our lives, our industry and our jobs. As it appears to be moving on with the help of remote working, masking, social distancing and vaccination, the industry is moving to positively decompress. NPI programs are now revving up once again and causing sonic shock waves of hiring activity and job movement. Were you furloughed, laid off or had your hours cut back due to the pandemic's effects? Boom! It's time to clap back!

Check out the PCB industry hiring pages. Here in the Pacific Northwest are pulses of hiring activity, and most likely in your area too. One PCB designer moved to a company which is staffing up for new projects, leaving a void at the previous company. I am happy to have recently been given the opportunity to fill the position. But my movement left a void in the company I left, which is now trying to recruit another designer to fill my place. Will they hire a designer who was previously laid off? Will another designer depart their job to fill it? Design resource movement. It will go on and on and hopefully that is a good thing if we all can learn from it. (Ed. note: Please be sure to fill out the annual PCD&F design engineer salary survey at https://www.surveymonkey.com/r/LHCJCZF. All individual data are kept confidential.)

2020, what did we learn? Regardless of the 5 W's – who, what, when, where and why – our present state-of-being is subject to unforeseen circumstances. We've seen that a supersonic economy can be put on hold by the smallest of organisms – a virus in this case – which caught us off guard. We've seen our strengths can become weaknesses if not paired with the diverse strengths of others. We've seen no one is an island. We're in it together. Hopefully, we've seen we need a healthy industry ecosystem full of workers, moving about, healthy in mind and spirit.

What must we do moving forward?

Germinate. Write down your ideas, visions and goals. These are seeds which, upon sprouting, will help reveal options to move positively within your organization. They can help you become a positive shockwave and foster movement within, or even outside the organization, if the culture or atmosphere becomes too compressed.

Feed. Find your strengths and feed them. Upon starting at my new company, I was delighted to receive a copy of Don Clifton's book, *Discover Your Cliftonstrengths*. This let me know the leadership of this engineering group is interested in helping me to understand my strengths and pairing those strengths with others to achieve synergy.

Grow. We grow by pushing away the compost of our surroundings. We must push toward the sky! As PCB engineering professionals, we must reach for technology and skillset nutrients, which are easily found within the pages of this publication and the upcoming events sponsored by the PCEA and many other electronics industry organizations.

Transplant. New to the PCB engineering industry? Maybe you consider yourself a seedling. You need to learn all you can in your present position and, eventually, in a new one, to avoid becoming rootbound. Again, this may happen inside or outside your company, but it must happen. Look to your organization's management as your gardener. For the organization to benefit, you must grow. Are you an old-timer in this industry? Your management should consider you a valuable, aged, majestic oak. Most likely you have been transplanted many times and are thriving because of it. You provide shade and seeds for future ideas to be planted anew. You make it easy for them to answer the most profound PCB engineering staffing question: "When is the best time to plant a tree?" Answer: "Thirty years ago."

Message from the Chairman

by Stephen Chavez, MIT, CID+

I'll keep this month's message short and simple. Printed circuit engineering is so much more than simply connecting dots. Knowing how to design a PCB correctly, having the ability to successfully collaborate with others, effectively communicating with internal team members and suppliers, and lastly, mastering the CAD system are all major attributes of most successful printed circuit engineers.

As companies and engineering teams push the

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envelope with their designs, the use of their CAD systems, and their capabilities in how effectively they work together to bring their respective products to market on schedule and under budget, many of us must constantly evolve and continue our professional development. It's extremely competitive out there! Even we industry veterans with decades of experience and education must constantly evolve and stay sharp so we don't get left behind and or become obsolete. That's why PCEA is a great industry association to get involved with.

Collaborate, educate and inspire are the core principles of PCEA. Sharing that latest industry information, technologies, educational content, and industry best practices are topics you'll find within PCEA. Building long-term relationships both professionally and personally as well as mentorships are also aspects one will find. A good example of these topics in motion was a recent Orange County, California, chapter meeting. Scott McCurdy and his leadership team held another successful chapter event with roughly 100 or so attendees. The topic was Designing for RF: Tips and Tricks from the PCB Pros, presented by EMA, one of our (PCEA) sponsors. It was another great event. I also want to thank EMA for bringing excellent industry content to the table. The collaboration between PCEA and EMA was another home run!

With so many industry webinars, Zoom, GoTo and MS Teams meetings, plus the flood of "free" online content, we've been getting bombarded with information for quite a while. It's hard to find the time to attend these industry events, to know which content is worth giving up an hour or more of time to sit through. Rest assured that if PCEA puts on an event or collaborates with another industry association, you can count on the best and most relevant industry content.

It's been over a year since we've been on lockdown, but we are slowing coming out of it. I cannot wait to get back to attending live in person industry conferences! I'm sure most readers feel the same. Like always, we adapt to the times and the evolution of the industry as this new way of collaborating through online meetings and the 24 hours online streaming content are here to stay. Of course, no experience is quite like a live industry conference! I can't wait to see you all in person at the next industry event!

Over these next few months, we will be rolling out lots more educational content as we continue to integrate and collaborate with our sponsors. Per our mission statement, partnering and collaborating with our sponsors allows us to bring outstanding industry educational content to everyone in the industry.

I continue to wish everyone and their families health and safety. Best of success to all as 2021 unfolds.

Warmest regards,

Steph

Next Month

Next month is hopeful and wide open for coverage of a potpourri of PCEA activities. Tune in to this column for the latest events ideas.

Upcoming Events

Below is our list of upcoming events. Hope to see you at any of these!

- **PCB West**
  Oct. 5-8, 2021
  Santa Clara Convention Center
  Santa Clara, CA
  www.pcbwest.com

- **SMTA International**
  Nov. 1-4, 2021
  Minneapolis, MN

- **PCB Carolina 2021**
  Nov. 10, 2021
  Raleigh, NC

- **Productronica**
  Nov. 16-19, 2021
  Munich, Germany

Spread the Word

If you have a significant electronics industry event to announce, send me the details at kelly.dack.pcea@gmail.com, and we will consider adding it to the list.

Refer to our column and the PCEA website to stay up to date with upcoming industry events. If you have not yet joined PCEA, visit our website: pce-a.org and find out how to become a member.

Conclusion

Sometimes it's just way too easy to describe our work in metaphor. This month we covered PCB engineering career movement, drawing parallels from the phenomena of sonic booms to to gardening 101. Whether we use metaphor or cold hard numbers and statistics, as our PCEA Chairman Steph Chavez mentions, the goal of the PCEA is to collaborate, educate and inspire. We want you to value yourself along with those you work with and work for. We hope we are reaching you.

See you next month or sooner! ▫

The Case of the Noisy PDN

Tips for reducing resonance and SSN.

FAST INTERFACES AND switching speeds are becoming commonplace, and with them comes increased noise, amplifying any problems within the power delivery network. Products today are the direct result of the fast signal capabilities in current technology, making it impossible to eliminate noise. This noise can be seen in the form of simultaneous switching noise, which resonates and can combine to destroy the voltage signal and collapse the signal eye. Therefore, the only viable option is to mitigate the noise via containment.

Ground is the point from which every measurement is evaluated. Therefore, any variation will affect timing and voltage. Every signal switching on the board, whether slow or fast, contributes to noise on the power and ground planes. This "ground bounce" is commonly referred to as simultaneous switching noise (SSN) and is essentially crosstalk on the ground **(FIGURE 1)**.

Since all digital signals share a reference point (in this case ground), too much noise on one section of the board can have disastrous effects on unrelated sections of the board. With more ground planes and copper, the effects of SSN tend to be more of a local problem – such as near a chip with poor decoupling capacitors – rather than over the entire plane.

The accumulation of SSN is not easy to visualize in the time domain; multiple signals are turning on and off at certain times, and the noise generated from these actions adds up. All the signals on the board are returning through the ground, bouncing their respective voltages. Signals with higher voltage swing can be particularly damaging to faster signals, which have reduced margins. These already vulnerable signals, such as timing, memory or sensors, are the most susceptible to uncontrolled variation on the ground plane: for example, if just one incorrect bit of a data bus can have detrimental effects to the functionality of the design.

Exploring resonance. Not as intuitive, but equally if not more important, is analysis in the frequency domain. Utilizing conversion through Fourier transform, we transition from the time domain to the frequency domain **(FIGURE 2)**. It boils down to basic math; we factor individual complex signals down to the frequency components made from sine waves. Signals are then dismantled and factored down into individual waves that can be more easily controlled. Therefore, even though the board may not be operating at a specific frequency, it may still be an area of concern, as signals are composed of smaller individual frequencies. When peaks align, as we would see with signals of the same frequency, they can add up to sweeping voltage spikes across the board, known as resonance.

Resonance is the accumulation of repetitive small waves that, when combined, form a big wave. Think of it as a crowd effect: frequencies with a common denominator and multiples of each other that accumulate. For example, if you're in a theater and one person stands up and starts screaming, it's easy to suppress the noise they're emitting. However, five or more people screaming in that same theater create noise that's harder to control.

Keep in mind certain regions of the board will echo frequencies better than others. This is related directly to the shape of the copper pour, as it can affect resonance by creating a sort of echo chamber on the power plane. In our theater example, the size and shape of the theater itself will affect how noise is handled. Will it be suppressed or amplified?

We can't approach this as a typical signal integrity problem because all frequencies happen at once; they're all on the board, at the same time, on the same

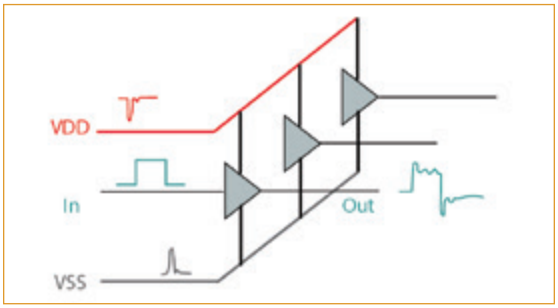

FIGURE 1. Simultaneous switching noise.

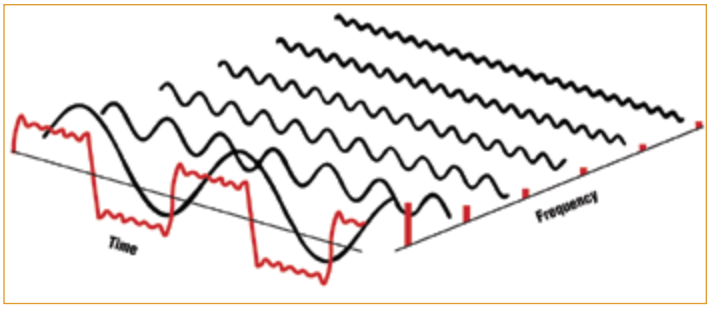

FIGURE 2. Time domain to frequency domain.

TERRY JERNBERG is an applications engineer with EMA Design Automation (ema-eda.com), with a focus on PCB design and simulation. He spent his early career on signal integrity simulation for the defense industry and was fundamental in the adoption of these tools at EMC and Bose. A vocal advocate for simulation, his enthusiasm for physical modeling has expanded to include power and thermal capabilities.

piece of copper. It's not an individual effect like reflection or impedance mismatch. We're dealing with the culmination of multiple signals and frequencies happening at the same time. By dismantling signals into numerous sine waves, we can easily switch focus and control noise by muting the sine waves with targeted capacitors.

Containment is key. Luckily, designers have control. Resonance and SSN can be reduced by altering shapes of the power planes or by adding external capacitors. Managing resonance is about balancing the frequencies we inherit due to the nature of the design with what we have control over. If we know signals are made of sine waves in a specific frequency range, then no matter the amount of current, we can control the voltage proportionally by reducing the impedance. The goal is to have a low impedance over a wide frequency range. To reach this goal, keep in mind three items: copper shapes, the value of any capacitor added, and the way capacitors are attached.

Altering copper shapes can suppress resonance and change the path for the current to flow. Through elongation and notches we can introduce interference, interrupting the echo chamber and steering the signal to where it needs to go. It's important to steer current away from items such as clocks and oscillators because the noise they create can affect the entire board. This can be accomplished through guard traces, which act as a moat preventing the signals from reaching these critical components.

Modifications on the plane affect impedance. Therefore, it's imperative to analyze how these changes affect our initial low impedance plan and adjust to meet original goals. Instead of a smooth area for current to flow, copper is broken up with notches, traces and vias. This increases impedance in certain areas of the design. Placing a capacitor to seal the opening at the required frequency can suppress areas of high impedance.

Resonance can be addressed in a similar way. Placing a capacitor for every frequency on the board is not feasible; however, capacitors targeting certain frequency ranges can combine and reduce the overall impedance. Instead of managing each individual signal, we can eliminate the noise from multiple signals operating in the same frequency range. If we create a smooth enough path by way of low impedance with the capacitors, that current cannot generate enough voltage to be problematic.

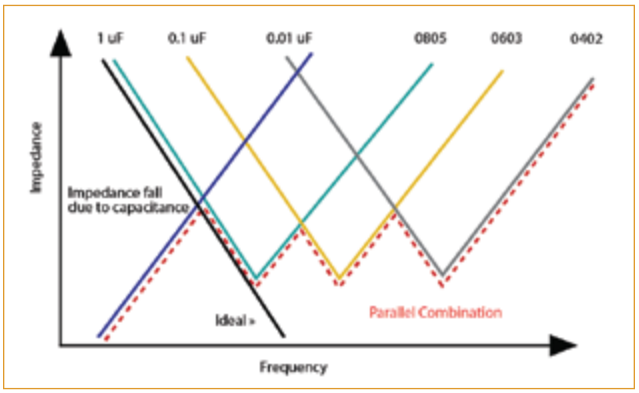

FIGURE 3. Matching resonant frequency.

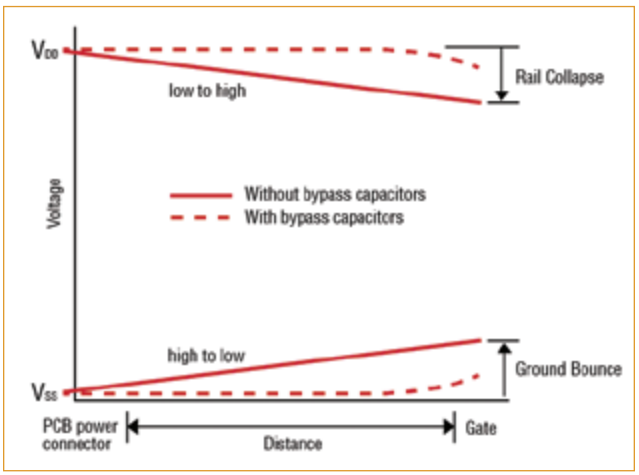

FIGURE 4. Signal eye collapse.

Cap selection and placement matter. The value of the capacitor and how it is attached have a direct correlation on the effectiveness. To suppress current over a specific frequency range, you must identify the ideal capacitor value based on the resonant frequency. This is accomplished by referencing the component datasheet for the optimal performance frequency of the capacitor and matching this with the frequency we are trying to control on the board **(FIGURE 3)**.

Once selecting a capacitor to suppress resonance or impedance, we must also control the mounting impedance so the capacitor can be effective. The mounting impedance is made up of the capacitor size, type, placement, routing, vias and the device packaged itself. While this can be done manually, software and tools can aid in identifying the ideal capacitor value, size and placement to reduce impedance. Through the process of designing the board, the ideal current flow can be compromised; however, through some simple steps we can contain it.

Power first. If we choose not to address power at the beginning of the design process, we increase the likelihood of discovering catastrophic mistakes later. The later in the design cycle these defects are found, the more limited our options to resolve them.

For example, with ground bounce increasing the base of your measurements and resonance decreasing the top margin, it is likely the signal eye will collapse **(FIGURE 4)**. If this is caught at the end of the design process, no workaround will correct this. The only option is to change the signal, and that is not guaranteed to work. A "power first" mentality addresses power issues and influences decisions throughout the design process to prevent this from happening.

Power should not only be addressed first; it should be incorporated throughout the analysis process as well. Power and signal integrity are intertwined, as issues within the power delivery network can have a direct effect on signal quality. Looking at the design as a whole and incorporating signal and power integrity in tandem is the next step. This is where co-simulation comes into play. □

The Phenomenal OCR

At least five operation areas can benefit from switching from manual data entry.

"Innovation is the ability to see change as an opportunity, not a threat." – Steve Jobs

SEVERAL YEARS AGO, I embarked on an advanced engineering initiative, seeking unknown, innovative ways of processing PCB design packages for manufacturing external to the status quo, with a primary objective to drive efficiency and productivity, eliminating redundant data entry and reducing human interactions with their associated software applications. I had thrown in the towel relying on our software vendors to provide real and robust solutions. In my opinion, it was not in their interest. As their focus was selling more licenses to increase revenue, developing and marketing advanced automated solutions did not support this cause. My mantra was to take internal ownership and venture into unfamiliar territories. This path led me to OCR (optical character recognition) and, although skeptical at first, the results of our analysis were phenomenal.

Product design specifications and requirements are provided in formats such as PDF, Word, Excel, HPGL, or even as handwritten notes on scrap paper. A close associate of mine calls it "e-paper." The variety of methodologies used to convey the same information across the PCB industry that is often ambiguous is staggering, to say the least. We print, read, interpret (hopefully correctly) and manually enter these data into our respective software application, often multiple times by multiple organizations.

OCR is not science fiction. It is real and used by some of the largest companies in the world, processing millions of documents each day. The speed, efficiency and labor savings alone are in the hundreds of millions of dollars. Since it works for invoices, purchase orders, legal and banking documents, I thought, "Why not with fabrication specifications for PCB manufacturing?" The results of our findings were staggering.

A fabrication drawing outlines all pertinent information relative to the product in question. These attributes include part number and revision, surface finish, materials or stack-up, impedance requirements, drills and tolerances, dimensions, solder mask and nomenclature type and color, IPC specification classifications, and many others organizations manually enter into quoting or engineering applications.

Using an advanced OCR application such as ABBYY Flexicapture (abbyy.com/flexicapture), you simply import the fabrication drawing, and all the relevant product specification attributes are extracted into an XML file that, in turn, imports directly into the master database, quote or engineering applications, all in just a few minutes. While I certainly recommend an engineer read and review the fabrication specification, we have eliminated the time-consuming manual administrative task and error-prone entries, and replaced them with validation only.

"AN **ADVANCED OCR APPLICATION** CAN EXTRACT **ALL RELEVANT** PRODUCT **SPECIFICATION ATTRIBUTES** INTO XML FOR IMPORT INTO THE **MASTER DATABASE,** IN MINUTES."

The reality is most of the notes on a fabrication specification drawing are in excess of 20 words, and we need only specific information to complete our task. In essence, the OCR application can be taught to identify these keywords, and, in turn, that is what is extracted. Drill tables, with up to 20 or more drill callouts with tolerances, plated or non-plated, microvia or back drills, are in turn extracted. I could go on, but the fact is anything you read on the fabrication specification can be extracted into an intelligent XML file, and from there the opportunities abound with what you do with it. Operational areas that would benefit are:

- Quote generation
- Pre-production planning – travelers
- Document control – AS9102 reports
- Quality – inspection criteria or spec review
- Finance and accounting.

Using an advanced OCR engine with an embedded native language processor (NLP) provides the foundation to achieve speed, accuracy and a cost-efficient operation, all of which should be a major focus for any company leader in the competitive landscape of PCB

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FIGURE 1. Commercially available tools automatically extract the key information from fab drawings, eliminating manual entry.

manufacturing. Providing solutions to engineering personnel that take them away from menial tasks and effecting an environment for them to innovate will only enhance the operation. I looked beyond the industry standards and was pleasantly surprised what OCR technology is capable of, and the multiple benefits it could bring to our daily operations.

If you would like more information or discussions on what this can do for your company, please feel free to contact me directly. In my next column I will elaborate on how to drive more autonomous processing of the design data packages in an environment of smart engineering. □

The IoT is Fantastic but Flawed. We Need to Fix the Vulnerabilities – and Fast

Plus, how AI can help deal with the threats.

FORGET ENTERPRISE DIGITAL transformation. For better or worse, we are digitizing the world, and it's changing everything. The opportunities to make things better are tremendous; we can save wasted energy and natural resources, democratize access to all kinds of services, improve standards of healthcare, prevent avoidable accidents, and accelerate our transition to renewable energy. By connecting everything, and introducing AI into the mix, we can gain insights we would otherwise never detect. Moreover, we can see the effects of our own behavior and use the analysis to identify ways to improve. Earlier technologies could never have done all this for us.

But there is always an "on the other hand," and in this case the issues relate mostly to privacy and cybersecurity. We are putting more information about ourselves than ever before into the hands of data scientists. While we can expect better shopping experiences, we are at the same time disclosing insights into ourselves, our activities, and our preferences as individuals. And if we are not giving away information directly, everything we do online (and we are almost permanently online) reinforces the accuracy of any and every inference made by the AIs that constantly watch from the cloud.

We may not be too bothered about giving organizations information to help them offer us more of the things we like, but manipulation can take many forms, and power in the hands of rogue agents can enable abuse on any level – from rogue blackmailers threatening to expose details of our personal lives, to organized groups seeking to gain control of essential infrastructures, damage our economies, even destroy our democracies. The potential for damage through hacking IoT assets is limitless, both in scope and extent. Yet the technical standards surrounding IoT cybersecurity are underdeveloped, and legislation is inconsistent and fragmented. There are signs the situation will improve. The US IoT Cybersecurity Improvement Act, signed into law in December 2020, places obligations on bodies such as the National Institute of Standards and Technology (NIST) specifically related to securing IoT devices. In Europe, the European Telecom Standards Institute (ETSI) Technical Committee on Cybersecurity has published a standard, ETSI EN 303 645, for consumer IoT devices that could aid the development of future IoT certification schemes. Neither of these can yet be considered a global standard.

As a result, today's IoT and IIoT practitioners have only limited tools at their disposal to make "things" secure. Even so, given the scale of the risks, it's surprising many projects still fail to implement even the most basic security measures, such as changing the factory-set default password when installing a new IoT device. There is an urgent education challenge here, and there can only be more to learn as the future unfolds, so organizations that are installing and managing IoT applications must keep pace with developments. This is a battle of arms versus armor that will become increasingly complicated.

AI's ability to identify patterns, both normal and anomalous, buried within vast quantities of data, can help deal with these threats. Although AI can be a bit scary – it can get to know us better than we know ourselves and risk exposing the insights to others who have no business knowing them – it could become the most powerful tool we have to protect our safety and privacy against the most serious cyber evils. AI-based threat detection can work by spotting known patterns associated with attacks that have happened in the past. AI can spot previously unseen attacks, too, by looking for unusual patterns in otherwise normal data flows. We may draw some comfort from this: It means getting any kind of trick past an AI, whether recognized or unrecognized, is extremely difficult.

The development of laws for prosecuting hackers is, arguably, more seriously lacking than the technical standards situation. Existing laws on computer misuse are way behind the pervasively connected world of today. There has been no justice for the Stuxnet gang, or those responsible for Mirai or BlackEnergy. In any case, there is much speculation they may be backed by various state security services, so prosecution would be difficult or impossible, even if they are positively identified.

We know IoT devices are vulnerable, and it's partly due to the tight constraints usually imposed on factors like power consumption, computing performance, and cost. They simply cannot execute heavy security protocols. Security for edge devices needs to be strong yet lightweight and unobstructive for legitimate users.

With the continued expansion of the IoT, we are seeing a growing diversity of connected devices in use, spanning a widening performance spectrum. We can get more and more computing done for each dollar spent on the silicon and for each watt dissipated. Tougher security standards, as they evolve, should consume some of this extra capability. On the other

continued on pg. 29

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Demystifying POWER INTEGRITY

How to easily check current limits between a DC-DC converter and an FPGA.

by RALF BRÜNING and MARCUS BUECKER

The design of power-supply structures on PCBs is not trivial. It requires careful consideration and techniques to achieve the best performance. Today's high-pin-count devices need efficient power distribution systems permitting high-speed/high-frequency switching. The space available on PCBs is increasingly scarce. Thus, engineers fight for every square millimeter, using multiple layers for the layout of signal nets and power areas, parts of the power distribution which are then connected using dedicated power distribution network (PDN) via structures.

The narrowing of various supply voltages, coupled with increasing IC complexity and the number of voltage rails required, makes power integrity analysis inevitable for high-speed designs. This applies to AC as well as DC effects. The most compelling evidence is that modern circuits like (LP-)DDR memories operate at very low voltages (LP-DDR4 at 1.1V, for example).

Hence, typical power distribution systems today contain large numbers of vias connecting the different parts of the PDN across board layers. Often, large currents travel within these PDNs. Currents can reach dozens of amps when multiple FPGA signals are switching in parallel, while parasitic switching currents can reach even higher numbers for a very short period of time. Automatic via reinforcement functionalities within the PCB design environment often add fuel to the fire. This means automatically generated via structures may not be optimally designed against the required electrical power conditions imposed by increasing currents.

Temperature constrains current. The laws of physics dictate PCB traces and vias have a maximum current carrying capacity. A direct relationship exists between trace width/via dimensions and their current-carrying capacity. Specifically, any cross-sectional area of copper (trace width/thickness or via dimension) is a victim of temperature rise as a function of the current flow. This maximum allowed temperature typically constrains the maximum allowed current. PCB layout engineers often find this in the various IPC formulas dealing with PCB trace currents.[1,2] Proper sizing and number of PDN vias for low resistance and long-term reliability are essential for successful PCB design.

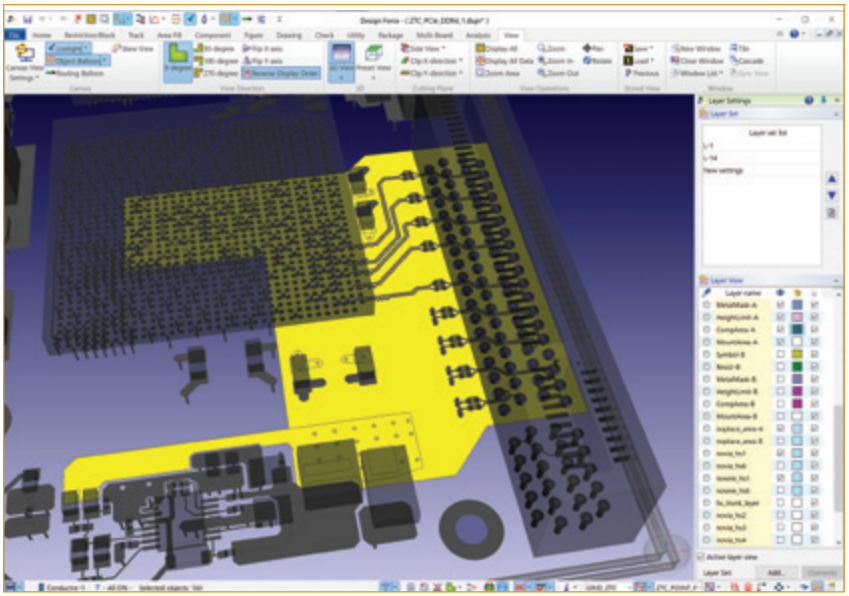

FIGURE 1. Investigated structure: the main power supply of an Intel Arria FPGA.

This article describes how to easily check the current limit between a DC-DC converter and an FPGA, using the Zuken PI/EMI tool in a real-life example.

Simulation scenario. The supply system in our example is routed on two layers, connected by 68 power vias in total **(FIGURE 1)**. The current limits can be checked directly using the DC analysis features of the analysis tool. An embedded DC solver is used to perform IR-drop analysis and quantify current distribution across the

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surface of the investigated power distribution system (FIGURE 3). The investigated case was simulated in less than 30 sec. (25µm discretization).

Such a fast simulation approach enables the execution of various parametric studies. These could be changing the PDN routing patterns or connection strategies or adding and deleting vias. Re-simulation cycles help elaborate the impact of such measures. Within the tool, users can manually create virtual via types to explore the solution space with respect to power flow and IR-drop.

In our example, closer studies reveal currents are not distributed equally between all vias of the power via array. For instance, a few vias carry the majority of the current, while most others show only smaller current values. We investigate this using the tabular view showing all via currents of the VCC system in the PI tool (FIGURE 4).

The via structures under investigation are identified by cross-probing between the PI/EMI analysis tool and the main PCB canvas in 2-D or 3-D. In this example, several of the vias carry only a minimal portion of the overall current, while others are overloaded. This situation may lead to wasted board space (unnecessary vias), while also running the risk of other vias overheating. Worst case: Vias could melt away over time during system operation.

Next, we use the integrated PI/EMI tool for analysis on potential design issues, such as the impact of adding or removing power vias. The maximum allowed current can be specified on a per-via basis to check for current-carrying violations.

Based on the initial results, various parametric studies have been performed in this case. In one instance, an additional PDN-via has been added and varied in its position in relation to coil L101. Furthermore, some of the vias considered unnecessary have been removed. The results of multiple DC simulation cycles have investigated the implications.

FIGURES 5 and 6 show the current distribution of the original structure compared to a via-array featuring that one additional via. Note the newly added via will now take most of the current (428mA).

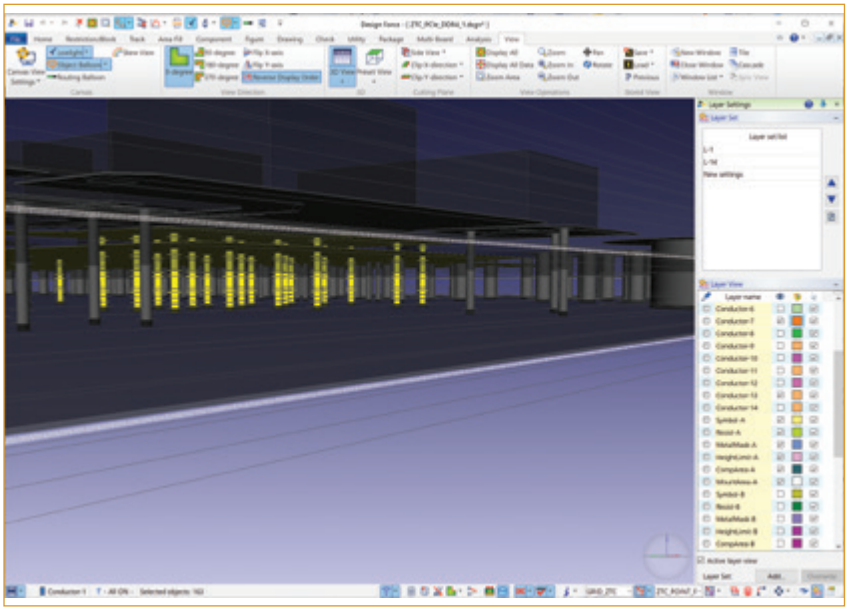

FIGURE 2. PDN vias between Layer-1 and Layer-4.

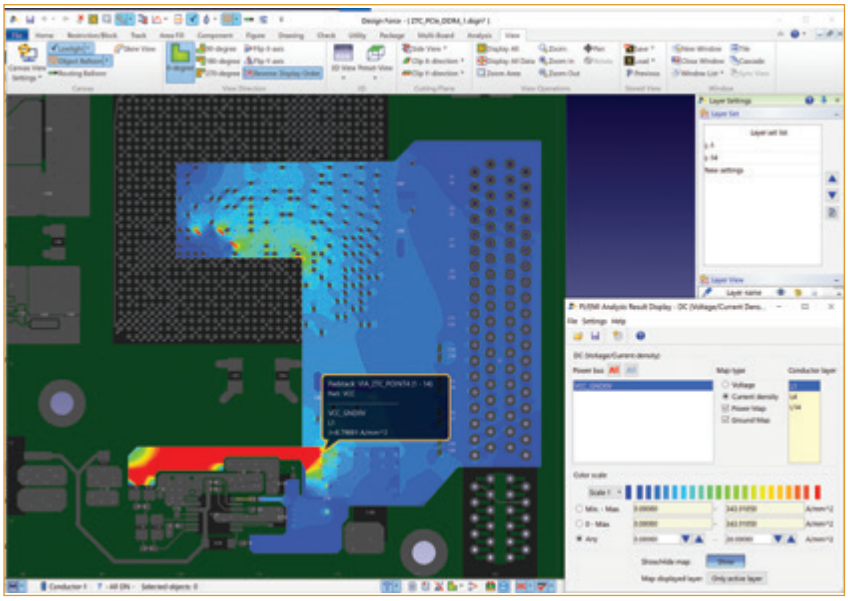

FIGURE 3. DC analysis result (current distribution).

FIGURE 4. Virtual PCN via with less DC resistance for what-if studies.

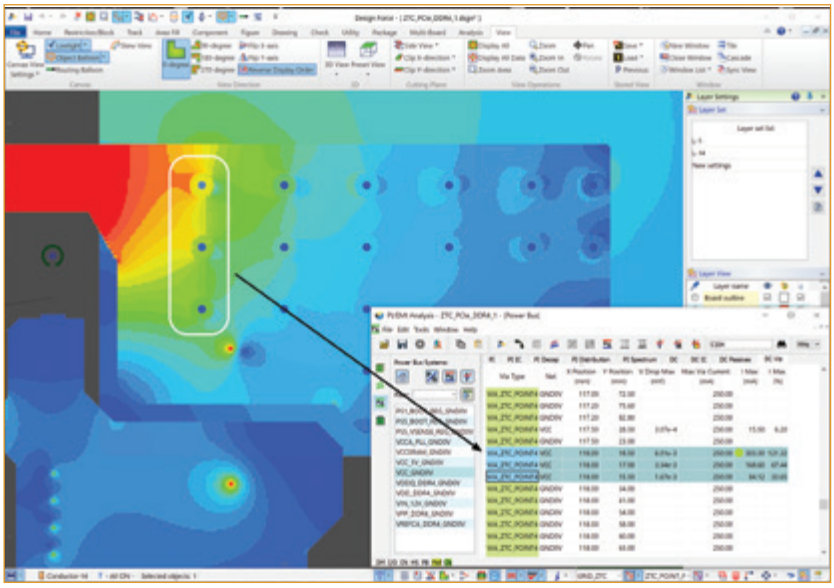

FIGURE 5. PDN via current results, original structure.

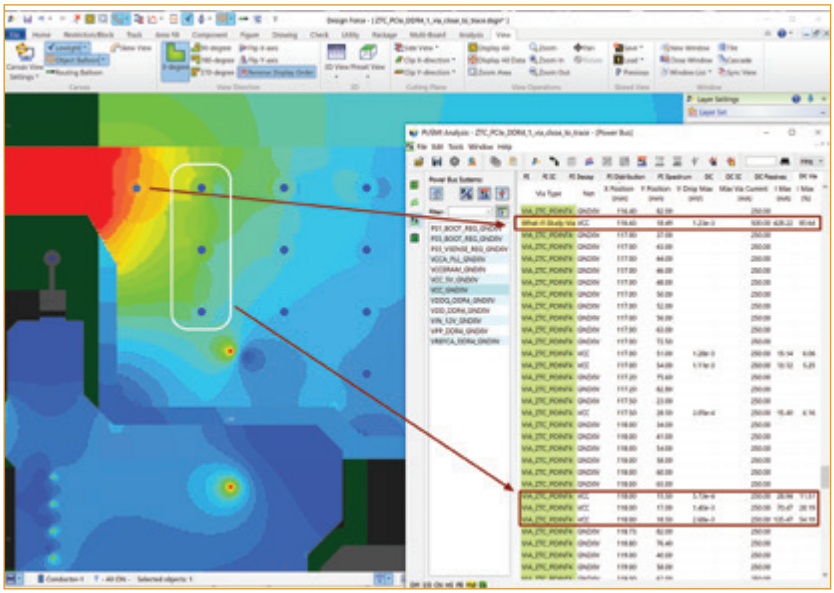

FIGURE 6. PDN via current results, modified structure.

Conclusion

PCB designers often struggle to find the optimal power/current carrying capability with a minimal number of vias, perhaps smaller vias. This is particularly true for small form-factors (e.g., IoT or medical applications) or complex high-speed designs. These can range from data center servers to industry automation or automotive ECUs and especially EV electronics. All these applications support various levels of high-current loads from the increasingly power-hungry MPUs, DSPs, FPGAs, or ASICs.

Designing power modules using modern DC/DC converters (and PMICs) requires advanced information on parasitic behavior of the copper spread over the board as part of the PDN. Easy-to-use and easy-to-access PI simulation techniques can be vital to enable proper PCB operation under such conditions. □

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Material Gains, continued from pg. 26

hand, device makers will inevitably face pressure to increase features and performance. We can expect future generations of edge devices to become more capable, bigger, more power-hungry, with performance-oriented design evident at every level from the application software to low-loss and thermally enhanced substrates. Expect more focus on highly optimized board designs, even for relatively simple devices.

Leveraging AI in the cloud, as well as embedded in edge devices, the IoT – for all its vulnerabilities – is the most pervasive and empowering influence in the modern world, a critical enabler for handling challenges like the climate crisis and complex of cross-border trading arrangements like that between the UK and EU. The benefits are too good to ignore, despite the obvious security dangers. □

How are Electronics Manufacturers Using BLOCKCHAIN TECHNOLOGY?

Three options for leveraging the secure digital ledger.

by QUENTIN B. SAMELSON

In last month's introduction to blockchain technology,[1] we noted how the technology offers a way to automate and simplify multiparty processes that are time-consuming, resource-intense, and therefore costly. We often summarize this sort of process as "high-friction." But pioneers in applying blockchain to improve multiparty processes learned early that it wasn't enough to find a process that was slow or frustrating. There needed to be a quantifiable performance (often financial) benefit as well. This wasn't always easy to establish. Unlike applying automation to improve internal processes, the "friction" in multiparty processes occurs outside an organization. As a result, the costs and performance issues caused by that friction may not be captured well enough inside the organization to understand its true impact.

Perhaps it's understandable, then, that the most successful early blockchain applications were often driven by companies large and sophisticated enough to not only recognize, but quantify, the opportunities and to have enough influence with their partner companies that those partners were willing to collaborate on a solution. Indeed, a recent article in *MIT Sloan Management Review*[2] states, "The biggest challenge to companies creating blockchain apps isn't the technology – it's successfully collaborating with ecosystem partners."

Early Use Cases

In the electronics industry, the earliest proof-of-concept blockchain applications generally revolve around processes between an initiating (usually large) company and its partners. The initial company generally sponsored the development of the application, and its partners were generally willing to participate in the improved process. For example:

1. A major computer OEM leveraged blockchain technology to enable a "buy/sell" process among its component suppliers, third-party manufacturers (EMS providers), and itself. This sort of buy/sell process has been automated before with more conventional technology,[3] but blockchain was clearly superior due to its ability to let multiple parties view the same transaction but keep some data (like pricing) private between authorized parties **(FIGURE 1)**. The older, conventional technology had to model the process as a series of separate two-way transactions; blockchain permitted a much more efficient, single-transaction approach.
2. Another large electronics company noticed both its accounts receivable and accounts payable processes were often blocked by simple discrepancies between invoices and purchase orders or contracts. Using blockchain to ensure there was only one shared record removed the majority of discrepancies. (The payoff in addressing these processes is different: Removing impediments in accounts receivable helps a company get paid faster; eliminating disconnects in accounts payable reduces overhead.)

Adapting Use Cases from Other Industries

Additionally, electronics companies began to hear about applications originally developed for other industries, especially ones dealing with tracking shipments and understanding the

FIGURE 1. Use a blockchain-shared ledger to manage a separate financial flow (supplier to OEM to EMS) and physical flow (supplier to 3PL hub to EMS) with a smart contract that automatically executes the financial transactions when physical actions have occurred. Use a blockchain-shared ledger to manage a separate financial flow (supplier to OEM to EMS) and physical flow (supplier to 3PL hub to EMS) with a smart contract that automatically executes the financial transactions when physical actions have occurred.

FIGURE 2. The Responsible Sourcing Blockchain Network was set up to improve the knowledge of how critical materials like cobalt were sourced, and to provide tracing of goods made with those materials.

origin, or "provenance," of purchased items. The first prominent shipment-tracking application was developed by IBM for Maersk, and a food-provenance project for Walmart grew into the IBM Food Trust application. These prompted extensions in two very different directions:

A. To improve the responsible sourcing of raw materials, a group of electronics and automotive companies formed the Responsible Sourcing Blockchain Network[4] to promote the use of blockchain to trace raw materials all the way back to the source **(FIGURE 2)**.

A. Once the Food Trust platform was established, other companies recognized electronic "trackers," which physically accompany a shipment, add a new level of useful data to the existing track-and-trace capability, providing detailed information on the quality of the produce shipped and linking the quality data captured during shipment to the transactional data captured as the shipment passed from source to destination. Thus, blockchain platforms offer new markets for electronics devices that support data collection.

On the other side of the electronics industry, companies that market big, rack-mounted equipment for data centers and telecommunications often struggle with the process of onboarding local contractors to assist with installation. To make matters worse, the new "vendor" qualification process often subjects those contractors to high costs and delays. The ability of blockchain to permit secure sharing of pre-validated data spawned an application called "Trust Your Supplier." Companies that rely on local contracting firms recognized much of their qualification process was common and – once validated – could be reused. Blockchain provides the ability to reuse that pre-validated qualification data without revealing the identity of the previous customer(s) of the contracting firm, and only after the contractor has given its approval.[5]

Electronics companies now have three basic options to leverage blockchain technology:

- They can be the "founder" of a new, unique capability to be employed with their own network of trading partners. If the idea has broad applicability, this could grow into a new platform like the ones mentioned above.
- They can join an existing network to solve an industrywide problem that they are also experiencing. As mentioned, networks already exist to assist with logistics, responsible sourcing, local contractor qualification, and other industry issues.
- They can leverage existing blockchain applications to "convene" their own network.

Convening a network of your own comes with a unique set of opportunities and challenges. More on that last idea in next month's article. ▫

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FAILURE ANALYSIS of Burned Printed Circuit Board Assemblies

When it comes to contamination analysis, things are not always as they appear. **by CLAIRE BRENNAN, PH.D.**

In the failure analysis of electronics assemblies, we are often asked to perform a failure analysis on hardware that has undergone a significant thermal event. Hardware might be burned, melted or covered in debris. Determining a root cause for failure can be extremely difficult when the hardware itself is so damaged that much of the evidence has been destroyed. So, what can you do? Like many things, it depends. The success of the failure analysis depends on the overall degree of damage, the amount and type of secondary damage, and the history of the part. Over the years, we have developed some tools and techniques to get the most out of these challenging failure analysis requests.

The first step in these types of investigations is to manage expectations. Most customers will understand that much of the evidence was destroyed during the thermal event failure and that root cause analysis will be very difficult. It is important to discuss what types of information can be gained, however, and what may not be possible. It is also critical to get as much information as possible about the history of the part and any details about the failure itself. This proactive discussion will help lead the investigation in the "right" direction and avoid going down a path that will not yield useful information. For example, if some of the metallic hardware is corroded, it is important to know the storage environment of the unit, not just temperature and humidity, but also the amount of time the unit was stored and its relative orientation. The product history information is useful to separate damage caused by the failure versus damage that occurred before or after the failure.

As with all types of failure analysis, it is critical to document everything with high-resolution photos and/or optical microscopy at every stage of the investigation. If disassembly needs to be done, it is critical photos are taken before and after the disassembly. In some cases, it can be helpful to take a video of specific disassembly steps. This will help capture "intangible" information such as if the part made a certain noise, or if certain parts were easy or difficult to move. Ensure photos are taken before the part is moved, since heavily damaged hardware can cause pieces to become loose, shift, or fall out during movement. When opening compartments, such as a chassis, make sure to place a plastic bag underneath the part to catch any debris and/or loose parts.

The initial photo-taking stage is usually the best time to gather material samples for analysis. This analysis can confirm the presence of certain materials in the construction (for example, was the correct adhesive used on a particular component?) or to identify possible contaminants that may have contributed to the failure. It is good practice to label each sample with the location where it was taken, often including a corresponding photo. Even if some of the debris appears to have an obvious origin (e.g., copper from the internal layers of the PCB or solder ball from a component's solder joint), it is good to confirm these assumptions. When it comes to contamination analysis, things are not always as they appear. This debris analysis can also give clues about the temperatures reached during the failure based on the softening point and melting points of various compounds and alloys.

Depending on the type of debris, analysis can be carried out through x-ray fluorescence (XRF), scanning electron microscopy with energy dispersive x-ray spectroscopy (SEM/EDS), Fourier transform infrared spectroscopy (FTIR), or x-ray diffraction (XRD). Each of these analytical techniques is suited for a specific type of sample and will provide different information. **TABLE 1** is a short summary of the more common techniques for contamination analysis of solid materials, including the capabilities and limitations of each technique. With heavily thermally damaged electronics hardware, the contamination analysis process will likely be complicated by the large amount of carbon-based debris. Since the high heat of the failure can alter some materials, complementary techniques might be needed, such as SEM/EDS and FTIR, to determine the different materials. For example, if a dark-colored, metallic-looking material is collected on the failed hardware, it can first be analyzed with the SEM/EDS. SEM may show the material charges when exposed to the electron beam, indicating it is not purely metallic, and EDS analysis may show significant carbon and oxygen. If the material is then analyzed using FTIR, it

TABLE 1. Summary of Analytical Tools Used in Contamination Analysis

Technique	Type of Materials	Capabilities	Limitations	Other Considerations
XRF	Organics, Non-organics	Elemental Identification	Can't quantify some low atomic number materials	May be limited by sample size/geometry
SEM/EDS	Organics, Non-organics	Elemental Identification	Can't quantify some low atomic number materials	Best for conductive samples
FTIR	Organics	Compound Identification	Sample must be IR responsive (nonmetallic)	Standards or comparative materials may be needed
XRD	Crystalline materials	Crystal structure determination	Sample must be crystalline or semi-crystalline	Best for powders or flat samples

could be found to resemble the FTIR spectrum for an adhesive material used on the assembly. By running a "new" sample of the adhesive against the unknown material from the failed hardware, it could be determined the temperature during the failure was hot enough to degrade the adhesive material, or perhaps an incorrect adhesive was used. The wide variety of materials used in the PCBA necessitates multiple analytical tools for identifying different types of debris.

After the initial documentation of the as-received hardware and collection of samples, the team should have a short meeting to reevaluate expectations and develop an analysis plan. Typically, the next analysis step will be some sort of nondestructive testing or nondestructive examination (NDT/NDE). This could include 2-D x-ray, 3-D computed tomography (CT), acoustic microscopy, thermal imaging, various types of electrical testing, and optical microscopy (bright field, dark field, polarized light microscopy, etc.) **(FIGURE 1)**. X-ray radiography (both 2-D and 3-D CT scanning) is a powerful tool for examining the internals of failed electronic components, as well as pinpointing and quantifying the amount of damage in a printed circuit board assembly. For example, for heavily damaged PCBs, documenting how many layers are damaged and which layers have the most severe damage provides useful information, since this can help pinpoint where the failure started **(FIGURE 2)**. Identifying internal damage to individual electronic components, such as surface mount components, can be difficult since some of this damage might be secondary to the failure. It is important not to focus too much on damage, which is secondary to the primary failure, but documentation of this type of damage is still necessary to get a complete picture of the failure.

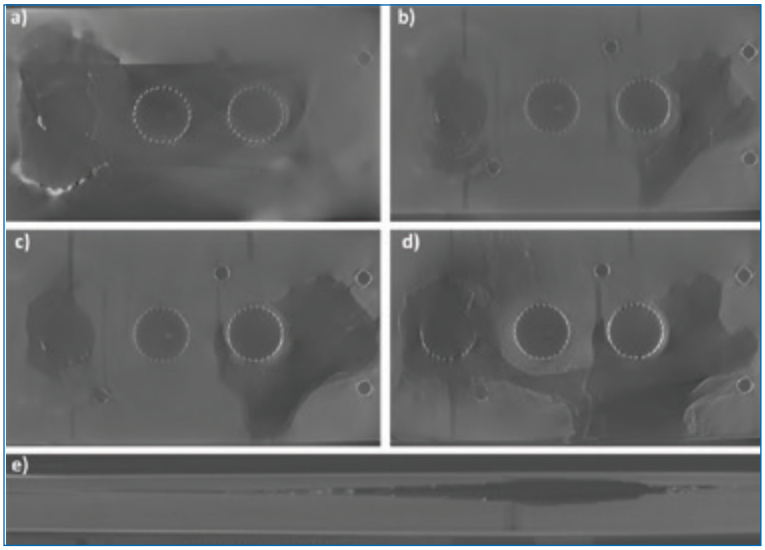

FIGURE 1. 3-D CT scan images of several layers of a PCBA from the top-down are shown in a) - d). 3-D CT scan image in e) shows a sideview of the PCBA, where damage and delamination can be seen in several layers. Dark contrast in the images indicates lower x-ray density material, and the dark regions within the PCBA above show excessive heat damage to the PCB.

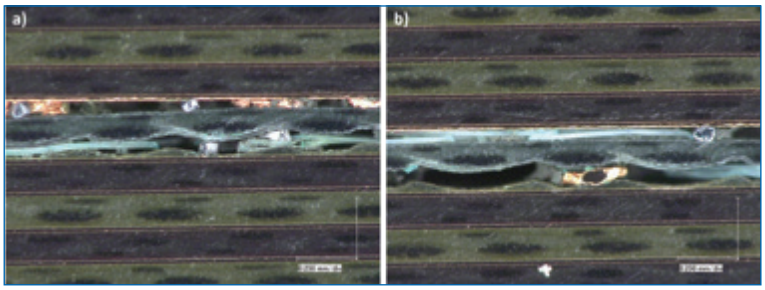

FIGURE 2. Metallograph cross-sectional images of a failed PCBA in a) and b), showing internal damage to the layers of the board. This technique permits visualization and characterization of the damage to the board, including damage to the glass fibers and copper layers as shown here.

Acoustic microscopy and thermal imaging are other tools used to image and document internal and external damage. Acoustic microscopy has the added advantage that it can pinpoint where the damage is located in a specific device. Depending on the extent of the damage, electrical testing may not be needed. However, for multiple damaged components on a failed printed circuit board, electrical testing can be used to map the extent of damage on the board, as well as diagnose the type of electrical damage that occurred (overstress, overcurrent, short, open, etc.). It is important to discuss any findings from nondestructive testing before moving on to any destructive analysis.

Destructive analysis can encompass a variety of activities, including physical decapsulation of components, cutting/sectioning in regions of interest, cross-sectioning printed circuit boards, and other techniques. Decapsulation and cross-sectioning may be used to verify the components or PCBs were made according to the applicable specification or drawing. For example, cross-sectioning can verify PCB layer thicknesses, as well as other features such as layer finishes and plating. Care should be exercised during this phase of the investigation, taking the necessary precautions to not introduce any artifacts that would confound or confuse the destructive analysis results.

Decapsulation of specific components is often a slow and tedious process, depending on the encapsulation/potting materials used and the chemicals used to remove them. Often, commercially available decapsulation chemicals can be used at room or elevated temperature. Alternatively, acids (such as sulfuric, nitric, etc.) can be used alone or mixed at elevated temperature to remove the encapsulation materials. Another tool that might be used in conjunction with chemical techniques is plasma etching or ion milling. Depending on the equipment used, these techniques can be focused or broad in nature, but are typically very slow. A summary of the techniques/tools used in decapsulation of electronic components is listed in **TABLE 2**. Each technique has its advantages and drawbacks, but one of the most important considerations is always how the decapsulation process alters the internals of the component. For example, some solder alloys are subject to chemical attack from sulfuric acid, so it is important to keep that in mind when analyzing the internals of the part.

Although failure analysis of thermally damaged PCBAs can be challenging, a variety of techniques can be used to get critical information about the failure. A combination of visual inspection, material/contamination analysis, nondestructive evaluation and destructive techniques can achieve probable root cause for the failure. Even if root cause cannot be determined, it might be possible to rule out several scenarios based on the hardware. Throughout the process, documentation of the condition of the hardware and communication with the customer will be needed to develop a complete picture of the failure and manage expectations. It is critical to help the customer gain as much information about the failure as possible, so this information can then be used to make future design and manufacturing decisions/recommendations. ▫

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TABLE 2. Summary of Tools Used in Decapsulation

Technique	Amount of Damage	Equipment Needed	Speed	Hazardous Materials?
Chemical	Mild to Severe	None*	Varies	Yes
Plasma	Minimal	Plasma Etcher	Slow	No
Ion	Minimal	Ion Miller	Slow	No
Mechanical	Severe	None**	Fast	No
Laser	Minimal	Laser System	Varies	No

*Other than a hotplate, as needed. **Other than cutting and grinding/polishing equipment

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The Interaction of 2 SOLDER PASTE ALLOYS with 5 Surface Finishes

For spread and wetting performance, certain finishes stand out. **by PRITHA CHOUDHURY, PH.D., MORGANA RIBAS, PH.D., JOHN FUDALA and MITCH HOLTZER**

Electronic assemblers have myriad material and process choices to make, not limited to board materials, solder masks, laminate Tg's, components, surface finishes, assembly materials and design for manufacturing (DfM) process conditions. High-reliability alloys such as Innolot are designed to meet harsh automotive conditions and extend service life of the solder joint. Applications requiring higher operating temperatures and increased number of cycles to failure have benefited by implementing that alloy. While solder alloy selection is an important factor in determining reliability of the solder joint, considerations should be made for surface finish selection to further enhance performance. This study explores surface finish factors such as IMC formation, voiding and solder spread that contribute to reliability.

Each choice can have a significant impact on the in-service reliability and commercial success of the assembly. This multipart article will focus on data developed from an extensive study of surface finishes and solder pastes used by many global, high-reliability assembly manufacturers. The study included two commonly used solder alloys in paste form:

1. SAC 305 (96.5%Sn, 3%Ag, 0.5%Cu) powder size distribution (PSD) type 4 with novel "CVP-390" paste flux
2. Innolot (91.95%Sn, 3.8%Ag, 0.7%Cu, 3.0%Bi, 1.4%Sb, 0.15%Ni) PSD type 4 with the novel paste flux and five variations of surface finishes, including
   a. Organic solderability preservative (OSP) (MacDermid Enthone Entek Plus HT) using two thickness levels
   b. Immersion tin (Ormecon CSN)
   c. Immersion silver (MacDermid Enthone Sterling)
   d. Electroless nickel/immersion gold (ENIG) (MacDermid Enthone Affinity).

Characterizations of void creation, solder spread and initial intermetallic compound (IMC) thickness are discussed here. Details of IMC growth after thermal cycling, and the effect of the IMC thickness versus solder joint shear strength for each combination of solder alloy and surface finish, will be covered in the future. Results of data using multiple surface finishes and low-temperature soldering alloys are being developed and will be presented in a follow-up article.

Background

Metal-to-metal interconnects can be made using any of three common processes: welding, brazing or soldering. Welding requires reaching the melting temperature of the joined metal(s). Copper has a melting point of 1,085°C. Although welding copper to copper creates a very strong connection with no intermetallic compounds, the very high temperature eliminates its practicality for assembling components to an epoxy/copper-laminated substrate.

Brazing, according to the American Welding Society A3.0M/A3.0:2020 standard, requires reflow temperatures in excess of 450°C. Brazing is commonly used to bond copper-to-copper tubing used in water supply lines and HVAC systems. Many alloys of brazing materials are available; 80%Cu/15%Ag/5%P is a common copper-to-copper brazing alloy. Very strong joints are formed; however, the high temperatures required for brazing and the cost of a 15%Ag brazing alloy are prohibitive for circuit assembly applications.

Solder joints need to create a reliable mechanical bond with low electrical resistivity between component I/O joints and the copper pads on a printed circuit board. Copper pads on a PCB require a surface finish to prevent oxidization during the period between circuit board production and the assembly of surface mount components.

Two solder alloys and four common copper surface finishes were used in this study. Hot air surface leveling (HASL) copper surface finish was excluded from this study because of the issue with poor coplanarity. This became an issue when the RoHS (lead-free solder) and sub-0.8mm BGA pitch technologies converged in 2006, and has become more problematic as assemblers began placing BGA devices with 0.5mm and 0.3mm pitches. Use of HASL finishes has declined dramatically in all but non-ROHS compliant assemblies using larger (1.0mm and above) BGA components.

Experimental Design

This article discusses voiding resistance, spreading/wetting of

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the solder alloy on the surface finishes, and initial IMC thickness of paste alloys and surface finishes. Two different OSP coating thicknesses were used: 0.4µm and 0.6µm. Both zero and one reflow preconditioning cycle were tested for each combination of materials. Five replicate test vehicles were measured for each condition. Convection reflow was performed using a Heller 12-zone reflow oven. The reflow profile, shown in **FIGURE 1,** was relatively hot, with no nitrogen used for the preconditioning reflow. The same profile using <1,000ppm O_2 was used for final reflow.

Voiding inspection used a Phoenix Micromex system with a slightly different test vehicle. The print and reflow parameters were identical with all combinations of solder paste alloy and surface finishes.

Initial IMC thickness was measured. Results of IMC growth and shear testing differences after 2,000 thermal cycles will be reported in the second installment of this article.

Results and Discussion

Formation of a strong solder bond via the interfacial IMC is essential for the functionality and reliability of the package. With smaller solder joints, the influence of the IMC layer on joint reliability is more significant.[1] Solder joint reliability depends not only on the solder alloy but the component, PCB finishes, and the IMC formed within and at the solder/substrate interface.[2,3,4] The PCB surface finish forms a critical interface between the bare copper on the PCB and the component to be assembled and therefore is an important factor in the reliability of solder joints.[2,5] The most important function of the PCB finishes is to increase the solderability of the substrate by preventing oxidation of the copper pads on the PCB, even after extended times between the PCB fabrication and SMT assembly.

Voiding. A summary of the voiding results as a function of solder alloy, surface finish component type with zero and one prior reflow is shown in **FIGURE 2.** The results show the surface finishes examined had little effect on the measured voiding. The high-reliability Innolot alloy-based solder paste generated slightly more voids on average than the SAC 305 paste. Previous internal studies have shown reducing the peak reflow temperature and increasing the time above liquidus (TAL) reduces voiding with Innolot and the novel flux, but this was beyond the scope of this study.

A second result was a clear increase in voiding with the land grid array (LGA-256) device. Voids are reduced as volatile gasses from the solder paste flux escape from the solder joint during preheat and especially during the TAL portion of the reflow profile.

Low-offset LGAs can inhibit this outflow of vapors, leaving them entrapped in the solder joint. While LGA voiding was relatively low (<12%), this device clearly had measurably higher levels of voiding among the components tested. One-time prior reflow had a minor effect on voiding levels, especially with the LGA-256 device.

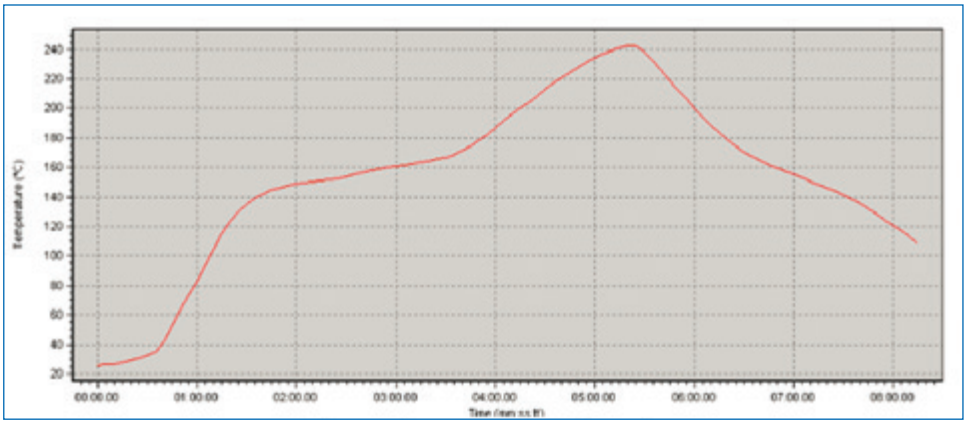

FIGURE 1. -155°C to 175°C, 70 sec. soak, 240°C peak, 70 sec. TAL.

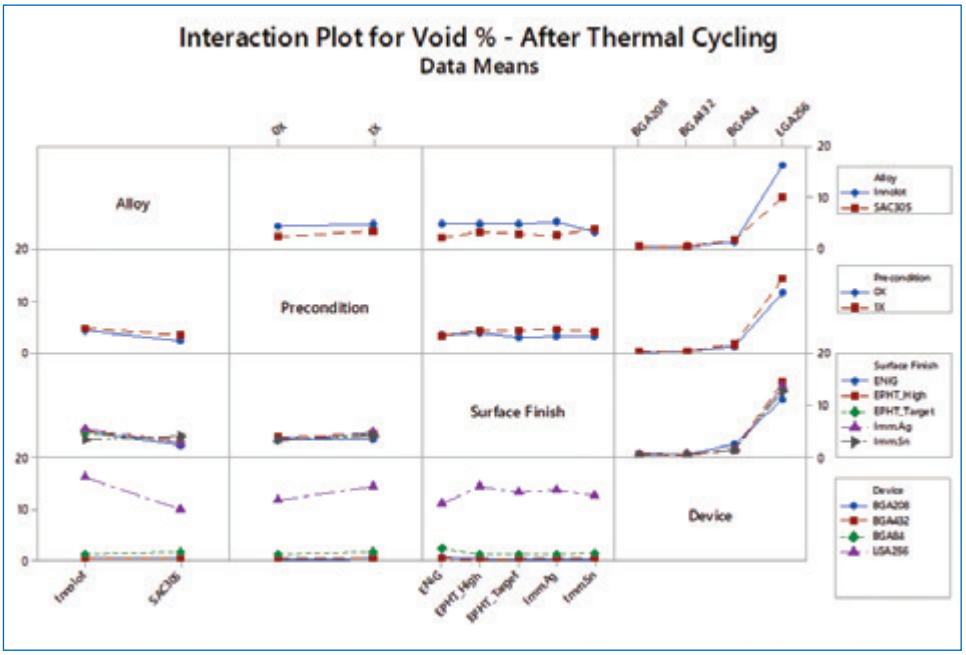

FIGURE 2. Voiding main interaction plots.

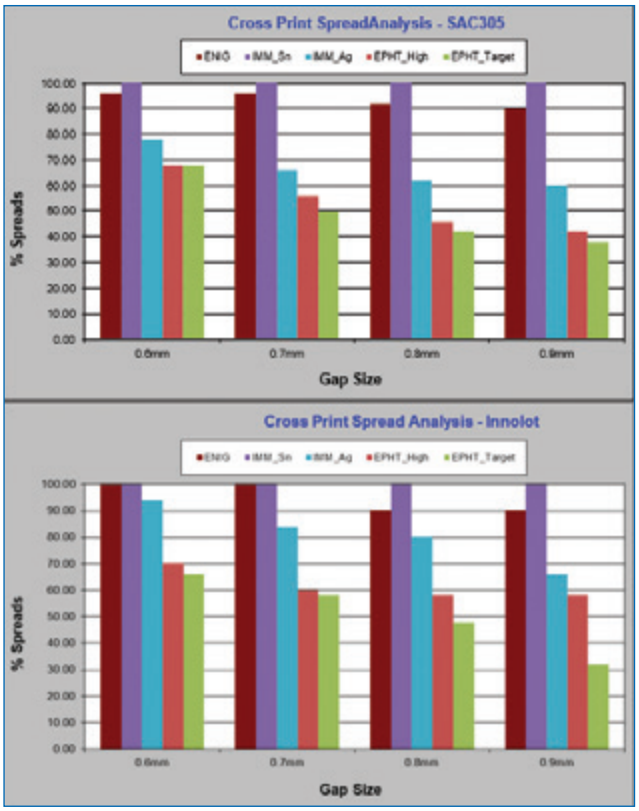

FIGURE 3. Cross-print spread results of SAC 305 and Innolot with each surface finish.

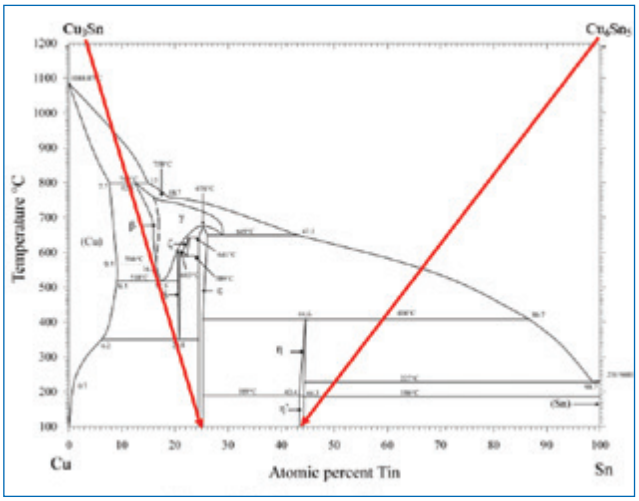

FIGURE 4. Tin-copper phase diagram.

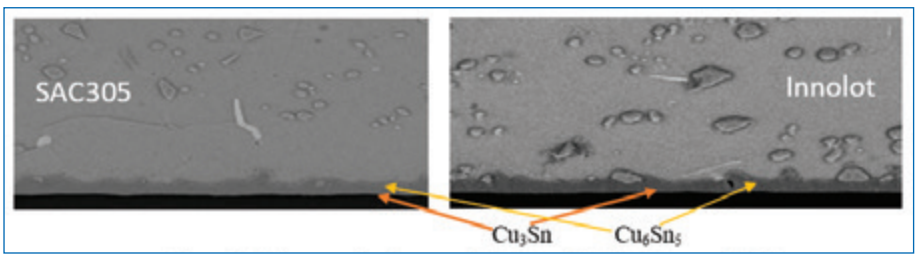

FIGURE 5. Micrographs of measured Cu_3Sn and Cu_6Sn_5 intermetallic layers.

Wetting. Formation of the interfacial IMC is strongly influenced by the processing parameters during reflow because of its effect on wetting and microstructure.[2,6] ENIG is unique in that the high-tin alloys tested interact with nickel to form $(Cu, Ni)_6Sn_5$. Some surface finishes could act as a barrier layer to reduce interdiffusion between the solder and copper base and thus reduce the formation of IMCs.[5,7]

Solder spread and wetting were measured using an internal test method developed by MacDermid Alpha known as the cross-print spread test. In this procedure, solder paste is printed and reflowed on parallel traces of the surface-finished copper. The distance between the traces is spaced in 0.1mm intervals ranging from 0.6mm to 0.9mm. The ability of the paste to bridge a larger gap is an indication of good spread **(FIGURE 3)**.

R1206 passive components with tin-coated nickel terminations and multiple-sized BGA components with SAC 305 spherical interconnects were used throughout the study.

A DEK Horizon printer and a 0.004" thick laser-cut stainless steel with no nanocoating was used to print the solder paste deposits. Each condition used the same print process settings (2"/sec. squeegee speed, 15 lb. of pressure and stencil snapoff speed @0.2"/sec.). A Fuji NXT-II pick-and-place machine was used to place the components into the paste deposits.

Cross-print spread results. In general, metallic surface finishes (ENiG, ImSn, ImAg) gave better results in the cross-print spread test **(FIGURE 3)**. The interesting finding is that a thicker OSP coating (0.6µm versus 0.4µm) showed better solder spread. The increased resistance to copper oxidation with the thicker OSP coating may be the explanation.

As-reflowed condition. Soldering of copper substrate involves eutectic melting (reflow) of solder bump and (ii) reaction of molten solder with substrate, resulting in the formation and growth of one or two intermetallics; i.e., Cu_3Sn (ε-phase) and Cu_6Sn_5 (η-phase). Mechanical bonding is mainly provided by the η-phase that has a peculiar scallop-like morphology.[8] The η-phase **(FIGURES 4** and **5)** changed from a scallop to a flat structure in the presence of as little as 0.05 wt% Ni.[9]

Conclusions

The lack of increased voiding after thermal cycling indicates neither intermetallic micro-cracks nor Kirkendall voiding was an issue with any of the combinations of solder paste alloys or surface finishes. Bulk voiding in the solder joint would not be expected to increase or decrease as a function of thermal cycling.

Innolot was prone to a slightly higher level of voiding. Reflow profile adjustment has proven to mitigate this issue.

A clear trend showed higher spread and wetting performance using the metallic (ImSn, ENIG, ImAg) pad finishes versus OSP. The thicker OSP finish (0.6µm)

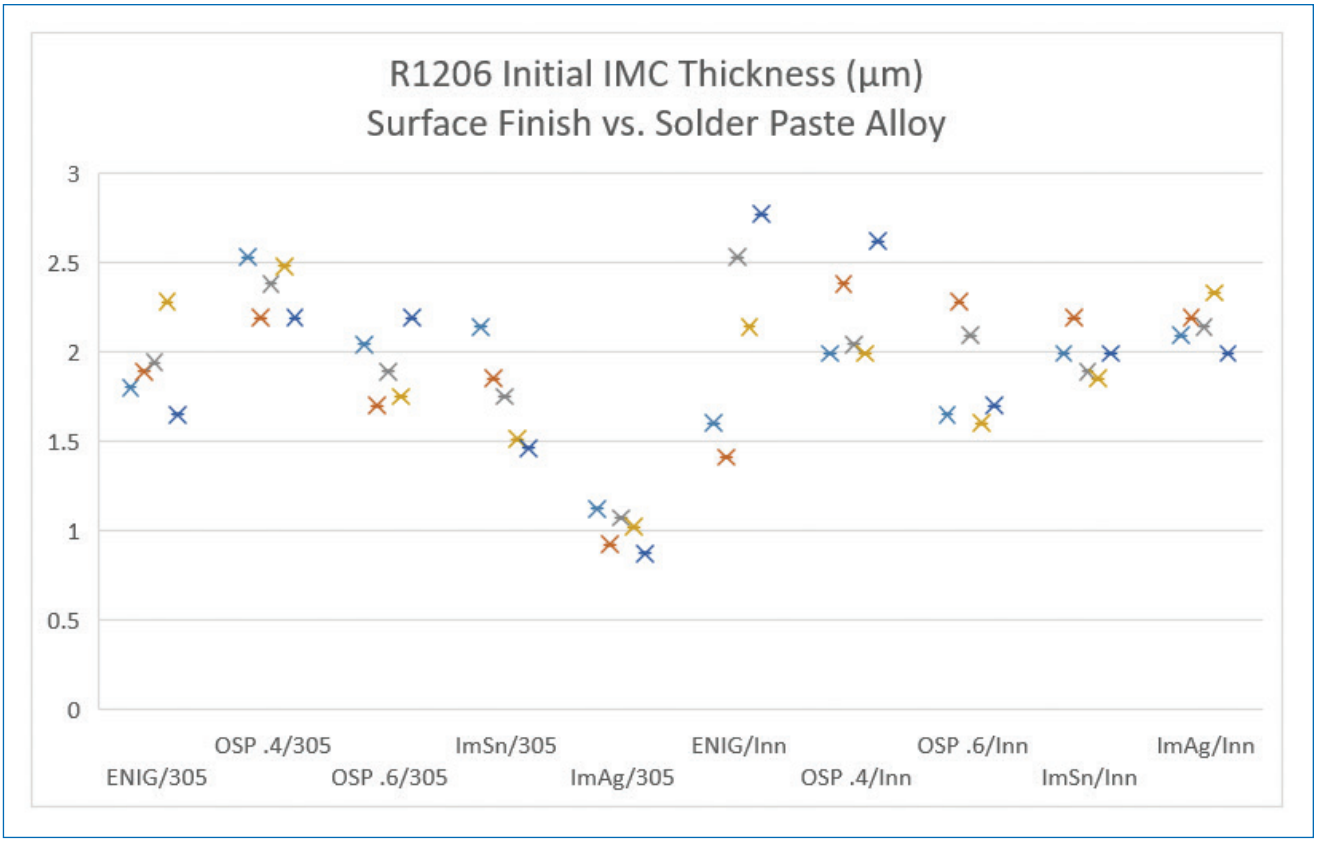

FIGURE 6. Initial IMC thickness in R1206 on different surface finishes with SAC 305 and Innolot pastes.

resulted in higher wetting performance with both the SAC 305 and Innolot-based pastes versus the 0.4µm thick OSP pad finish.

Each combination of solder alloys and surface finishes created a measured IMC between 0.9µm and 2.7µm. The data show the process capability (CpK) of the ENIG finish appears lower than the other combinations. The results of IMC growth after thermal cycling will be discussed in the next article in this series.

The follow-up article will explore the effect of solder alloy on each of the primary final finishes discussed here when exposed to harsh thermal cycling requirements (-40°/160°C). □

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State-of-the-Art Technology Flashes

Updates in silicon and electronics technology.

Ed.: This is a special feature courtesy of Binghamton University.

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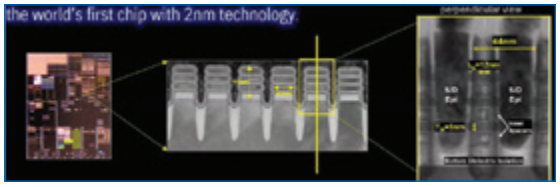
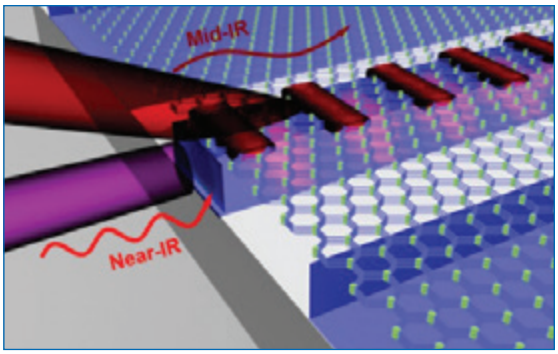
The **INTEGRATED ELECTRONICS ENGINEERING CENTER (IEEC)** at Binghamton University is a New York Center of Advanced Technology (CAT) responsible for the advancement of electronics packaging. Its mission is to provide research into electronics packaging to enhance our partners' products, improve reliability and understand why parts fail. Research thrusts are in 2.5/3-D packaging, automotive and harsh environments, bioelectronics, flexible and additive electronics, materials for packaging and energy storage, MEMS, photonics, power electronics, sensors, embedded electronics, and thermal challenges in electronic packaging. More information is available at binghamton.edu/ieec.

IBM unveils world's first 2nm chip technology. SIBM announced a breakthrough in semiconductor design and process with the development of the world's first chip announced with 2nm nanosheet technology. The new design is projected to achieve 45% higher performance and 75% lower energy use than today's 7nm chips. IBM said this new frontier in chip technology will accelerate advancements in AI, 5G and 6G, edge computing, autonomous systems, space exploration, and quantum computing. The technology would likely not be in high volume production until 2024. *(IEEC file #12281, Semiconductor Digest, 4/27/21)*



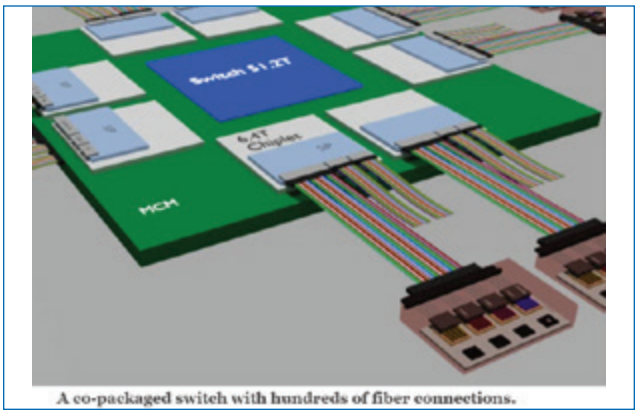
"Egg carton" quantum dot array could lead to ultralow power devices. University of Michigan researchers have developed a new approach by sending and receiving information with single photons of light using a "quantum egg carton" that captures and releases photons, supporting "excited" quantum states while it possesses the extra energy. Their experiment demonstrated the effect known as nonlinearity to modify and detect extremely weak light signals. This takes advantage of distinct changes to a quantum system to advance next-generation computing. As silicon-electronics-based information technology becomes increasingly throttled by heating and energy consumption, nonlinear optics is a potential solution. *(IEEC file #12154, Science Daily, 3/4/21)*

Waveguide design enables transmission of two types of light. Vanderbilt University researchers have developed a method of simultaneously transmitting two types of optical signals across a single chip. The work enables a dramatic increase in the volume of data a silicon chip can transmit over any period, and directly supports "lab-on-a-chip" capabilities. The number of waveguide channels, limited by space on a chip, defines the number of signals a chip can process. The hybrid hyperbolic-silicon photonic waveguide leverages the optical properties of both materials. In the mid-IF, the hBN crustal is able to support an optical mode called a hyperbolic phonon polariton, which permits the long-wavelength mid-IR to be focused and transmitted within deeply subwavelength structures and slabs. *(IEEC file #12162, Photonics Media 3/5/21)*



Aluminum-ion batteries offer promise. University of Nebraska researchers have developed a battery made with a pure aluminum anode, a graphene cathode, and an organic electrolyte. Aluminum-ion batteries promise significant improvements over lithium-ion technology. The ability to exchange three electrons per ion, compared to lithium's one, brings the potential for higher storage capacity. Al-ion batteries could also use cheaper/abundant materials, avoiding many of the issues that continue to plague Li-ion supply chains. A battery capable of both high storage capacity and ultrafast charging could open applications for energy storage, bridging the gap between battery and supercapacitor. *(IEEC file #12177, Science Daily, 3/12/21)*

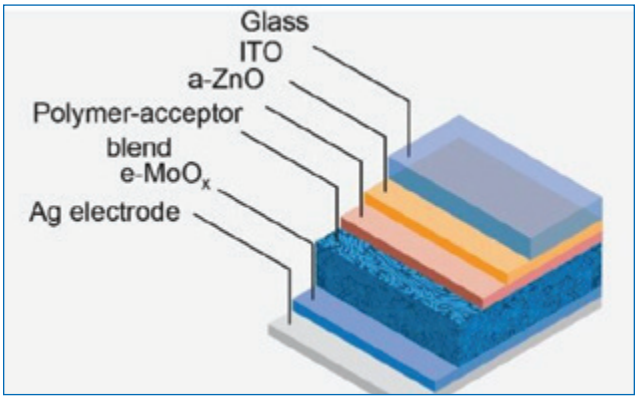
Silicon photonics startup focuses on connectivity. Teramount (Israel) researchers have developed fiber-to-silicon connectivity solutions for ultra-high bandwidth applications and demonstrated a 100x improvement in tolerance for assembling fiber to silicon chips. This breakthrough photonic-plug technology can enable next–generation technology for silicon photonics in data centers, mobility 5G and beyond. The approach simplified the packaging of silicon photonics chips by using a form of passive alignment instead of active alignment. The solution involves two main elements: a PhotonicsPlug that is flip-chipped on to the silicon photonics die while still part of a wafer; and a "bump" design element added to the silicon photonics chip next to the optical waveguide. *(IEEC file #12184, EE Times, 3/18/21)*



A co-packaged switch with hundreds of fiber connections.

Rare open-access quantum computer now operational. A Department of Energy open-access quantum computing testbed is ready for the public. Indiana University researchers recently became the first to begin using Sandia National Labs' Quantum Scientific Computing Open User Testbed, or QSCOUT. Quantum computers are poised to become major technological drivers over the coming decades. Scientists can use Sandia's QSCOUT for research that might not be possible at their home institutions, without the cost or restrictions of using a commercial testbed. "QSCOUT serves a need in the quantum community by giving users the controls to study the machine itself, which aren't yet available in commercial quantum computing systems." *(IEEC file #12180, R&D World, 3/17/21)*

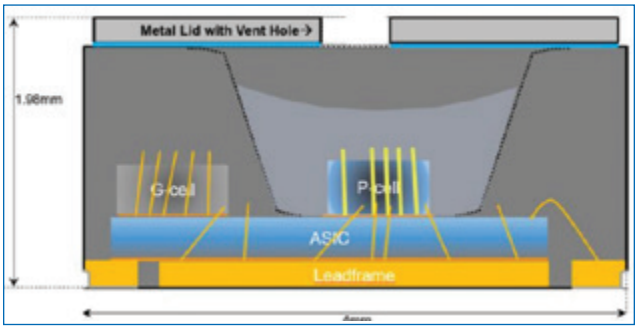
Plastic solar cells combine high-speed optical communication with energy harvesting. University of St Andrews resaerchers have demonstrated a plastic solar panel that combines indoor optical energy harvesting with simultaneously receiving multiple high-speed data signals by multiple-input multiple-output (MIMO) visible light communications (VLC). This is an important step for future self-powered data-connected devices. They demonstrated that organic photovoltaics (OPVs) are suitable for high-speed optical data receivers that can also harvest power. A panel of four OPV cells was used in an optical wireless communication experiment, receiving a data rate of 363Mb/s from an array of four laser diodes while simultaneously harvesting 11mW of optical power. *(IEEC file #12178, Science Codex, 3/2/21)*



Heat conduction record with tantalum nitride. Removal of heat from computer chips requires materials that are extremely good at conducting heat. Vienna University of Technology researchers have analyzed materials on an atomic level and found an excellent new heat conductor: theta-phase tantalum nitride (hexagonal θ-phase of tantalum nitride). The combination with nitrogen and the special atomic scale geometry makes the phase metallic, and it suppresses interactions of the heat-carrying vibrations with other vibrations and with the conducting electrons. It is those interactions that inhibit heat conduction in other materials. This form of tantalum nitride combines several important advantages, making it a record-breaking material with a thermal conductivity several times higher than silver and comparable to diamond. *(IEEC file #12205, Science Daily, 3/31/21)*

A breakthrough that enables practical semiconductor spintronics. It may be possible in the future to use information technology where electron spin is used to store, process and transfer information in quantum computers. Linköping University researchers have constructed a semiconductor component in which information can be efficiently exchanged between electron spin and light at room temperature. Quantum dots are considered to have a great potential as an interface to transfer information between electron spin and light, as will be necessary in spintronics and quantum computing. They demonstrated using an adjacent spin filter to control the electron spin of the quantum dots remotely. The quantum dots are made from indium arsenide (InAs), and a layer of gallium nitrogen arsenide (GaNAs) functions as a filter of spin. A layer of gallium arsenide (GaAs) is sandwiched between them. *(IEEC file #12221, Science Daily, 4/8/21)*

Miniaturized stacked die QFN for tire pressure monitoring system applications. Starting in the mid-2000s, active Tire Pressure Monitoring Systems (TPMS) have been mandated on many vehicles worldwide. The first systems were large and bulky, with significant electronics content. Since that time systems have become gotten more energy-efficient and form factors have decreased dramatically. Researchers from NXP Semiconductors have miniaturized a 1.0mm pitch, 7x7mm package size 24-lead stacked-die QFN down to a 4x4 mm package size QFN with 0.5mm pitch while still meeting automotive AEC Grade 1 reliability requirements. The three stacked die consisted of an ASIC, pressure sensor, and accelerometer. *(IEEC file #12182, SMTA, 3/17/21)*



Market Trends

The future of solar technology: New technology makes foldable cells a practical reality. With the recent development of foldable mobile phone screens, research on foldable electronics continues to be intensive. One key application of the foldable technology is in solar panels. A requirement for this is the ability to withstand the pressure of bending within a very small radius while maintaining its integrity and properties. Pusan National University researchers are developing solutions using single-walled carbon nanotube (SWNT) films. They embedded the conducting layer into a polyimide substrate, filling the void spaces in the nanotubes. Their resulting prototype is 7 micrometers thick, and the composite film exhibited exceptional resistance to bending, 80% transparency, and a power conversion efficiency of 15.2%. *(IEEC file #12130, Semiconductor Digest, 2/10/21)*

AI commission proposes $32 billion in AI research. The National Security Commission on Artificial Intelligence has approved a report on the path ahead to bolster US superiority in AI. The proposal calls for US funding of $32 billion in non-defense federal research by 2026. By 2025, the DoD and the intelligence community must be AI-ready. They dinged China for its domestic use of AI in facial recognition and related surveillance technologies. China's domestic use of AI is a chilling precedent for anyone around the world who cherishes individual liberty. Its employment of AI as a tool of repression and surveillance – at home and increasingly abroad – is a powerful counterpoint to how we believe AI should be used. *(IEEC file #12164, Fierce Electronics, 3/5/21)*

Lithium-ion battery market size to be worth $83.36 billion by 2027. The global lithium-ion battery market size is expected to reach $83.36 billion by 2027. Emergence and increasing popularity for electric vehicles (EV) is expected to drive the demand for lithium-ion battery in automotive industry. The automotive industry has been witnessing a palpable shift from using nickel metal batteries to lithium-ion batteries in plug-in vehicles and EVs. Beneficial physical characteristics such as small size and lightweight have bolstered the demand for li-ion (lithium-ion) batteries across the automotive industry. The development of energy storage technologies is enabling battery manufacturers to introduce advanced li-ion batteries that are compatible with the next-generation battery-operated, electronic products. Currently, various types of li-ion batteries, such as li-manganese oxide, li-ion phosphate, li-nickel manganese cobalt oxide, and li-cobalt oxide have high demand as advanced li-ion batteries across end-user industries. *(IEEC file #12165, Semiconductor Digest, 3/8/21)*

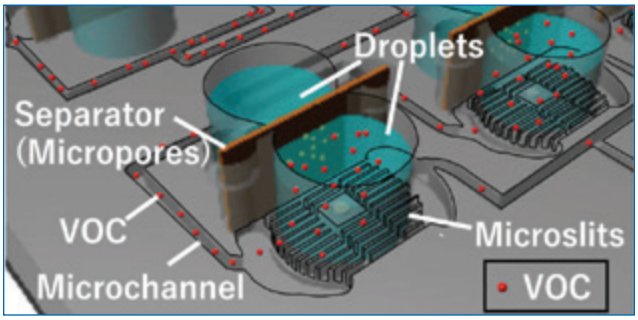
New Maine ferry to be hybrid electric. Casco Bay Lines has committed to an integrated hybrid-electric power and propulsion solution for its new vessel. The new 50-meter ferry will feature ABB Marine & Ports' hybrid power, propulsion and a shore charging system, supporting diesel-electric and zero-emissions battery-powered modes, as well as a combination of both. The vessel is expected to cut up to 800 tons of carbon dioxide per year, helping to improve air quality in Portland, Maine. Momentum for lower carbon footprint ferry operations continues to grow worldwide, and more US operators are replacing obsolete vessels to match regulatory and societal demands. *(IEEC file #12171, Science Daily, 3/9/21)*

Huge potential for electronic textiles made with new cellulose thread. Electronic textiles offer revolutionary new opportunities in various fields, in particular healthcare. Chalmers University of Technology researchers have developed a thread made of conductive cellulose, which offers fascinating and practical possibilities for electronic textiles. Sewing the electrically conductive cellulose threads into a fabric using a standard sewing machine, they succeeded in producing a thermoelectric textile that produces a small amount of electricity when heated. At a temperature difference of 37°C, the textile can generate 0.2mW of electricity. This cellulose thread could lead to garments with built-in electronic, smart functions, made from nontoxic, renewable and natural materials. *(IEEC file #12173, Science Daily, 3/10/21)*

SiC and GaN due for rapid expansion. TrendForce expects three factors to drive the rapid growth of the GaN and SiC markets in 2021 they are: Widespread vaccinations are projected to drastically curb the spread of the pandemic, thereby galvanizing a stable increase in the demand for base station components such as power inverters, Tesla began adopting SiC MOSFET designs for its in-house inverters the automotive industry has started to place increasing importance on third generation semiconductors, China will invest enormous capital into its 14th five-year plan starting this year. The total yearly revenue from GaN RF devices in 2021 is projected to reach $680 million, a 30.8% increase year-over-year, whereas GaN power device revenue is projected to reach $61 million, a 90.6% increase year-over-year. *(IEEC file #12186, Electronics Weekly, 3/15/21)*

Smell sensor combines biology with electronics. University of Tokyo researchers have combined biological smell sensors with an electrochemical electrode system to make a smell sensor. The sensor could detect concentrations on the order of parts per billion. The active part is a partnership or two of roughly sausage-shaped receptors normally found in cells of

yellow fever mosquitoes – an "olfactory receptor," which can detect a chemical, and an "olfactory receptor co-receptor," which has an adjustable ion channel through its length. When they lie next to each other through the thickness of a membrane, if the olfactory receptor comes in contact with a molecule it is sensitive to, it triggers the co-receptor to open its ion path briefly, chemically connecting one side of the membrane to the other. *(IEEC file #12191, Electronics Weekly, 3/16/21)*



Recent Patents

PCB assembly embedded thermal management using thin-film thermoelectric coolers (assignee: Honeywell), patent no. 10,939,537. Systems and methods for a printed circuit board assembly comprising a thermoelectric device at least partially embedded within the printed circuit board assembly are provided. The thermoelectric device is configured to adjust a temperature of the printed circuit board assembly based on the measurements of one or more sensors coupled to the printed circuit board assembly. Additionally, a control circuit is coupled to at least one thermoelectric device and one or more sensors, wherein the control circuit is configured to control at least one thermoelectric device,

Optical fiber system with photonic IC coupled to multicore optical fiber (assignee: Swanson Eric), patent no. 17/019229. Disclosed herein are optical integration technologies, designs, systems and methods directed toward optical coherence tomography (OCT) and other interferometric optical sensor, ranging and imaging systems wherein such systems, methods and structures employ tunable optical sources, coherent detection and other structures on a single or multichip monolithic integration. In contrast to contemporary, prior-art OCT systems and structures that employ simple, miniature optical bench technology using small optical components positioned on a substrate, systems and methods according to the present disclosure employ one or more photonic integrated circuits (PICs), use swept-source techniques, and employ a widely tunable optical source(s).

Semiconductor package having liquid-cooling lid (assignee: Raytheon), patent no. 16/989919. A semiconductor package includes a substrate; a die mounted on a top surface of the substrate in a flip-chip fashion; and a lid mounted on the die and on a perimeter of the substrate. The lid includes a cover plate and four walls formed integral with the cover plate. A liquid-cooling channel is situated between the cover plate of the lid and a rear surface of the die for circulating a coolant relative to the semiconductor package.

Stretchable Display Device (assignee: LG Display), patent no. 20210050404. A stretchable display device comprises a lower substrate; a plurality of island substrates spaced apart from each other and disposed on the lower substrate; a plurality of pixels defined on the plurality of island substrates; a plurality of base polymers disposed between adjacent island substrates of the plurality of island substrates; and a plurality of conductive particles distributed in the base polymer and electrically connecting a plurality of pads disposed on the adjacent island substrates.

Planar wafer-level fan-out of multichip modules having different size chips (assignee: IBM), patent no. 16/576,240. Package structures and methods are provided for constructing multichip package structures using semiconductor wafer-level fan-out techniques in conjunction with back-end-of-line fabrication methods to integrate different size chips into a planar package structure. The packaging techniques consider intra-chip thickness variations and inter-chip thickness differences and utilize standard back-end-of-line fabrication methods and materials to account for such thickness variations and differences. In addition, the back-end-of-line techniques permit formation of multiple layers of wiring and interlayer vias, which provide high density chip-to-chip interconnect wiring for high-bandwidth I/O communication between the package chips, and redistribution layers to route power/ground connections.

Solder joints for board level reliability (assignee: to Xilinx), patent no. 10,930,611. An integrated circuit assembly having an improved solder connection, and methods for fabricating the same are provided that utilize platelets within the solder connections to inhibit solder connection failure, thus providing a more robust solder interface. In one example, an integrated circuit assembly is provided that includes a package substrate having a first plurality of contact pads exposed on a first surface of the package substrate and a second plurality of contact pads exposed on a second surface of the package substrate. The second plurality of contact pads have a pitch that is greater than a pitch of the first plurality of contact pads. Interconnect circuitry is disposed in the package substrate and couples the first and second of contact pads. □

Utilizing Lean Manufacturing Principles to Cut Time and Cost in Test

Building functional test fixtures in-house mitigates several of the "seven wastes."

THE MANTRA OF the electronics manufacturing services (EMS) industry has been faster, better, cheaper for four decades, given that outsourcing isn't justifiable without a speed, quality or cost improvement over in-house processes. Continually delivering those benefits requires a focus on working smarter that relentlessly asks, "Where can we improve?"

Taiichi Ohno's concept of the seven wastes *(muda)* in manufacturing as part of the Toyota Production System (TPS) provides a good thought process for evaluating any process. To recap, those seven wastes are:

1. Waste of overproducing (no immediate need for product being produced)
2. Waste of waiting (idle time between operations)
3. Waste of transport (product moving more than necessary)
4. Waste of processing (doing more than what is necessary)
5. Waste of inventory (excess above what was required)
6. Waste of motion (any motion not necessary outside of production)
7. Waste of defects (producing defects requiring rework).

SigmaTron's Elk Grove Village, IL, facility continually focuses on improving efficiency in inspection and test. Recently, its test engineering team found that building functional test fixtures in-house drove improvements that mitigated several of the seven wastes.

An initial benefit was eliminating the waste of waiting. Ordering parts and building a fixture in-house reduced fixture development lead-time to three weeks from an average of six-to-eight weeks. Given supply and demand imbalances in many markets are driving original equipment manufacturers (OEMs) to speed new product introduction (NPI) processes wherever possible, reducing test fixture lead-time offers significant benefits.

While it will vary from fixture to fixture, in-house fixture design can also reduce test time. For example, in one recent case, the test engineering team designed a two-tiered fixture capable of testing a printed circuit board assembly (PCBA) and a higher-level assembly (HLA). The PBCA was placed on a bed-of-nails with a cable that plugs into the HLA. This combined fixture design cut PCBA test time in half and reduced the HLA test time to 30 seconds from 3.5 minutes. Typically, an outside vendor would have designed this as two fixtures, but in-house personnel were able to consider all product characteristics and anticipated production volumes when optimizing the design.

This design also eliminates the wastes of transport and processing that a two-fixture strategy would have represented. This improves quality outcomes by minimizing the defect opportunities that excess handling can create and adds cost benefits of faster test times and lowered nonrecurring costs.

Building fixtures in-house also shortens the test team's learning curve and enables them to tailor fixtures to project requirements more closely than may have been possible with an outside vendor.

The team also applied these concepts when determining how best to use flying probe test capabilities. A major driver for adding flying probe test capability is the convenience of a fixtureless test resource for NPI and pre-production builds while functional test fixtures were in development. A secondary benefit is the ability of flying probe test equipment to minimize troubleshooting time on functional test failures by exploiting its electrical test capabilities. Both benefits mitigate the waste of waiting.

For example, a flying probe tester's ability to detect device voltages helps it determine if the device has issues based on the voltage detected. This works for analog and digital components, as well as bipolar transistors. A higher voltage measurement is used for MOSFET devices. The voltage of interior transistors is measured on CMOS or logic gate devices. With BGAs, the capacitance value of the logic array can be measured and compared to the standard. This particular tester was selected because of an integrated automated optical inspection (AOI) feature, which enables visual inspection of SMT and through-hole component placements, in addition to electrical test.

Using flying probe in NPI and preproduction validation activities helps mitigate the waste of defects when the data are used to fine-tune the process. Combining test and inspection features minimizes the wastes of transport and processing. Using it as a troubleshooting tool helps minimize the waste of waiting by reducing technician time spent identifying the issue.

While the argument can be made that inspection and test activities are non-value-added processing, the reality is they are necessary non-value-added activities. Even when processes are kept within control limits, some components will fail. In the case of NPI and preproduction activities, inspection and test activities help quickly identify issues in the new process, which can lead to corrective actions that eliminate defect opportunities. Finally, finding ways to reduce test and troubleshooting time has more than just a cost benefit. In today's environment of supply not keeping up with demand, the ability to reduce lead-time or processing time is critical toward meeting OEM schedules in multiple industries. □

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What the Hell Just Happened?

Is round-the-clock engineering any way to live?

> IDLENESS, n. A model farm where the devil experiments with seeds of new sins and promotes the growth of staple vices. – Ambrose Bierce, *The Devil's Dictionary.*

WHAT MAKES A marketing expert a Marketing Expert?

What distinguishes a soft skill from a hard skill?

Is expertise conferred with an MBA at the tender age of 27? (How can somebody be considered a master of anything at 27?) Does wisdom come from meeting one's quota nine reporting periods out of 10? Is it filling up spaces with arcane verbiage, hoping the reader is overwhelmed and won't ask impertinent questions, like what does this all mean, and how does it benefit me?

Conversely, is acquisition of a hard skill dependent on one's mastery of differential equations, and number theory, and polar coordinates, and game theory, and Brier scores, and C++?

What is mastery? Who attests to it? Malcolm Gladwell says it takes 10,000 hours of practice to master a skill. Given the events of the past 14 months, have we mastered living and working at home? And Zoom?

What makes an educated person, and how does that translate to revenue-rendering job skills? Big picture: Does choosing electrical engineering over sociology make one a superior human being? How does one quantify superiority? Are engineers more adept at recognizing the untruth of alternative facts than humanities graduates? Why are so many technical professionals contemptuous of their nontechnical colleagues?

Ernest Hemingway is having a moment right now, perhaps because 60 years ago he hastened his demise, also because the media tends to fixate on anniversaries with zeros. Add guns, as Hemingway did, and the draw is irresistible. Prior to that 1961 infelicity, he wrote compact, understandable, hard-drinking, tough-guy prose that won him a Nobel and anointed him poster boy for creative writing teachers everywhere.

What can we learn by combining the literary spareness of Hemingway with the inherent tendency to dispense bullshit (for a fee) by marketing "experts" who tend to charge by the hour, if not by the word?

The Hemingwayesque response might be, "I paid for *that?*"

Much has also been written recently about McKinsey, a famous management consultancy. It made its name peddling advice to large companies with insecure management. Insecurities come from not knowing exactly how to position companies to benefit from present trends, and separating trends from passing fads. Is such advice worth the price? Consider history: Did the know-it-alls at McKinsey make the right calls on offshoring? Reshoring? Pandemic in between? Industry 4.0 when the world returns to some definition of normal?

What does it all mean? Especially to small companies like my own that don't have a prayer of affording such advice, now or anytime soon, but that need well-coached big companies to write the standards, attend the conferences, lobby the government, and generally stay on society's good side? Assuming, for discussion's sake, the advice was worth having in the first place. Are small companies, by virtue of their smallness, missing gateways and market share because they can't afford such counsel? With apologies to Hemingway, and John Donne, for whom does the bell toll?

None dares call them soft skills. You know, the ones we aren't supposed to showcase on our résumés. Because "team player" and "natural born leader" and "ability to navigate a pandemic with little preparation and no prior experience" are givens. Better the interviewer know you've mastered Python and Raspberry Pi.

Sure.

John Wayne Gacy had a soft skill. He loved kids. He was also good with knives. Quiet guy. Always kept to himself. Paid his taxes. Never bothered anybody. Kind of a "people person," in his own understated way. Funny smell coming from the direction of his house. You simply can't judge a book by its cover.

Why are so many American serial killers named Wayne?

What is your vision of hell?

- Eternal public radio pledge week?
- A nonstop flight to nowhere with a screaming toddler in the row behind you? Some Rapture. I want my money back.
- Fox News, in a road to Damascus moment, suddenly and inexplicably praising the virtues of wind and solar power? Or MSNBC warming to the Second Amendment?
- Life with or without video screens?
- A 72 rpm vinyl record of Ethel Merman belting out showtunes with a skip in it?
- Returning to the office?

A paper in the April 8 issue of *Nature* reports research findings that people favor complex solutions over simple solutions to problems, despite evidence that subtracting features is more efficient. No authors

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from McKinsey – or members of Congress – appeared in the byline.

Who knew Francis Galton was the father of standard deviations, regression to the mean, and an early version of crowdsourcing?

The Chinese say 996 (working 9:00 am to 9:00 pm, six days a week) is the key to success. To succeed, you can't restrict yourself to 40 hours. That is certain. But are 90 to 120 hours of work per week really necessary to get ahead, let alone get rich? Whither the anthill? All work and no play makes Johnny a disagreeable monopolist.

It is a really good time to be an economist. The market for slick-looking growth forecast charts is almost limitless. A lot of data to mine, with many ways to interpret how mass unemployment begins and ends. Fertile ground to test whether green jobs are good jobs.

This morning a post from a leading AOI manufacturer says there is no such thing as too much inspection. Wait one damn minute. I came of age in the '80s, when the Japanese were eating everyone's lunch, and W. Edwards Deming and JIT were the rage, and the plan was to build in quality and put quality establishments out of business. What the hell happened?

How quickly should one respond to an email or a Linked In request? Does an immediate or instant response connote desperation? How is desperation revealed in elapsed seconds or minutes between initial request and subsequent response, and how does one draw the line between keen interest and desperation? Who draws what impressions from this, and why?

"A POST FROM A **LEADING AOI MANUFACTURER** SAYS THERE IS NO SUCH THING AS **TOO MUCH INSPECTION.** WAIT ONE DAMN MINUTE."

Remember this fundamental truth: Google and Facebook are, at their core, advertising companies. Recent political controversies merely distract from the main prize. Strip away the techie veneer and that's what you get: an updated version of the *Man in the Grey Flannel Suit,* with hoodies.

This concludes a compendium of lockdown-induced contemplation. You may now exit the kaleidoscope of my mind as the ride comes to a complete stop.

Now we're vaccinated. Back to work. Get organized. Focus. Clean out the mental attics.

Endure customers trying to enforce their vision of restored normalcy.

Oh, them.

Like the third party deputized by a customer to conduct a quality survey on one week's notice. Never mind 11 years' doing business, plus all the right aerospace certifications. Oh no, they had to see for themselves. Answer #1: We don't do onsite quality surveys on one week's notice. Answer #2: We don't do onsite visits, period, until further notice (still playing it safe and waiting for widespread vaccinations to have their effect). Learn Zoom or send forms to be filled out. They went away. Nice try.

Or the engineer who really wants to sit with our x-ray technician while we inspect his product. He wants to be able to direct us where to look (as if we can't figure it out) and where to take pictures. He also can't let his product out of his sight. Something about IP. He earnestly sets forth his reasons for company policy. We respond with equal zeal that extraordinary circumstances demand the inflexible abstract rules be bent, and that he accept our terms and stay remote. He bends the rules; we get the job.

Or the program manager who insists we maintain a program build schedule despite our principal project engineer's sudden, unplanned serious illness. And a pandemic. And an OEM design engineer with only the faintest grasp of the capabilities of the Keysight 3070 in-circuit test system. Minor inconveniences became major when the PM attempted to micromanage the transition from the ill engineer to his replacement. What followed was a bevy of helpful suggestions like, "Can you call Keysight and ask if in the midst of this pandemic by chance they have additional idle resources to add to this project?" (We did, and Keysight didn't.) And, "Could you assure us that any testing activity on our boards be done separately and by separate people from the engineer debugging our other programs?" And of course, "Can we please get a day-by-day list of project milestones, including expected completion dates for each of the 26 power-up test steps contained within our engineer's statement of work? Include in your spreadsheet both expected as well as achieved dates, and be prepared to explain any deviations from projected completion dates." Program debug and defined project milestones don't coexist well. They didn't in this case either.

Or every customer who now thinks they have license to do business 24/7/365, and not because of the difference between Asian and American time zones. These are locals. The unspoken assumption is work time is endless, and endlessly flexible, and suppliers should be endlessly available to inquiring clients. Those who desire to compete ignore these unwritten rules at their peril.

What do McKinsey's bright young things make of that over their spreadsheets? Did they anticipate round-the-clock availability emerging from our enforced hermit life?

Ernest Hemingway is not available for comment. ▫

Age Causes Knee Damage

Soldering excursions can lead to visual process indicators.

BOB WILLIS
is a process engineering consultant; bob@bobwillis.co.uk. His column appears monthly.

THIS MONTH WE look at cracks in plated through-holes around the knee of the hole. **FIGURE 1** shows very small via holes that were subjected to multiple lead-free soldering steps, then underwent thermal cycling with no failures but a little cracking.

The cracks visible in the microsection were found on via holes not after the initial two reflow steps and wave-soldering test boards, but after further temperature cycling at -55° +125°C. No electrical failures were detected, just the impact of repeated stressing of the copper. It is a good demonstration of how reliable a board can be, but all that stress does have some visual impact. Care must be taken during microsection preparation to see these indicators.

We have presented live process defect clinics at exhibitions all over the world. Many of our Defect of the Month videos are available online at youtube.com/user/mrbobwillis. Find out how you can share our new series of Defect of the Month videos to explain some of the dos and don'ts with your customers via CIRCUITS ASSEMBLY: https://bit.ly/3mfunlF. □

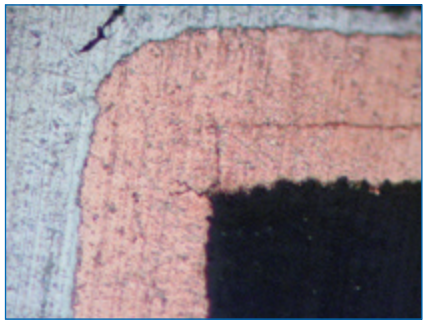

FIGURE 1. Cracks in a plated through-hole.

Around the World, continued from pg. 11

Lava, a handset ODM and EMS for such firms as **Nokia** and **Motorola,** is considering an IPO.

Lorain County Community College awarded three graduates with the community college's first bachelor of applied science in microelectronic manufacturing (MEMS).

Microart Services, a UK EMS provider, has joined forces with engineering firm **Berlin KraftWorks.**

More than 50 CEOs in May urged US Commerce Secretary Gina Raimondo to take concrete steps to address challenges confronting the entire US electronics supply chain.

Nortech Systems is applying for the Employee Retention Credit to support ongoing investment in its front-line workforce and to drive increased manufacturing output to meet customers' rising demand for mission-critical parts. The EMS company estimates the ERC will, if the application is successful, total $5 million in fiscal 2021.

Omega EMS acquired energy storage firm **TeckQuest.**

Orient Semiconductor Electronics is looking to scale up its EMS business beyond the electronics sector, while strengthening its collaboration with backend house **Chipbond Technology** in the fields of 5G, IoT and automotive electronics.

OSI Electronics added a **Europlacer** SP710-AVi screen printer and **ALeader** 3-D solder paste inspection at its UK plant.

PG Electroplast, one of India's leading electronics manufacturing companies, is raising Rs 76.6 crore from investors for plant expansions.

Prime Technological Services installed a **Test Research Inc.** TR7007QI SPI.

The US Lighting Group intends to form a new division, **RVtronix,** to design, manufacture and distribute electronics to the RV Industry.

VDL Groep will make a public offer for all issued and outstanding shares in the capital of EMS provider **Neways.**

Robotics startup **Wyzo** has developed a so-called "sidebot" for pick-and-place applications in the manufacturing space.

XDry named **MaRC Technologies** exclusive representative in the Pacific Northwestern US.

Yamaha Motor Europe Factory Automation announced a distribution agreement with **S.D.A. s.r.o.** in Slovakia and Czech Republic.

Z-Axis added a **Xeltek** SuperBot 5e robotic IC programmer, and a Universal Instruments Radial 88HT through-hole insertion machine.

Dragos Maciuca
Executive Technical Director
Ford Motor Company

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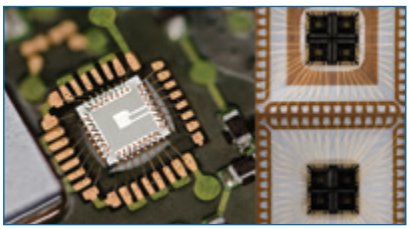
Takaya
takaya-itochu.com



HENKEL ABP 8068TD

Loctite Ablestik ABP 8068TD high thermal die attach paste is for use in applications where no die back-side metallization is required. Is for bare silicon die integration and high-power applications. Dissipates heat in applications where bare silicon die are used. Bulk thermal conductivity of 50 W/m-K.

Henkel
Henkel.com

ECD OVENSENTINEL WITH PROFILE SNAPSHOT

OvenSentinel continuous monitoring technology now has Profile SnapShot, a one-button, on-demand oven profile confirmation that delivers a data file, rather than a profile image only. Reduces requirement for incremental profiling using instrumented assemblies. Delivers instantaneous view and generated data set of oven profile, allowing validation and documentation of oven conditions for reflow soldering. Calculations can be instantly captured and displayed. Integrates TrueProfile traceability.

ECD
ovensentinel.com

OTHERS OF NOTE

NORDSON EFD 70CC OPTIMUM

70cc Optimum syringe barrels hold assembly fluids, such as adhesives, epoxies, sealants and solder pastes. Are for electronic applications such as underfill, potting and conformal coating. Reduce number of fluid changeouts in automated manufacturing processes. Come in clear resin for general purpose applications and UV-blocking amber resin for light-sensitive assembly fluids. Consistent internal diameter maintains proper seal with piston.

Nordson EFD
nordsonefd.com

EUTECT SENSITIVE WIRE FEEDER

Sensitive Wire Feeder can be used in conjunction with a laser, iron or induction system for soldering assemblies. Drive is now shielded by a metal cover, improving EMC compatibility. New signal filter software improves measuring accuracy and stability during wire feed. Weight has been reduced 11%, permitting the SWF to be moved more dynamically when integrated on a robot arm.

Eutect
eutect.de

PACIFIC TRINETICS CELSUS-20

Celsus-20 smart storage cabinet is for SMT component reels. Stores 6,400 reels in less than 26 sq. ft. of space. Auto material retrieval from bill of material reportedly eliminates errors. Preparatory software controls each component's MSD and lifecycle. Stores electronic components in reels, tubes, trays and packs. Configurable to store any type of large or small products.

Pacific Trinetics
ptchips.com

KIC WPI

WPI (Wave Process Inspection System) brings process monitoring, process control and traceability to the wave solder process. Provides automatic profiling, including dwell time and parallelism measurement for each production board, real-time preheat and wave analytics, and automatic SPC charting.

KIC
kicthermal.com

DYMAX 9906-AA

9906-AA light and/or heat-curable cationic epoxy is for active alignment of camera modules, optical components, LiDAR, and other ADAS assemblies used in automotive apps. Low volumetric shrinkage, high Tg, and low CTE. Has 85°C/85% RH resistance, exhibits less overall movement through thermal excursions, and features higher viscosity and thixotropy to maintain bead shape upon dispense. Can be refrigerated and shipped/stored at 1°-5°C and not frozen. Meets NASA ASTM E595 low-outgassing specifications.

Dymax
dymax.com

TRI TR7007 SII ULTRA

TR7007 SII Ultra 3-D high-speed solder paste inspection performs at speed up to 180 cm^2/sec. Inspects low solder bridges and compensates board warpage for eliminating local PCB deformation. Eases data exchange between production line and MES to enable data traceability for connected factory. Uses YMS 4.0 Industry 4.0 data-driven management system.

Test Research Inc.
tri.com.tw/en/index.html

In Case You Missed It

This column provides abstracts from recent industry conferences and company white papers. Our goal is to provide an added opportunity for readers to keep abreast of technology and business trends.

Connectors

"Impact of Thermal Cycling on Cu Press-Fit Connector Pin Interconnect Mechanical Stability"

Authors: Yeon-Jin Baek, *et al.*

Abstract: Compared with a BGA interconnection press-fit pin connector, interconnects are expected to have a different degradation mechanism. In this study, the impact factors affecting the reliability and degradation mechanism of press-fit connector pins were investigated. The bonding strength of inserted pins was measured before and after thermal cycling at room temperature and elevated temperature conditions. Bonding strength of the press-fit pins to the PCB copper barrel was observed to increase after thermal cycling. Development of an intermetallic compound between the copper pin and the copper barrel is observed. The microstructure of the press-fit connector pin and the barrel and localized stress and strain levels were analyzed by electron backscattered diffraction, including inverse pole figure maps, grain reference orientation deviation maps, and strain contouring maps. Along with the increase of pull strength after thermal cycling, an increase in residual stresses was observed, while strain contouring maps exhibited a decrease in localized strains at the interface between a press-fit pin and copper barrel. (*Journal of Electronic Materials,* June 2021)

Component Authentication

"How Nanotech Can Foil Counterfeiters"

Authors: Roozbeh Tabrizian and Swarup Bhunia

Abstract: Radio frequency (RF) nanoelectromechanical systems (NEMS) are devices that don't have to be visible to be scanned. Consisting of two 50nm-thick conductive layers of indium tin oxide, with a 100nm-thick piezoelectric film composed of a scandium-doped aluminum nitride, they can be fabricated with lithographic techniques similar to those used to make ICs. An etched pattern includes a ring in the middle suspended by four slender arms. That design leaves the circular surface free to vibrate. When the film is mechanically deformed, the material generates an electric voltage across it: the converse piezoelectric effect. A coil on the perimeter of the tag is connected at one end to the top conductive layer and on the other end to the bottom conductive layer. Subjecting the tag to an oscillating magnetic field creates an oscillating voltage across the piezoelectric layer, as dictated by Faraday's law of electromagnetic induction. The resulting mechanical deformation of the piezo film in turn causes the flexible parts of the tag to vibrate. A network analyzer is then used to scan for the unique resonances of an individual tag. (*IEEE Spectrum,* May 28, 2021, https://spectrum.ieee.org/consumer-electronics/portable-devices/how-nanotech-can-foil-counterfeiters)

Flexible Electronics

"Pioneering Chemistry Approach Could Lead to More Robust Soft Electronics"

Authors: Susil Baral, Chunming Liu, *et al.*

Abstract: A new approach to studying conjugated polymers made it possible to measure the individual molecules' mechanical and kinetic properties during polymerization reaction. The insights gained could lead to more flexible and robust soft electronic materials, such as health monitors and soft robotics.

Conjugated polymers are essentially clusters of molecules strung along a backbone that can conduct electrons and absorb light. This makes them a perfect fit for creating soft optoelectronics, such as wearable electronic devices; however, as flexible as they are, these polymers are difficult to study in bulk because they aggregate and fall out from solution. Cornell University researchers employed an approach called magnetic tweezers to stretch and twist individual molecules of the conjugated polymer polyacetylene. Through use of novel single-molecule manipulation and imaging approaches, this work provided the first observations of single-chain behaviors in conjugated polymers, which lays the foundation for the rational design and processing of these materials to enable widespread application. (*ScienceDaily,* Jun. 16, 2021, sciencedaily.com/releases/2021/06/210616143239.htm)

"High-Performance Flexible Nanoscale Transistors Based on Transition Metal Dichalcogenides"

Authors: Alwin Daus, Sam Vaziri, *et al.*

Abstract: Two-dimensional semiconducting transition metal dichalcogenides could be used to build high-performance flexible electronics. However, flexible field-effect transistors (FETs) based on such materials are typically fabricated with channel lengths on the micrometer scale, not benefitting from the short-channel advantages of 2-D materials. Here, the authors report flexible nanoscale FETs based on 2-D semiconductors; these are fabricated by transferring chemical-vapor-deposited transition metal dichalcogenides from rigid growth substrates together with nano-patterned metal contacts, using a polyimide film, which becomes the flexible substrate after release. Transistors based on monolayer molybdenum disulfide (MoS_2) are created with channel lengths down to 60nm and on-state currents up to 470μA μm^{-1} at a drain-source voltage of 1V, comparable to the performance of flexible graphene and crystalline silicon FETs. Despite the low thermal conductivity of the flexible substrate, it was found heat spreading through the metal gate and contacts is essential to reach such high current densities. (*Nature Electronics,* Jun. 17. 2021, nature.com/articles/s41928-021-00598-6)

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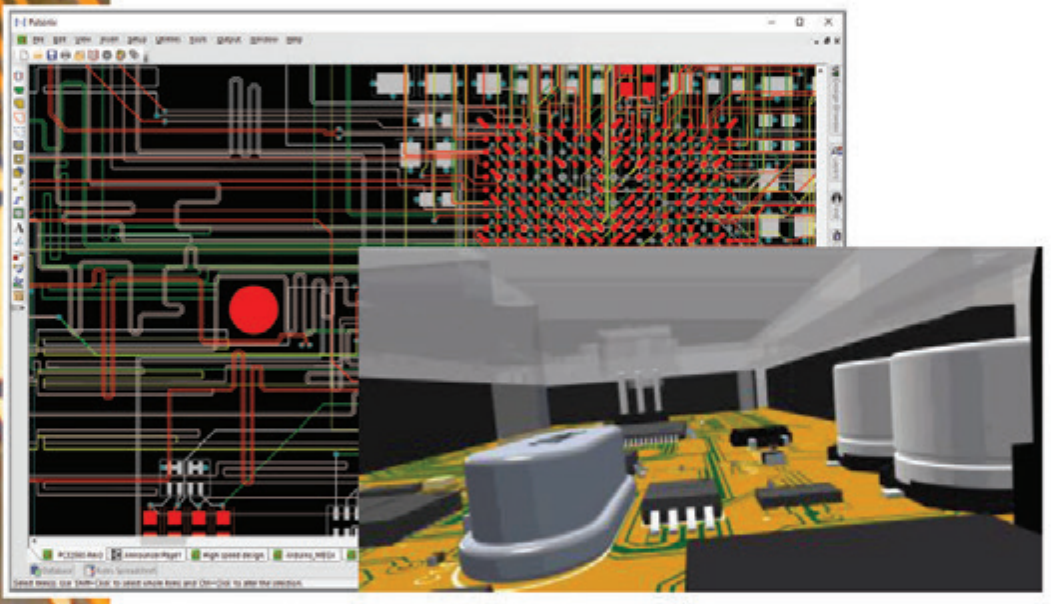

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