Keeping the PDN Running Smoothly, pg. 24

UP Media Group

PRINTED CIRCUIT DESIGN & FAB
CIRCUITS ASSEMBLY

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April 2021

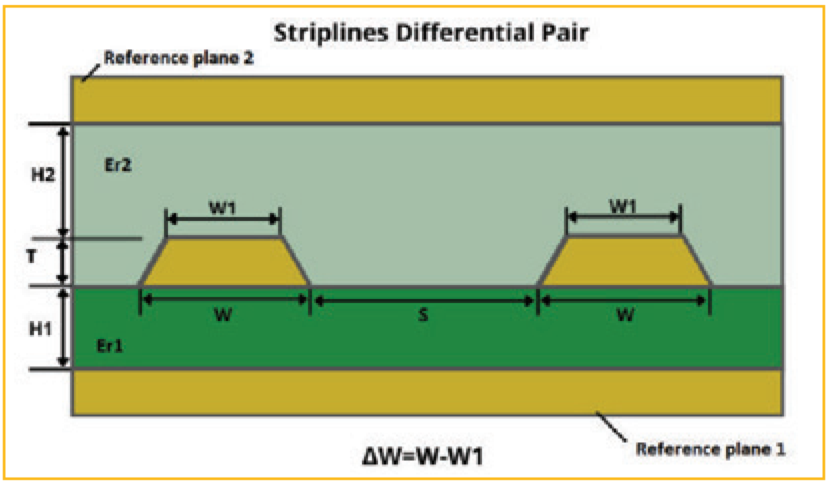
in

Finding the Right Model for Plating

AI for PCB Designers

Signals Move in Spaces, Not Traces

Catching Hermes



What affects impedance

In summary, the impedance of PCB signal traces is affected by:

- The height of the dielectric layer between the signal trace and the reference plane
- The width and the thickness of the signal trace
- The dielectric constant of a dielectric material

Dielectric materials used in PCB constructions are categorized in two types: copper clad cores and prepregs. The various types of cores and the prepregs usually have different dielectric constants, as specified in the detailed data available from the laminate manufacturer.

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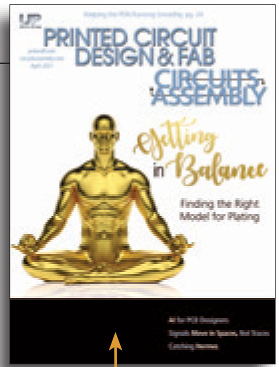
FIRST PERSON

MONEY MATTERS

TECH TALK

DEPARTMENTS

FEATURES



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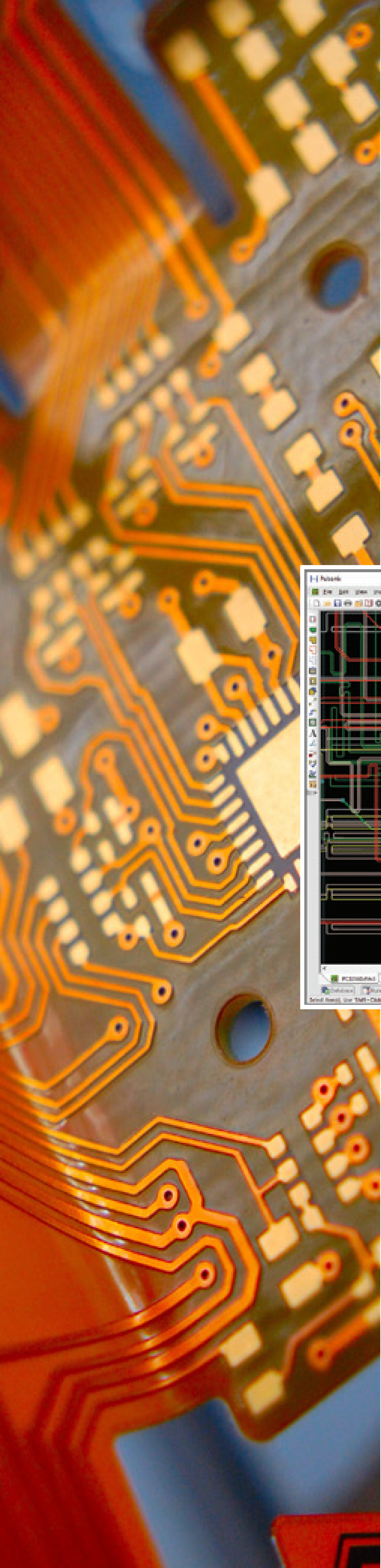

MIKE
BUETOW
EDITOR-IN-CHIEF

In Defense of Diversity

MUNITIONS ARE COOL AGAIN. Well, maybe they always were. But the emphasis by North American manufacturers on procuring defense contracts has perhaps never been greater.

In the throes of the dotcom meltdown of late 2001 to early 2003, when China and Taiwan hoovered up the vast majority of the Western PCB market, forcing those hardy remaining souls to repurpose their business plans, the Pentagon became an unwitting savior. Manufacturer after manufacturer pivoted from the "3Cs" (computers, communications, consumer) to CET&I (military communications, electronics, telecommunications, and intelligence technologies). They eschewed past complaints of onerous red tape and sprung for the certifications to elbow their way into the Pentagon supply chain.

There wasn't much choice at the time. It was military or bust.

Going back to 2001, the United States made about 45% of the world's electronics equipment. Defense and related high-rel sales made up less than 10% of the US domestic fabrication market, which at the time was coming off a record year at around $11 billion in production output spread across 650 or so facilities.

We all know what happened.

But about that cure. As we reported in last month's digital edition ("US Defense Suppliers Have Begged for Help. A Pandemic Helped Them Get It"), 145 of the 202 printed circuit board facilities in the US as of 2017 supplied the US Department of Defense in some manner.

My concern is that North America might put all its eggs in one basket. This is more an issue for fabricators than assemblers, since the former is less automated and requires more skilled labor hours per $1 million of product shipped. Also, the workforce is aging faster on the fab side in the West, and it's generally more difficult for fabricators to recruit new engineers and operators, as the industry as a whole and the companies are smaller, and the opportunities for career growth are fewer. Quick swings in demand can truly hamstring a company in the short-term, and many board shops don't have access to enough capital to sustain long downturns.

Despite the significant hoops, there's no question military work holds appeal. The end-customer pays. The margins are relatively steady. There is always the promise of future business, even if the demand volume tends to be somewhat administration-dependent.

I recall a warning IBM economist Phil Swan made in 2001 at an IPC TMRC meeting. In tough times, he said, governments look inward, which could further upset the supply chain. "Most legislators tend to be provincial when push comes to shove. Only 40% of the US Congress has a passport. They're not in touch with the rest of world any more than they have to be. The majority haven't served in a war and don't have that experience. It wouldn't take a lot for them to shut the door and [hurt] economic globalization." How prescient does that sound today?

At that time, the North American fabrication market was still a $11 billion entity. Today it's less than a third of that. My best estimate pegs the Defense Department procurement of printed circuit boards at a little over $1 billion annually. That's not far off where it was 20 years ago.

As such, I admit to being concerned when I see so many companies focusing their efforts on the A&D market. Commercial aerospace, as we've seen, is the definition of boom/bust (absolutely no pun intended. Seriously.). Military is steadier, but less so than generally appreciated. It's not uncommon for the CET&I budget to gyrate 10% in either direction year-over-year.

For those still doubting, keep this in mind: Just 10 years ago, in fiscal 2011, the US defense budget for CET&I was $17.7 billion. Two years later, it was $13.6 billion, a reduction of almost 24%.

Is your business ready for that?

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P.S. We have three great webinars coming up in the next two months: Chrys Shea on screen printing, Greg Papandrew on reducing bare board procurement costs, and Dr. David Bernard on getting the most from your x-ray inspection system. Visit pcb2day.com for details.

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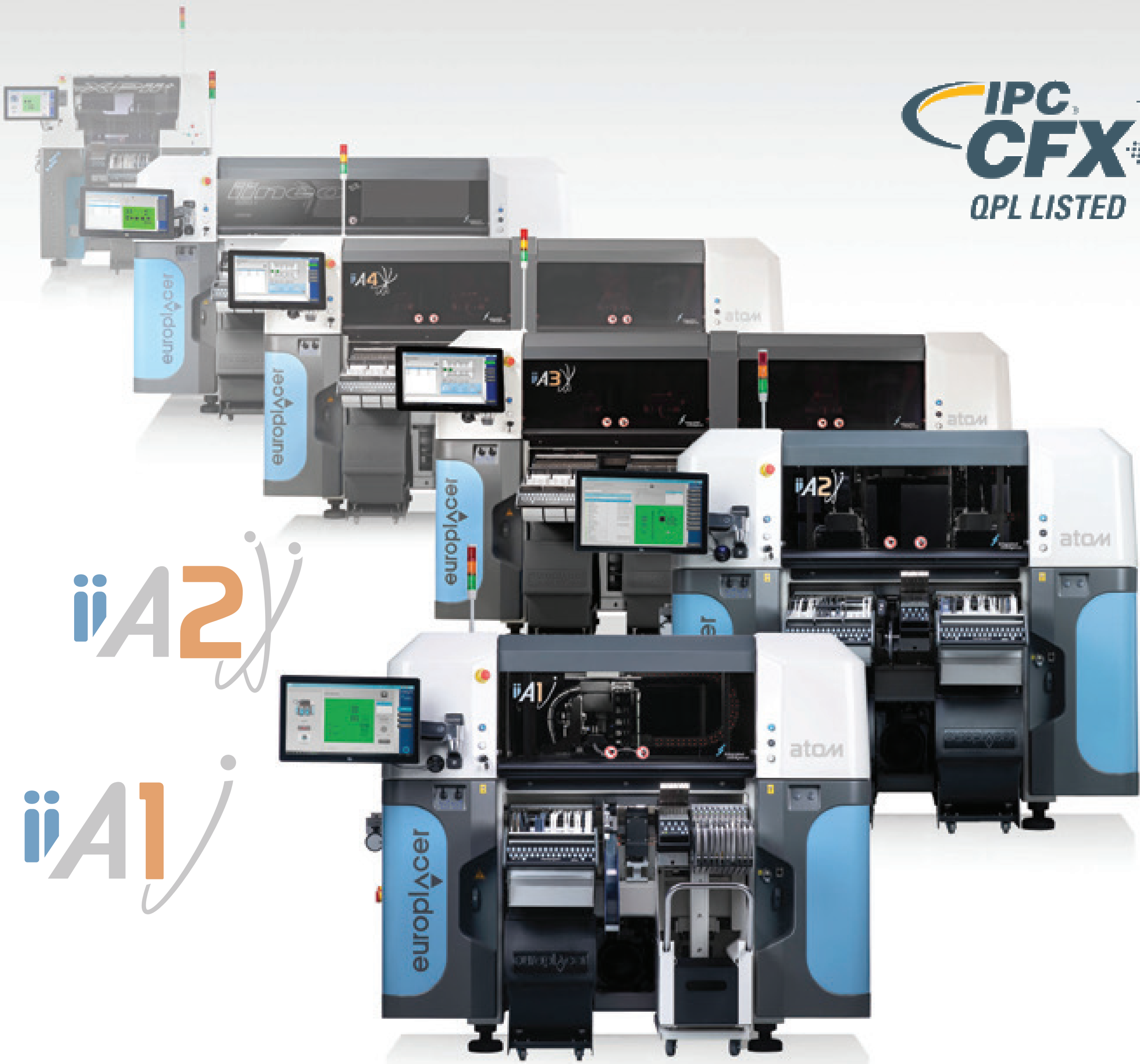

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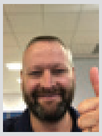
PCDF People

The best technical conference paper of IPC Apex Expo 2021 is "Signal Integrity, Reliability, and Cost Evaluation of PCB Interlayer Crosstalk Reduction" by **Sarah Czaplewski,** IBM.



Elmatica named **Craig Haywood** senior technical advisor. He spent the past 14 years at Amphenol Invotec.

Hirose Electric USA named **Shinya (Sid) Tono** president and COO.

IPC inducted **Karen McConnell** into its Hall of Fame, given to individuals who have provided exceptional service and advancement to IPC and the electronics industry. McConnell supports numerous IPC standards development committees, including the Land Pattern Committee, Design for Excellence (DFX) Subcommittee, Generic Requirements for Digital Twin Task Group, CFX Subcommittee, Terms and Definition Committee and Electronics Documentation Committee.

Orbotech named **Avi Greenberg** general manager Americas and vice president sales.

PCDF Briefs

Autodesk and SnapEDA have partnered to release a new app for Fusion 360.

Bittele Electronics updated its *DFM Handbook* and *DFA Handbook.* Both detail best practices for printed circuit board fabrication and assembly.

Calumet Electronics announced its SBA certification as a HUBZone business. Calumet also won the **IPC** Peter Sarmanian Corporate Recognition Award for support of individuals through technical and management programs.

The Design Automation Conference and Semicon West have been rescheduled to Dec. 5-9.

The **ExpressPCB** Plus PCB Design Suite (ExpressSCH Plus and ExpressPCB Plus version 3.0) now includes integrated search and download for components using **SnapEDA.**

High data throughput and innovative thermal management may lead to a revolution in systems design that places the burden of electronics cooling on the enclosure more than on the card.

IDEX Biometrics signed an agreement with **MFLEX** to mass produce circuit boards for biometric payment cards.

DuPont to Acquire Laird in $2B+ Deal

WILMINGTON, DE – DuPont has entered into a definitive agreement with private equity firm Advent International to acquire Laird Performance Materials for $2.3 billion, which will be paid from cash on hand. The transaction is expected to close in the third quarter, subject to regulatory approvals and other customary closing conditions.

Laird provides high-performance electromagnetic shielding and thermal management, as well as performance components and solutions that manage heat and protect devices from electromagnetic interference. It has a workforce of more than 4,300 employees with a global network of 11 manufacturing sites in North America, Europe, and Asia and 2020 revenues of $465 million.

The transaction brings together DuPont's films, laminates and plating chemistry with Laird's electromagnetic shielding and thermal management solutions.

"The acquisition of Laird Performance Materials is a significant step in advancing DuPont's strategy to grow as a global innovation leader and premier multi-industrial company," said Ed Breen, executive chairman and CEO, DuPont. "Laird is a strategic and complementary addition to the electronics and industrial business, and our applied material science expertise, together with Laird's industry-leading application engineering capabilities, further strengthens DuPont as an essential partner for major electronics OEMs and manufacturers."

DuPont expects to realize approximately $60 million in pretax run-rate cost synergies by the end of 2024, the majority in the first 18 months post-closing. The estimated one-time cost is approximately $40 million. (CD)

EC Clears TBBPA from RoHS Restriction List

BRUSSELS – The European Commission published the final report on the study to support the review of the list of restricted substances and to assess a new exemption request under RoHS 2 on Feb. 11. The report includes assessment of seven substances, including Tetrabromobisphenol A (TBBPA), for possible restriction.

BSEF, the International Bromine Council, notes the recommendation of "no restriction" on reactive uses of TBBPA (for example, in printed circuit boards), which reflects the low risk of this application in terms of exposure and end-of-life treatment under controlled conditions.

"The study authors did not follow their updated methodology, which states publicly available data should be used for a substance when it's available," said Kevin Bradley, Ph.D., secretary general of BSEF. "We believe available data in the TBBPA REACH dossier leads to a different conclusion: no significant risk under current use conditions."

The report recognizes the need to wait for the finalization of the REACH evaluation of TBBPA, due later in 2021. The report also highlights the difficulty in substituting TBBPA in both its reactive and additive applications.

"The report bears out what we have also seen in a recent study on the impact of BFRs on WEEE plastics recycling by consultants SOFIES." The SOFIES report noted the potential for regrettable substitution and impacts on WEEE plastics recycling with other flame retardants.

BSEF welcomed the EC disclaimer. "It is very helpful to have this disclaimer in place given the serious concerns that we and other stakeholders have over the way the Oeko Institut executed the studies," Bradley said. (CD)

US EPA Prohibits PIP (3:1) in Electronics as of Mar. 8

WASHINGTON – As a final rule, the US Environmental Protection Agency is prohibiting the processing and distribution of phenol, isopropylated, phosphate (3:1) (PIP (3:1)) in electronics as of Mar. 8.

There are some exceptions to the prohibition: for example, for new and replacement parts for automotive and aerospace industries. However, there are no electronics

IMI has installed a UCE (Universal) alkaline etching machine.

A new **iNEMI** project reports benchmark new and emerging test and measurement methodologies for 5G/mmWave materials.

L3Harris launched a 3-D printed RF circuit at the International Space Station, built with a **Nano Dimension** printer.

Lumentum raised its offer for **Coherent** to $6.9 billion, part of a three-way takeover battle for the laser firm.

Molex has received a US patent for a grid array connector system. The novel connector has conductors from cables directly terminated to a PCB.

MTS Systems announced that, based on the preliminary voting results, its shareholders have approved adoption of the previously announced merger agreement with **Amphenol.**

Rogers announced the release of its 2021 ESG Report, which details the company's environmental, social and governance (ESG) strategies and commitments.

Royal Circuit Solutions installed more than $2 million worth of new printed circuit manufacturing equipment and expanded its PCB plant.

Ventec's facility in Kirchheimbolanden, Germany, is now certified according to AS9100D (DIN EN 9100).

Zero Defects International and **Skyla** announced strategic plans to offer PCB frontend CAM services throughout continental Europe and the United Kingdom.

CA People

ACL Staticide named **Daniel Kaiser** to direct sales and marketing. He replaces **Tony Banks,** who retired after 33 years with the company.

Advanced Precision Distribution named **Tom Seratti** president. He has more than 40 years of experience in executive and sales management positions at ITC Electronics, Zack Electronics, Marshall Industries, Avnet, SPI Westek and OK Industries.

AIM Solder appointed **Frederik Rostami** Automotive business manager.

Balver-Zinn managing director **Gregor Jost** passed away.

IPC presented three volunteers with Dieter Bergman IPC Fellowship awards: **Michael Ford, Jan Pedersen** and **Peter Tranitz.**

industry exceptions, says IPC.

The EPA's final risk management rules to reduce exposure to five persistent bioaccumulative and toxic chemicals (PBTs) went into effect Feb. 5.

PIP (3:1) is used as a plasticizer; a flame retardant; an anti-wear additive; or an anti-compressibility additive in hydraulic fluid, lubricating oils, lubricants and greases, various industrial coatings, and in adhesives and sealants, says IPC. PIP (3:1) is also used in plastic-containing materials that are used to form tubes, harnesses, cables, sleeves, gaskets, and covers of parts – parts used in electrical or electronic products.

IPC seeks member input on the EPA final rule, requesting information on how the final rule may adversely affect supply chains for electronics manufacturers. To provide input, contact Kelly Scanlon, EHS policy and research director, at kellyscanlon@ipc.org. (CD)

East West Goes North, Nabs Varitron

ATLANTA – East West Manufacturing announced on Mar. 10 it has acquired Varitron, an electronics manufacturing services provider based in Montreal. Financial terms were not disclosed.

Varitron was founded in 1991 and operates four facilities in the Montreal area. After the deal closes, Varitron will maintain its Montreal leadership team.

The deal was financed by Heritage Growth Partners.

"We are excited to partner with Varitron to expand our integrated design, manufacturing and distribution services into Canada," said Scott Ellyson, co-founder and CEO, East West. "Varitron has an extraordinary reputation for putting customers first and has an established presence for innovation in a variety of high-growth sectors such as medical, industrial, telecommunications and defense. Varitron allows us to offer our customers even greater nearshore, higher-mix, lower-volume, quickturn electronic manufacturing services. With the addition of Varitron's rapid prototyping and strong R&D capabilities, and our collective design, manufacturing and supply chain capabilities, we can support customers from product inception to full-scale production on a global basis."

Varitron has annual revenues in the range of $100 to $125 million, CIRCUITS ASSEMBLY estimates, putting the combined entity at around $250 million. (MB)

ITAC Software Acquires Cogiscan

MONTABAUR, GERMANY – iTAC Software will acquire 100% of the shares of Cogiscan for an undisclosed sum, the company announced in mid-February. Cogiscan, founded in Bromont, Quebec in 1999, provides factory automation software for the electronics manufacturing industry. It will continue to operate independently after closing.

iTAC, a subsidiary of the Dürr Group, cited Cogiscan's expertise in Industry 4.0 as an impetus for the deal.

"Digitalization is one of the Dürr Group's core competences and offers great potential for growth. With the acquisition of Cogiscan, we will be adding a strong team of experts and key technologies to the digital factory, which is a cross-divisional virtual organization for joint development of digital products," said Peter Bollinger, CEO, iTAC.

Cogiscan has more than 450 customer sites across 50 countries. The two companies have been collaborators for more than 10 years, with Cogiscan supplying machine data to iTAC's MES for corporate customers. (MB)

OEP Takes 30% Stake in Cicor

BRONSCHHOFEN, SWITZERLAND – One Equity Partners has purchased HEB Swiss Investment's shares in EMS firm Cicor Technologies for an undisclosed sum. The closing of the transaction is subject to customary regulatory approvals.

HEB Swiss Investment had been a major shareholder of Cicor Group since March 2009 and held approximately 29.35% of the shares as of Dec. 31.

OEP is a middle market private equity firm with more than $8 billion in assets.

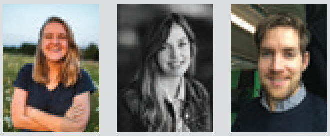
The company also owns Spartronics and Primus Technologies. (CD)

Virtex Acquires EMS Firm Altron

AUSTIN, TX – Virtex continued its growth by acquisitions in March with the purchase of Anoka, MN-based Altron Inc. Financial terms were not disclosed.

Altron, not to be confused with company of the same name once located in Wilmington, MA, has a single facility outside Minneapolis, where it focuses on regional defense and medical customers. It was founded more than 45 years ago and specializes in high-mix, low-volume production.

In a press release, Brad Heath, CEO, Virtex, said, "Altron extends Virtex's geographic reach further into the Midwest medical, aerospace and defense corridor, enhancing our relationships with key customers we service in other regions. Altron also brings expanded expertise in medical device manufacturing to Virtex." (MB)



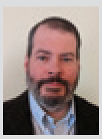
CalcuQuote promoted **Alex Pinell** (left) to account manager, focusing on clients in eastern North America. She joined CalcuQuote in April 2020. Also named account manager is **Marisol Cajigal** (center) in Madrid, who will concentrate on Europe, and **Jordan Lawrence,** who will focus on central and western North America.

iNEMI appointed **Dr. Shekhar Chandrashekhar** chief executive. He was most recently operations manager of Smart Manufacturing Innovation Centers (SMICs) for the Clean Energy & Smart Manufacturing Innovation Institute (CESMII). He began his career as a member of technical staff at AT&T Bell Labs and held several management positions with Bell Labs/Lucent Technologies/Alcatel-Lucent, where his responsibilities spanned supply chain and network solutions. Shekhar holds a doctorate in mechanical engineering from Concordia University.

Kurtz Ersa added **Andrew Hoggard** to its field service engineering team in support of the US and Canada.

Yusaku Kono and **Jon Vermillion** were presented with IPC President's Awards. Kono serves on the Connected Factory Initiative Subcommittee, the J-STD-001 and IPC-A-610 Automotive Addendum Task Group, the High Voltage Cable Task Group, and the WHMA A-610 training committee. Vermillion co-chairs the IPC-J-STD-001 committee and IPC-J-STD-001 training committee.

TTI named **Mike Morton** chief executive.



Yamaha Motor appointed **Michael Helin** to senior automation engineer of Robot Operations FA.

CA Briefs

A broad coalition of 17 tech, medical, auto, and other business groups urged President Biden to work with Congress to fully fund domestic semiconductor manufacturing and research provisions established in the recently enacted National Defense Authorization Act (NDAA). The letter also calls on leaders in Washington to enact an investment tax credit to help build and modernize more semiconductor manufacturing facilities in the US.

ACC Electronix purchased a **Nordson Dage** Assure component counter and a laser marking machine.

Chem3 named **Phoenix United Associates** exclusive representative of its ElectroJet digital printers.

China pledged to boost spending to drive research into cutting-edge semiconductors and AI in its latest five-year targets, laying out a technological blueprint to vie for global influence with the US.

Cogiscan named **Danutek** to handle sales in Eastern Europe.

Dixon Technologies is looking for land in the Kolar, Bengaluru Rural and Ramanagara districts to set up an electronics manufacturing unit.

Eastek is opening a manufacturing facility in Fresnillo, Zacatecas, Mexico.

EMD Performance Materials announced an expanded focus on the US electronics business and a new name in the US: **EMD Electronics.**

Foxconn and **Fisker** will develop an electric vehicle, part of the manufacturer's efforts to boost its automotive capabilities.

IPC unveiled an ESG for Electronics Initiative to develop guidance for electronics manufacturers on an industry-specific approach to ESG (environmental, social and governance) practices and reporting and to develop aspirational goals that the industry is working to achieve.

Hentec named **BTU** exclusive distributor for products in Asia.

The Indian government has started inviting applications for the second round of large-scale electronics manufacturing under the production-linked incentive scheme, with focus on electronic components like motherboards and semiconductor devices.

Electronic components supplier **Infinite Electronics** has been acquired by **Warburg Pincus.**

Jaltek purchased a **Takaya** APT-1400F flying probe tester.

Kolb Cleaning named **Quiptech** distributor in Mexico.

Micropac is eyeing a larger facility and a possible HQ move in Garland, TX.

Mycronic will offer **Aegis Software's** FactoryLogix software solution with its K-Series 3D AOI equipment.

NEOTech partnered with **Numerica** to provide new 3D radar for C-UAS and short-range defense missions.

Next Generation Manufacturing Canada (NGen), a Canadian NGO, is investing $4.9 million into a business consortium led by aerospace technology company **MDA** to apply advanced manufacturing technologies such as robotics in electronics assembly.

Oppo has begun test production at its new smartphone assembly plant in Istanbul, which is currently under construction, according to reports.

Pegatron has leased a 420,000 sq. ft. industrial facility in Chennai, according to reports.

Pro-Active Engineering added two **Mycronic** DX100 high-speed pick-and-place machines, with an expected capacity increase up to 40%.

PVA has expanded its service footprint in Mexico to include direct support in Monterrey, Chihuahua, Queretaro, and three field service engineers in Guadalajara.

Thermaltronics appointed **Horizon Supply Group** distributor.

TopLine has been granted US patent D908648 for a novel design for an adjustable fixture for aligning column grid array substrates.

UTEP researchers have developed a new low-cost Aerosol Jet Printing (AJP) system that's capable of fabricating hybrid electronic devices.

Valuetronics' new EMS factory in Vietnam will be fully operational in the third quarter.

Xiaomi will open two new mobile manufacturing plants and a television plant in India.

STOCKED UP

Trends in the US electronics equipment market (shipments only)	% CHANGE NOV.	DEC.	JAN.	YTD%
Computers and electronics products	-1.5	0.8	1.0	9.2
Computers	-0.5	-2.4	5.3	4.5
Storage devices	-1.8	1.4	20.4	30.7
Other peripheral equipment	3.1	-3.8	12.6	26.9
Nondefense communications equipment	-7.4	2.8	-5.3	15.3
Defense communications equipment	8.7	-11.3	3.7	8.4
A/V equipment	-3.8	-12.9	16.7	24.0
Components[1]	0.7	-0.5	1.3	8.1
Nondefense search and navigation equipment	-1.2	-1.0	2.4	-1.4
Defense search and navigation equipment	-2.2	0.9	4.8	6.7
Medical, measurement and control	-0.5	1.5	1.7	10.4

[r]Revised. *Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: U.S. Department of Commerce Census Bureau, Mar. 4, 2021

METALS INDEX

US MANUFACTURING INDICES

	OCT.	NOV.	DEC.	JAN.	FEB.
PMI	59.3	57.5	60.5	58.7	60.8
New orders	67.9	65.1	67.5	61.1	64.8
Production	63.0	60.8	64.7	60.7	63.2
Inventories	51.9	51.2	51.0	50.8	49.7
Customer inventories	36.7	36.3	37.9	33.1	32.5
Backlogs	55.7	56.9	59.1	59.7	64.0

Source: Institute for Supply Managemen, Mar. 1, 2021

KEY COMPONENTS

	SEP.	OCT.	NOV.	DEC.	JAN.
Semiconductor equipment billings[1]	40%	27.3%	23.1%	7.6%[r]	29.9%[r]
Semiconductors[2]	5.79%	5.86%	8.4%	9.55%[r]	13.2%[r]
PCBs[3] (North America)	0.93	0.97	1.05	1.10	1.14
Computers/electronic products[4]	5.15	5.01	5.13	5.11[r]	5.06[p]

Sources: [1]SEMI, [2]SIA (3-month moving average growth), [3]IPC, [4]Census Bureau, [p]preliminary, [r]revised

Hot Takes

- Total **North American electronics manufacturing shipments** rose 9.7% in January from a year ago. Sequentially, shipments fell 6.4%. (IPC)
- **Employment in US engineering occupations** is projected to grow 3% from 2019 to 2029, about as fast as the average for all occupations, with about 74,800 new jobs projected to be added. (Bureau of Labor Statistics)
- **Global smartphone sales** to end-users declined 5.4% in the fourth quarter, while smartphone sales declined 12.5% in 2020. (Gartner)
- **The EMS sector** recorded 26 transactions in 2020, down from 29 in 2019. (Lincoln International)
- The 2020 output of the **cross-strait Taiwanese PCB** industry increased 5% year-over-year to NT$696 billion (US$25 billion). (TPCA)
- **Some 199 separate legal entities** of 151 different EMS companies in Europe had total revenues of €8.2 billion (US$9.9 billion) in 2020, down 5.4%. (in4ma)
- **Worldwide government IT spending** is forecast to total $483 billion in 2021, an increase of 5% from 2020. (Gartner)
- **PC shipment volumes** grew 12.9% in 2020. (IDC)
- **Smartphone shipments** are forecast to grow 14% year-over-year in the first quarter and 5.5% for the full year 2021. (IDC)
- **Automotive electronics** sales are predicted to hit $641 billion by 2030, a CAGR of 7.6%. (Precedence Research)
- **MOSFET chip prices** are set to rise significantly in the months ahead thanks to worsening shortages arising from persistently tight 8-inch foundry capacity. (DigiTimes)
- **Worldwide server shipments** declined 3% year-over-year to nearly 3.3 million units in the fourth quarter. (IDC)
- **Global DRAM revenue** reached $17.7 billion in the fourth quarter, a 1.1% increase from the previous year. (TrendForce)
- **IC Insights** raised its 2021 IC market growth outlook 700 basis points to 19%.

Where Does Plug-and-Play Fit into Industry 4.0?

Communications interfaces rely on handshakes, but software and simplicity no longer go hand-in-hand.

"PLUG-AND-PLAY" seems a simple, efficient concept, a beautiful merger of elegant design and high technology. What happened to it?

I forget exactly when I first heard the term plug-and-play, but it was sometime back in the late 1980s. As I recall, consumer electronics had something to do with it – perhaps a VCR player that connected to a TV. Or possibly it was tied to early personal computers, where the various accessories could be mixed and matched, so any brand of monitor, printer or keyboard could be added interchangeably to the system. Wherever the phrase came from, the meaning was universal: You could replace one part of a system with a new or different component, and the system would operate without a hitch.

In business the term seemed to morph in two directions. In administrative office environments, the term was associated with updates or upgrades to software. Transitioning spreadsheet software such as Lotus 1-2-3 to, say, Quattro Pro was seamless, thanks to the elegant design of similar operating commands. Just upload the new software onto your computer and begin using it. Meanwhile, on the manufacturing floor, a new piece of capital equipment could be dropped into the process flow and hooked up, and it fit seamlessly with the existing machines. *Voila!* New replaced old. Simple, easy, painless.

Regrettably, over time what was once plug-and-play has become complicated. Too often, when a "new and improved" version is introduced, the product interface also changes, not necessarily to improve the connection, but most certainly to appear new. As software and sensors replace traditional electromechanical options on newer, advanced manufacturing equipment, so too have most time-tested, mundane types of process equipment taken on entirely new looks.

Over the past decade, I have invested in a variety of capital equipment. Some is new technology, which understandably brings a steep learning curve as operators learn from scratch how it works, how it relates to processes up- and downstream, and all the collateral ways other processes may require rethinking and tweaking to best deliver the results the new process promises. I have also invested a significant amount in traditional processes, run on venerable equipment whose design has not changed for decades. When you duplicate or replace such equipment, most assuredly you think it will be a simple plug-and-play exchange or addition. Then reality sets in. The new and improved piece of equipment does not look or operate the same, and requires a total reeducation by all involved just to build product no different or better than has been produced for years. That's when I ask myself, "What happened to the simplicity of plug-and-play?"

If Industry 4.0 is the totally connected office and shop floor of the future, where sensors, computer power and feedback loops enable data to ensure quality flow, and if the traditional plug-and-play order (also known as Industry 3.0) is a shop floor of equipment performing binary tasks and equipment and processes operating virtually independently from each other, we may be living in an industrial *Twilight Zone!*

The sensors and interactive computing power required to enable equipment made by a variety of different companies performing different tasks to accomplish varying final results require elegant, high technology design to have the ability to communicate simply, flawlessly and continuously. And that is where *The Twilight Zone* comes in.

Quattro Pro's elegant design mimicked the operating communication commands of Lotus 1-2-3, enabling an easy shift between the software packages. The issue of intellectual property arose, however, with Lotus suing Quattro over patent infringements. The result: Quattro Pro had to remove that user-friendly, elegant design. Ever since, software companies have worked to differentiate product from competitors, and successfully made their "new and improved" version look totally different from the version it was replacing, to make it harder for competitors to copy, mimic or imitate their proprietary IP. IP protection certainly makes sense, yet it throws a wrench in the idea of achieving Industry 4.0's plug-and-play approach.

For the truly interactive shop floor, all the various manufacturers of capital equipment supplying industry – not just our industry – must be able to interface and interact with each other's equipment. More important, they need to be able to do it over generations of equipment, since the reality of manufacturing is equipment of all ages and origins is used. A new state-of-the-art machine has a better than 50-50 chance of being placed in service next to a 10-year-old model. Software suppliers have their work cut out for them. Not only must the operating system communicate universally, it needs to be upgradable and supported for decades!

Until that time, I fear we are living in industrial surreality, left wishing for plug-and-play simplicity, while struggling to try to best harness equipment to interact, leveraging all the necessary workarounds to make that myriad combination of exotic and mundane equipment that produces cutting-edge product work effectively together. □

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2021: A Year the EMS Industry Needs

It's a drink from an educational firehose, but the lessons will pay off.

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MANY WILL DISAGREE with this column's title this month, especially supply-chain professionals working 24/7 to address a market with varying material constraints, continual logistics challenges and unforecasted demand spikes. That said, over the past few years the electronics manufacturing (EMS) industry has had a changing of the guard. While some replacements are veterans of the last round of market constraints, most haven't seen the perfect storm that 2021 represents. The lessons learned this year will create invaluable experience for this next generation of leadership. Here are a few examples:

Information technology. Over the past decade, even small EMS companies have upgraded their IT capabilities to provide real-time visibility into most of their critical metrics. However, while an exception-based real-time system is wonderful in situations where exceptions happen in relatively low volumes, it creates information overload when it is identifying hundreds of exceptions in a month. The current market challenges are driving management teams to analyze what data they need to prioritize and how that data can be best formatted to help them stay ahead of shortages or capacity constraints. This will broaden the use of time-saving apps and create management teams with a better understanding of systems strategy strengths and weaknesses.

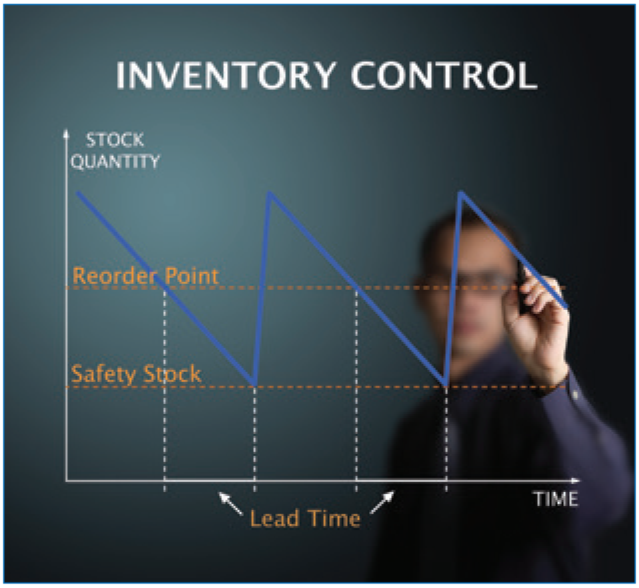

FIGURE 1. Material constraints mean supply-chain professionals must take a more hands-on, collaborative approach.

Supply-chain management. This year will likely teach newer supply-chain professionals a degree's worth of knowledge. Current constraints are driving a much more hands-on, collaborative approach to addressing critical material shortages. Risk management and negotiation lessons are being learned as companies decide how far beyond traditional forecast windows to place orders and work with customers to negotiate better priority for essential products at the manufacturer. There will also be lessons learned in the use of non-franchised sources for scarce material and a better understanding of best practices in vetting these sources and documenting their use with customers.

Program management. Program managers are learning a wealth of lessons in terms of forecasting, capacity planning and working with customers in a materials environment with lengthening lead-times and increasing prices. This year will likely improve negotiation skills and risk management. And just as the telecom bubble in the '90s taught a generation of program managers to carefully document customer commitments on continually increasing upside orders, I suspect this pent-up demand bubble may also teach a few lessons when it eventually bursts.

Inventory management. The current market dynamics make it easy to segue from a Lean "pull" system mentality back to the old "push" mentality on the production floor. If customer orders are increasing astronomically week over week, doesn't it make sense to build out the products with available material and production capacity earlier than scheduled so capacity will be available for next week's surprise upside demand? The answer is likely "yes" in an environment with continuing upside demand increases, assuming material can also be pulled in. A key lesson will be judging when demand is tapering and adjusting finished goods inventory accordingly.

Logistics. Transportation has been a wild card through most of the pandemic and will likely get worse before it gets better. A lot of air freight is transported on passenger planes, yet the number of flights has been reduced as discretionary travel slackened. Shipping and truck freight are over capacity. Cross-border shipments may be delayed by changing Covid-19 conditions that trigger changes in restrictions. In short, what used to be the simplest part of the manufacturing realization process now requires much greater coordination. That in turn is teaching multiple levels of EMS organizations about logistics options.

Continuity planning. Changing Covid-19 restrictions, particularly outside the US, are continuing to impact EMS facility operational status during a time when many facilities are at or near capacity. This is an acid test of the ability of impacted companies to transfer work among facilities. Longer term, this creates nimbler operational strategies and realistic planning that can efficiently support *force majeure* or disaster recovery activities.

Sales training. The most effective EMS salespeople are those who understand how their company addresses common challenges. This year will give every EMS sales team a full library of challenges and solutions stories, and likely a better understanding of key systems and processes associated with those solutions. At the same time, it will also open the door to more candid conversations with prospective customers. In a stable market, OEM sourcing teams often are reluctant to share information. In the current market, these same teams will spend more time in conversations evaluating prospective EMS suppliers' systems and processes for dealing with material constraints and upside demand. This will enable salespeople to build stronger initial relationships.

Customer expectations. The same changing of the guard found in EMS is taking place at OEMs. Challenges seen this year will teach the next generation of sourcing managers what their EMS providers can and cannot control. If there is a benefit to the pandemic, it is shared challenges have built more collaborative relationships among many OEMs and EMS providers. OEMs will be well-served by a generation of sourcing managers who understand the benefits of that level of collaboration and the value EMS providers bring to this type of challenge-rich environment.

In a nutshell, as operationally difficult as 2021 is shaping up to be, the lessons conveyed this year will likely create a cadre of seasoned manufacturing professionals that will benefit the EMS industry and its customers for years to come. □

The Art of Stifling Interference on a Printed Circuit Board Assembly

A printed circuit is an antenna for transmitting and receiving energy.

A RAGING FRATERNITY party with thumping house music can be annoying as the morning hours approach. Noise suppression ordinances to the rescue! The partiers have two choices: quiet down or get shut down.

In that sense, the fraternity party is like building an electronic circuit. If our machines make too much "noise" in any part of the spectrum, it's game over.

Just like kids can stop trampling everyone's lawn and come inside, shut the doors, windows, shutters and even the fireplace flue, we can also contain unwanted spectral emissions. Left unchecked, a printed circuit is an antenna for transmitting and receiving energy from within and outside the board.

Even a well-designed PCB has compromises. Our goal is to be ready to react to spurious emissions that take us beyond the allowable threshold. We start with a power budget, and a noise floor, and our electronics must comply with those design criteria while meeting regulatory requirements.

As we bring different functions aboard, the problems in the near field multiply. We think of high-speed transmission lines as the focus of our EMI abatement efforts. They are seen as the cause of the problem, owing to their signal rise times or a harmonic of that momentary event.

When the root cause is identified, the solution often comes in the form of an additional filter of some kind. Sometimes, that's not enough, and a more extensive re-spin of the board is needed. Just as good fences make good neighbors, so does metallic shielding around various circuits on the PCB.

Coupling: That trace right there is really noisy. Pass it on! If nothing else, a frame around a circuit helps define it as a group. Set off by the shield footprint, the part is already on its way to a happy state of affairs. The shield footprint is typically secured to inner ground planes by a ring of vias along the perimeter. That's all part of the 3-D Faraday cage that suppresses crosstalk within the board itself.

Coupling is a nonlinear thing. The amount of coupling one element will receive from another is a function of the length and width of the gap between the two elements, as well as the magnitude and frequency of the signals. With all that factored in, doubling the gap will square the amount of isolation. That's a bargain, but it works both ways, of course. Cut the gap in half and the coupling is squared. Yikes!

An interactive heatmap to show us the price of rotating an inductor or adding an extra decoupling cap would be nice. Right now, that is an outside function known as SI/PI. Signal integrity/power integrity is the branch of engineering that simulates circuits and saves us from critical mistakes. As the PCB becomes more advanced, SI/PI simulations become much more important.

Coexistence: Making each constituent equally uncomfortable. The only way to get space for something is to take it from something else. This fact of nature is in play for most power distribution networks. We often have just enough copper to meet the overall

FIGURE 1. More participants mean more noise.

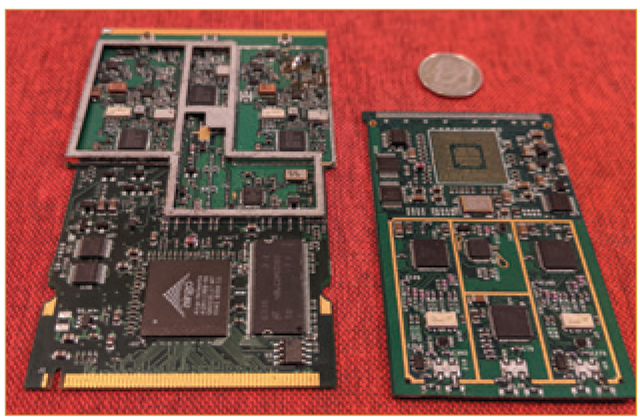

FIGURE 2. Generational shrinkage of a WiFi radio over the product lifecycle. They are much smaller these days.

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power requirements and then only if it is apportioned exactly **(FIGURE 2)**.

Getting the balance right is most important when power is limited. Mobile consumer electronics walk a tightrope of high performance with low power consumption. Inevitably, the battery grows to crowd the electronics together. When it comes to the final form factor, the shields will cover nearly all the components as a substitute for the space they had on the breadboard.

After all circuits are fully integrated and playing nice together, it's time to consider the world of other devices. Bottling up EMI is helped by the metal enclosures, plus an awareness of the noise sources and the circuit elements most affected by noise.

Aggressors: The party animals of the electronics world. We can depend on some circuits to be a house party. One of the characteristics of a noisy circuit element is that they never have a rest state. A crystal will hum along nonstop. A switch mode power supply turns on and off at a certain rate by design. These two players are not usually switching their states all that fast. It's those harmonics that come into play. Clock traces do the same thing and may not need the help from harmonics, but they get it.

The strategy here is to create a jail that keeps the spurious signals bottled up. For crystals, I like to isolate them with a moat in the copper pour that helps contain their emissions **(FIGURE 3)**. Not only is the copper pulled well back, no ground vias are nearby to introduce the crystal to the inner planes.

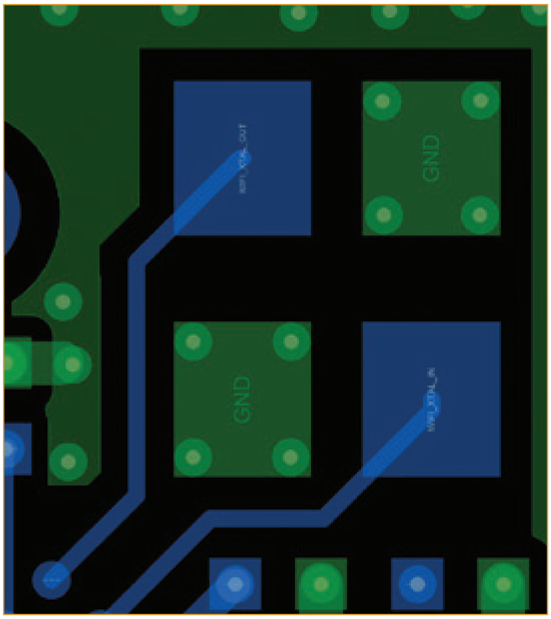


FIGURE 3. Isolating a crystal's ground pins from the surrounding copper pour. (I rotated the circuit along with the route-keep-out after this screen grab.)

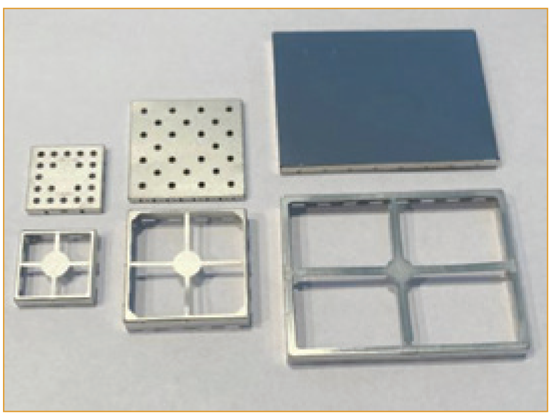


FIGURE 4. Off-the-shelf shielding solutions with pre-cut "mouse holes." The crossmembers stiffen the shield walls and provide a central pickup location for automated assembly. The lids can be perforated for airflow. (Source: Laird)

Layout of a switch mode power supply (SMPS) will feature an inductor on the output pin. The shape that connects the output pin(s) to the inductor is the power supply's megaphone. That connection must be short and only wide enough for full power transfer. Aim for a rectangular placement of each power supply sub-section. Voltage conditioning can go near the main supply, but individual power supplies should be located nearer their respective loads.

The repeated focus on clean power is because a good power distribution network will help cover for some shenanigans on the routing portion of the board. It's just a fact that some chips require a few compromises to get through the fan-out.

Victims: Some circuits are designed to listen, and that's what they do. If you are already fighting EMI/EMC issues, it pays to take a good hard look at the power distribution, as well as the grounding scheme. Sensors and other similar devices are effective at picking up unwanted interference. In their case, the shield isn't so much a jail as it is a penthouse where the listening device of whatever type can do its thing in peace.

Receiver circuits are more susceptible than the transmitter side. The higher magnitude of the TX signal raises the noise floor. Most of the traces on a board can be classified as one or the other, with I/O lines being a little of both. Locate the sensitive receive circuits as far as practical from the noisy inductors and other culprits. An elegant layout has these attributes and provisions to increase isolation, should the need arise.

The most common shielding type is the two-piece type that has walls and a lid that presses on over the walls **(FIGURE 4)**. This allows field service once the shield is installed, while the single-piece shield must be unsoldered from the board for work under the hood. Another way to use a single piece shield is to solder down little clips that hold the shield in place. Is that still a one-piece shield? The companies that make those also make a few standard-size covers to plug and play.

Of course, a two-piece will cost a little more. A four-sided shield with 90° bends keeps costs down. A six-sided L-shape or chamfered edge is not so bad, but costs will rise for polygonal versions. Multiple pockets within a single shield are possible. These are popular with analog circuits where multiple radios are in use.

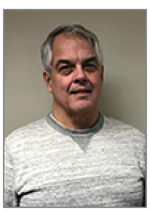
Materials are generally stainless steel, with aluminum or nickel-

continued on pg. 32

DC Analysis: Keeping PDN Running Smoothly (Not So Easy Anymore)

Many new products need tighter hardware.

TERRY JERNBERG is an applications engineer with EMA Design Automation (ema-eda.com), with a focus on PCB design and simulation. He spent his early career on signal integrity simulation for the defense industry and was fundamental in the adoption of these tools at EMC and Bose. A vocal advocate for simulation, his enthusiasm for physical modeling has expanded to include power and thermal capabilities.



TWO COMPELLING FORCES driving much of our technology – miniaturization and performance – are not new. In fact, one could say they have appeared within every product spec and design document in some form or another since the terms were coined. Fundamentally, this has enabled capability and portability with products in virtually every hardware sector. This will (and should) continue. In the area of miniaturization, both board and package are transforming as technologies such as rigid-flex, blind/buried vias, and multi-die packages move from fringe to mainstream. Further, performance improvements maintain the well-known doubling trajectory and are propelled forward by orders of magnitude in speed, while increasing efficiency and extending battery life. Often these gains are continually achievable only by reducing the voltage swing to under a volt. As miniaturization and performance drive devices to new functionalities and applications, the effects of these requirements are visible throughout the design process. Nowhere is this drive for smaller, faster, cheaper more noticeable than in power.

Power demands outpacing supply. To comprehend the extent of the power delivery network (PDN) transformation, consider the following. Design requirements associated with power delivery have become substantially more complex, with many ICs requiring power to be supplied at multiple voltage levels. Frequently those levels are near or below a single volt, contracting virtually every threshold and reducing margins to mere millivolts. Simultaneously, demand for current has skyrocketed in some product areas, made obvious by the extent to which we now account for adequate cooling. In addition to these increased electrical demands, the PDN must also be more responsive, capable of supplying the instantaneous current demands of high-speed signaling. While all this may suggest a more robust PDN is needed, as many new products reach manufacturing, often the opposite is true. Not surprisingly, the miniaturization effort has had a consolidating effect on the physical hardware, frequently bringing high-current ICs closer together **(FIGURE 1)**. Advances in device packaging have contributed as well. Pin counts can easily exceed a thousand on a single package, and mainstream spacing under a millimeter contributes to the same reality: The PDN is comprised of less copper in today's PCB than it was just a few years ago.

Controlling the PDN from the start. Recognizing this is a trajectory where power delivery *will* become problematic, and conceding that for some designs it already has, progressive product development teams are looking to power integrity simulation for answers. We'll see in subsequent columns several elaborate interactions attributable to the power system, such as complications with "the return path" and the ability to shield and control EMI, but first we need to ensure adequate capacity and effective distribution. Commonly referred to as the "DC" branch of power integrity, its primary task is to guarantee sufficient current sources at a steady voltage. The PDN must provide a conductive path such that current leaving the supply does not experience so much resistive loss the voltage can't be maintained when the device is drawing its maximum current. It is essentially an Ohm's law problem. By understanding a device's operating voltage and maximum current draw are defined by its specification, we quickly see PDN resistance is the only design element in which a product team has any control. Signal integrity has taught us the physics associated with current flow and electrical conduction are very predictable. We recall that with knowledge of the materials and conductor geometry, accurate/predictive characterization of electrical behavior can be determined. Mathematically, power integrity, aka PI or PDN simulation, has many similarities with its signal integrity roots. What is strikingly different, however, is the actual copper under examination and the current being conducted. Contrast the wide copper-flooded areas (to include entire planes) associated with power routing with the thin line of a signal trace, and we'd naturally expect the resistance to current flow would be much different. Likewise, consider the short bursts of current we see when digital signals switch, first in one direction and then the other, and compare

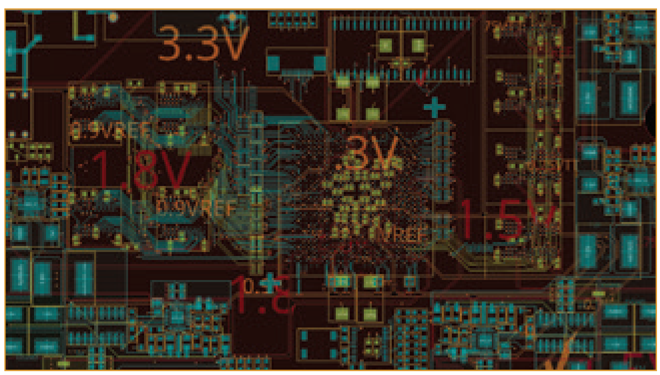


FIGURE 1. Multiple power planes have become the norm.

those to the steady drain, source to load, we see for power signals. Therefore, the physics of conduction are the same, but the signals conducted are very different, requiring different types of analysis and methodologies to meet our power delivery goals and demands **(FIGURE 2)**.

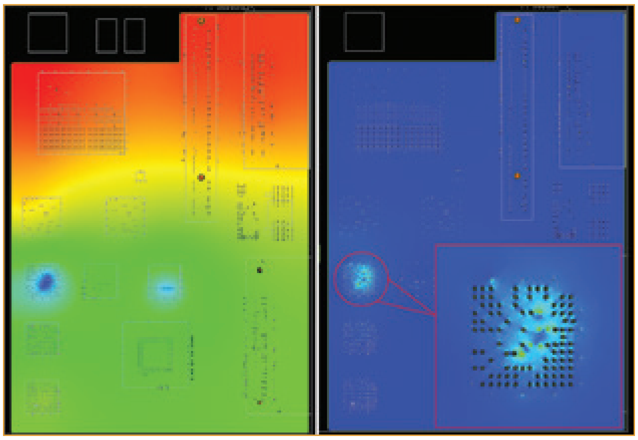


FIGURE 2. IR drop vs. current density.

DC aka distribution and capacity. As noted, our DC goals for power delivery, or PDN, can be broadly defined as distribution and capacity. Distribution implies all devices, even those farthest from the supply, have access to adequate current at the defined voltage. Similarly, under extreme demand, capacity ensures the power system can maintain that voltage, even when current draw reaches its allowable maximum. If the voltage supplied at every device doesn't droop below the acceptable value, we can have great confidence that even if each device needs to draw its most aggressive current, the power delivery network is capable of distributing adequate current to all devices.

Solving for V. The DC capability associated with power integrity simulation requires only two things: an accounting of load and resistance. An accounting of load is simply how many devices are being supplied and how much current each device requires. Cumulatively, this is the "I" in our Ohm's law (V = I x R) reference, while "R" is resistance. We know from previous discussion simulators routinely calculate resistance, even impedance ("complex resistance"), given only the materials and geometry contained in their CAD databases; this is exactly the case with power integrity. Often accessible directly from within the PCB CAD tools, PI simulators can readily identify conditions where a chip could become "power starved," but it doesn't stop there. Because the tools create a model of the board, all the properties (voltage, current and resistance) can be displayed as color-coded overlays directly on the board's etch. This enables both visualization of a problem and an environment where corrections can be made in the native CAD tool and be reflected in the design file. While not specifically addressing Power DC issues (one of distribution/capacity), these additional overlays are useful for identifying other concerns associated with power as well. Areas of high current density, which could result in both EMI defects and reliability issues, can be easily detected and prevented, as the simulators produce an intuitive, visual model of the power network.

Moving up a level of abstraction. Power integrity DC simulators exist from a number of vendors and have universally proved accurate. This is largely due to the extensive studies on copper conduction for the RF and high-speed digital industries. While traditionally this type of analysis has been done at the layout and routing phase of the PCB, it is increasingly apparent analysis needs to move up a level of abstraction to incorporate earlier system-level, power budgeting and inspection **(FIGURE 3)**. In this analysis, for example, a DC-to-DC convertor's dual role would be recognized, both as a load to the main supply net and the origin (supply) of the power net produced at its output. Leveraging the PCB model as a Spice model, external circuit elements such as switches, resistors and transistors can be included, permitting simulation of the system itself. Extending system-level checks to include device Spice models extends both the checking and display capability beyond individual nets to the system. This enables "sizing" and capacity checks to encompass device selection and verification, in addition to the checks performed on the etch alone.

PDN pressure is not going away. Although the technologies that will drive product direction in any hardware sector cannot be predicted, it's safe to say there is little desire for bigger, slower, less-efficient anything. Therefore, miniaturization and performance will continue to be prominent, and they have their sights on all that "extra power plane copper."

Will you be ready? □

FIGURE 3. Power design is a hierarchical problem. Source: Sigrity Power Tree.

High-Speed Telecom Requires 'Dialed-In' Materials

Stronger, faster and more robust networks will be one of the positive legacies of the pandemic.

HOPEFULLY, WE WILL soon be able to start living our post-Covid-19 lives. Going forward, some of us want fundamental changes. Others are keen to return to the way things were. Although we will be pleased to put this situation behind us, some things are here to stay. One, obviously, is the lethal group of coronaviruses that will surely continue to take lives after lockdown (we hope at a greatly reduced rate). Another, I believe, is the tendency for many of us to continue working from home (WFH) to a much greater extent than before.

WFH has been one of the headline trends of this crisis. Although clearly not to everyone's taste, it could turn into a revolution founded on the internet technologies that allow us to meet with colleagues online, access data and tools remotely, and benefit from high connection speeds wherever we are – wired or wireless. That so many can do meaningful work this way also reflects the soft nature of many tasks associated with getting things done in developed economies. These soft deliverables liberate us from location and will be critical to our economic survival of this pandemic.

Many are keen to recover the social dimension to our working lives. While physically working together in the same space and time to achieve shared goals is a powerful part of team building and cohesion, we can also take advantage of the flexibility to ease some of the more stressful aspects, such as traveling and being away from loved ones.

WFH has also powered a rise in IT equipment sales as lockdown periods have been enforced across the world. Internet use has surged 30% in the past months, challenging the networks to support this explosion of connectivity. In addition, service providers and end-users are more aware of security vulnerabilities and the importance of protecting people and assets against cyberattacks. As if securing connected devices within a restricted campus is not difficult enough, widespread WFH significantly extends the attack surface available to hackers.

Among the techniques put forward to protect and manage telecom networks, AI is perhaps one of the most powerful and exciting. The ability to predict the usual and identify the unusual in its midst is the key to AI's power in these roles. By anticipating usage patterns, AI can help network operators provision resources optimally to ensure resilience and maintain uptime. At the same time, the technology has become sophisticated enough to distinguish the many small aberrations that characterize human behavior from the more seriously unusual events likely associated with fraudulent activity and cybercrime.

Underlying everything, of course, are demands for greater speed and capacity driven by the uptick in reliance on the internet for work and social connections. This involves committing to rolling out the new generations of high-performance hardware needed to handle the extra subscribers, extra traffic density, and extra speeds. In the last telecom boom, just before the 2001 dotcom bust, I worked with leading hardware vendors involved in building incredibly large multilayer telecom switch backplanes, up to 60" x 48", with as many as 40 layers. Getting these boards to operate at the speeds required, while also achieving the thermal performance needed to ensure reliability, proved extremely challenging.

While the physics of the situation have not changed in the intervening years, the materials at our disposal have. So, too, has our understanding of the interdependencies among parameters like signal speed, trace dimensions, energy loss, and dielectric properties. Getting the best tradeoff is critical to meet the world's connectivity needs going forward.

Skin effect is the greatest limiting factor in data transmission through PCB traces and depends on trace dimensions, particularly trace width. As signal frequency increases, the region at the edges of the trace where current, and therefore data, flows becomes thinner. Widening the trace can combat the restriction: the wider the trace, the more "skin" for current to flow, and hence more data can be transmitted. More skin from wider traces also helps reduce skew and lower trace resistance, which, in turn, lowers the system power requirement.

PCB geometry places a burden on layer usage that could be relieved if more layers are added in the same or smaller physical structure. However, as dictated by the dielectric constant (Dk) of the material, thinner spacing between layers requires smaller, narrower traces as the trace gets closer to the reference plane. This clashes with the drive to increase trace widths for increased data speeds and lower power. Smaller or narrower traces also increase pressure on PCB manufacturing processes. Larger traces are easier to manufacture – at every stage of the process, from imaging to etching – and permit better yields.

We have pointed out dissipation factor (Df) and Dk are important parameters to consider when choosing a dielectric material for high-performance, mul-

continued on pg. 29

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Messages from the Chairmen

The chairman and chairman emeritus describe the past and future.

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IN THIS MONTH'S column, the chairman and chairman emeritus for the PCEA give their viewpoints on the importance of organizing. And as always, I'll provide a list of events coming up.

PCEA Updates

This month I am excited to bring to our readers an inspiring message from not one but two of the PCEA's chairmen.

Many readers may not know that our PCEA board has two chairmen by design. Our idea from the beginning has been to preserve the experience from our past organizational associations and use it as our compass as we move ahead.

Steph Chavez serves as PCEA's chairman. Steph's primary interest is to lead this organization into a future that respects the ideas and efforts – the legacy – of those who have served the electronics industry so well in the past. To fulfill that interest, Steph relies on his counterpart, chairman emeritus Gary Ferrari, for his wisdom and experience. Gary's compass was magnetized by a career of serving the electronics industry and bringing together and leading electronics industry professionals.

This month, then, please trek along with us and enjoy this special "messages from the chairmen" interview as transcribed and lightly edited from our Zoom interview.

Message from the Chairman

An interview with PCEA chairman Stephen Chavez, MIT, CID+ and PCEA chairman emeritus Gary Ferrari, MIT, CID+.

Kelly Dack: Thank you for joining us, gentlemen! With me are Steph Chavez and Gary Ferrari, chairmen of the PCEA. Let me explain what I mean by chairmen. Steph Chavez is the officiating chairman of the PCEA. We also have Gary Ferrari, who serves as chairman emeritus for the PCEA. I'd like to start by asking Gary for some perspective on the past, and it's important that PCB designers are connected in some way by an organization.

Gary Ferrari: Well, way back in 1991, Dieter Bergman and I started the Designers Council. The main reason for starting was to respond to feedback from designers. PCB designers had expressed that engineers have IEEE and other organizations to participate in. They mentioned all they had were sore eyes from staring at their computer screens working all day long. (Laughs) They wanted to be represented. They wanted to have opportunities to learn from each other and to learn from the industry. That was the main thing. They inferred, "Everyone else has different kinds of credentials; we don't have any official credentials at all." That is when we started the exams and certification programs. The CID and CID+ were created "by designers, for designers." We had this as our mantra and even a logo. At one time we had t-shirts and other different schwag, all kinds of stuff. It grew rapidly.

Dack: So, Steph, why is it important designers connect with the other stakeholders? Gary mentioned some of the other stakeholders. What's your take on why it's so important, especially nowadays?

Stephen Chavez: When I think about our profession in the industry, to evolve, we collaborate. We have to get knowledge, because design is more than just someone sitting in a cube or behind a computer by themselves. It's a collaboration among engineering, fabrication and assembly – all the professions. And when we think of design as a team concept, we truly must have all the stakeholders involved. With stakeholder collaboration, cross-pollination of the designer, manufacturer, test, engineering ideas meld together to become the holistic makeup of the new hybrid designer. As designers collaborate, not just within their own company ecosystem but outward in the industry, PCEA is striving to add synergy within this collaboration. We want to help printed circuit engineering professionals take it to the next level with all the different industry associations. I think that's the next evolution that we are seeing now.

Dack: Can you share examples of how the PCEA membership is doing that collaboration? How are they feeding off and supporting one another?

Chavez: I have a lot to say, but since Gary is the emeritus, I'll be polite, and I'll let him speak first. (laughs)

Ferrari: One of the biggest items I see, which we didn't have in the past, is that the chapters are now actually working together. They're sharing. They are meeting together. One chapter is on one side of the country, and another is on the other side of the country. They are spreading out beyond the chapter itself with their own programs. I think this is outstanding because I remember years ago, some of the chapters in the Designers Council felt isolated and lost enthusiasm. It was the same guys all the time, the same people and no fresh ideas. However, Steph took a different approach. I'll let Steph describe it because it's beautiful.

Chavez: With the pandemic, the silver lining is the ability of collaborating virtually, no matter where you are in the world. So, while our physical footprints are smaller, our virtual footprints are much larger. We can effectively collaborate across our platform. Our PCEA chapters are doing this, and we see the chapters are growing astronomically. Our multi-chapter events had never happened before Zoom. We didn't have the chapters sharing like, "Hey, what did you do that was successful? Let's take some of that and do that here in my region or in my state." And even in areas that don't have a local chapter, they can still affiliate and gain that perspective and knowledge by being part of the overall PCEA collective. That's what we see as a huge benefit, and it is spreading like wildfire!

Dack: I don't want to pass up the opportunity to ask your perspectives on Gary's role as emeritus chairman. Steph, can you explain?

Chavez: Sure. Gary and Dieter Bergman were the founders – the visionaries – for the PCB Designers Council. They were instrumental in charting the educational and certification programs for PCB designers. Gary is an IPC Hall of Famer and has championed so much of what the trade organizations stand for throughout his career. He has been involved in IPC subcommittees and has chaired the IPC Designers Council executive board. I strongly feel we should always remember our roots to keep us grounded but move forward. Gary's role within the PCEA is as an honorary chairman because we value his input and his decades of lifelong lessons to guide us. We feel a strong urge to embrace the past while we can. We want to carry those values and experience with us as we move into the future.

Dack: Well said, Steph. Very good! Gary, do you have anything to add to that?

Ferrari: Yeah, just one item. Everything he said is 100% correct. The main difference I'm seeing is that the chapters we had, as Steph mentioned, they were separated. And the only time they had an opportunity to share anything was twice a year at the regular meetings. And never did all the chapters show up. But here and now they are sharing, even with relatively short notice. The movement is just growing astronomically. I'm so proud of the team we have, including you, Kelly! When we started out originally, we didn't have a large group. We had only a few people who worked with us. But the large groups of people were in the chapters themselves. We now have a vastly more diverse and beautiful organization. I have to give kudos to Stephen and the whole team for that.

Chavez: Let me add one more thing. Gary is truly at the essence of really taking it forward and making a difference. Let's call it what it is: Gary is our *esprit de corps!* He refuels us as we look at what he has done and how he continues in the second half of his career. His example gives us that extra bounce in our step moving forward.

Dack: Very good, right on! We're going to move forward now. I'd like to open it up to either of you for some visionary comments. It's been just a little over a year since PCEA has hit the ground running. Can you rehash what has been done over the past year? Can you give us a little info on what we're doing now? And then please, tell us where we're going. We need to talk about the future. It's open mic ... go!

Ferrari: One of the main items I think has taken a tremendous amount of work over the past year is our website. We started with no website at all both in PCEA and in our previous organization. Previously, in the 1990s, we came out with "The Route" – a newsletter we used to communicate with our members. Now, in the PCEA, it feels great to be leveraging the power of the internet and social media. We have sponsors and so many ways to reach out that did not exist before.

Chavez: To add to that, another difference from the past is the ability for internet collaboration. We evolve and our media team adapts on the fly. We have activities happening constantly. For example, we had our kickoff meeting last year, our initial grand opening. After that, we've had several follow-on chapter events. We even held an international tri-chapter event attended by an international audience. Because of the pandemic, we have evolved into this virtual world until we get through it. Eventually we'll go back to face-to-face meetings, but that doesn't mean we're going to walk away from virtual. We'll continue to embrace and do both. Chapters have come to life in areas we didn't have chapters before, and it's truly amazing. As far as a footprint, we have the greater Michigan area. We have St. Paul, Minnesota. We have Portland, Oregon, just to name a few. And we have chapters coming up in the Midwest like the Chicago/Wisconsin area; the New England, New Hampshire and Massachusetts area; Albuquerque, New Mexico; and then we have Texas: Houston, Dallas and Austin. Those are all in the early stages of their formation, but it's just amazing how it's taken off. And when we think about the events happening, it's just that things are happening so fast. And we have those growing pains too. When you think about what we have done, we have started a new industry association and are being successful getting it off the ground. It's been a challenge, but it's a worthy challenge, supplying the adrenaline of a startup experience, so to speak.

Dack: What is PCEA looking forward to on the 2021 roadmap?

Chavez: We want the growth we have been experiencing continued with our chapter activities. We also want to spread our chapter growth internationally. We see lots of activity going on there and excitement for engagement. A lot of us are wearing multiple hats right now, so getting more people involved will be a critical part of our evolution. We must make sure to have the right team evolve together. We must share the same vision.

With so much activity and so much eagerness about so many ideas, we must be certain we're doing the right thing in the PCEA that will be best for the industry. This is key, and that's where I see us in our 2021 evolution.

Dack: That's tremendous. Steph, Gary, thank you both for sharing your insights.

Next Month

More positive PCEA announcements are pending, awaiting official release. I hope to focus on these exciting topics in our next column!

Upcoming Events

Below is a list of upcoming events:

- Jun. 7-10, Zuken Innovation World (Scottsdale, AZ)
- Jun. 8-9: Cadence Live (online)
- Jun. 15-17: PCB East (Marlboro, MA)
- Oct. 5-8: PCB West (Santa Clara, CA)
- Nov. 1-4: SMTAI (Minneapolis)
- Nov. 10, 2021: PCB Carolina (Raleigh, NC)

Spread the word. If you have a significant electronics industry event that you would like to announce, please send me the details at kelly.dack.pcea@gmail.com, and we will consider adding it to the list.

Refer to our column and the PCEA website to stay up to date with upcoming industry events. If you have not yet joined the PCEA collective, please visit our website pce-a.org and find out how to become a PCEA member.

Conclusion

Never forget your roots. Carry them forward into the future, but be willing to change, grow and evolve. These are wise and profound messages from the chairmen. See you next month or sooner! ❑

Kiss the Mouse Click Goodbye

After 40 years, it's past time we overhauled our data package processes.

THE CONCEPT OF "smart engineering" has been a major focus of mine these past few years. In the 35 years I have been in the PCB industry, I've come to the conclusion we are stuck in a quagmire of unintelligent, unstructured and, frankly, 40-year-old technology of exchanging design data packages. The impact is repetitive, mindless, non-value-add administrative tasks across all facets of the industry. The problem has only been exacerbated with increased technology. All this negatively impacts labor costs, quality and NPI lead times.

Manual and duplicate data entry are the norm, with thousands of keystrokes and mouse clicks performed throughout the process. From quote to pre-CAM, planning methods and CAM, quality checks are abundant. One mistyped character or digit could potentially result in 100% scrap of the product. I've watched patiently as many industry proposals for intelligent and structured data packages have come and gone. The waiting has been daunting. We have invested millions of dollars on enhanced software applications for CAM, CAD and engineering to streamline and achieve efficiency and productivity. While these investments and initiatives certainly have improved productivity and cycle times, we are still enveloped in an extensive human-dependent, high-labor-cost operation with extravagant administrative tasks. This has and continues to be our reality.

My passion for consistent and results-oriented continuous improvement motivated a rethinking of the current methodology and defines what I call "smart engineering." How can we import these unstructured data packages and transform them logically so we have data-driven and amplified automated processes? In essence, how can we attain cohesiveness between the data and software applications engineers use to interact every day. The objective is semiautonomy by focusing on repetitive process automation (RPA), which is catapulted by intelligent database elements.

Technology and software applications exist today that, if integrated and developed appropriately along with a smart process, will be the catalyst to achieve this objective. Industry software applications can autonomously translate, analyze and prepare virtually all data formats used today. Optical character recognition (OCR) can scan, interpret and extract critical information from a fabrication drawing and export it into an XML file, which in turn autonomously populates quote and engineering applications. Specifications and product attributes can drive the CAM pre-production edits. In this scenario engineers are validating and innovating, versus "doing." Intelligent rules-based software applications perform tasks based on the attributes of the design and related product specifications. Adopting and integrating smart engineering tactics directly impacts the operational performance in which engineering resources are now focused, improving processes and quality that will support business revenue and growth initiatives.

EPIC Front-End Engineering was formed in late 2020, focusing on two fronts. First and foremost, we provide guidance and software development support to PCB frontend engineering with an emphasis on smart engineering. Our primary objectives are helping companies reduce labor costs, improve quality, and enhance productivity and efficiency of engineering resources. Second, we support the industry across all segments, to adopt and integrate intelligent data packages utilizing IPC-2581, which is the catalyst for a giant leap forward for the larger industry.

We are a high-technology industry, building products used in applications that drive the entire world. We are at the cusp of a revolutionary change, as intelligent data package concepts such as IPC-2581 are adopted by large OEMs and CAD software companies. The industry as a whole will reap many benefits. Getting the data package right is the trigger for the I4.0 Smart Factory and, in parallel, smart engineering.

Smart engineering goes beyond a single standard format, of course. In upcoming columns, I will elaborate on smart engineering concepts, with a focus on the benefits and steps we can take today to drive advanced automation within frontend operations.

The future of smart engineering is upon us, and the opportunities are bountiful. Sitting idle is not an option. ❑

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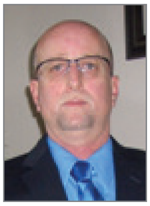

5 Options for Connector-Less Flex Jumpers

Adding solderable fingers to connect rigid boards.

WHEN DESIGNING A flex jumper between two rigid PCBs, where no room exists for connectors, are solderable pins or tabs that extend out of the edge of the flex circuit a possibility? If so, what are the cost and reliability implications?

Quite a few options are available, each with its pros and cons and cost implications. This month, we look at the possibilities.

Sculptured fingers. This construction yields unsupported copper fingers that extend beyond the circuit outline. The fingers are typically ~0.010" thick. These can be made by starting with very heavy copper (usually half hard) and etching down all areas other than the fingers, or starting with thinner copper and plating up only the finger areas to meet the desired overall finger thickness. The fingers can then be formed to best fit the desired applications (**FIGURE 1**). The cons to this construction are cost and handling issues. Adding sculptured fingers to a flex circuit will have a modest cost impact, but the biggest downside is these parts are fragile. The fingers can be easily bent out of shape during shipping or handling on the production floor and are difficult to realign once damage occurs.

Brazed or welded fingers. This construction also yields unsupported fingers that extend beyond the circuit outline. The fingers can be thick copper (I recommend half hard or full hard copper), but more often they are a more durable material such as nickel. While this construction is more robust and tolerant to handle than sculptured construction, the fingers can still be damaged if mishandled. Cost implications vary from vendor to vendor, depending on the level of automation incorporated when the fingers are attached.

IDC contacts. Insulation displacement contacts use special pins with "claws" that pierce the polyimide insulation and contact the base copper (**FIGURE 2**). These contacts are reasonably durable and come in a range of configurations. The downsides are cost and limited minimum pitch between contacts, and only vendors with IDC equipment support such needs.

Unsupported fingers. This construction is typically created by using a laser to ablate the dielectric material covering both sides of a row of parallel copper traces. Unlike sculptured fingers, the finger thickness in this construction will be the same as the rest of the circuit (i.e., very thin). This construction always requires a tie bar on the end of the fingers to help prevent damage. This construction is most often used to connect a flex to a rigid PCB using hot-bar soldering. Unsupported finger circuits are typically only one of two layers, so the additional processing steps associated with the laser ablating and cleaning have minimal cost implications.

Supported fingers. This construction yields the least expensive and most robust final product. The fingers are only exposed on one side, so no pre-punching of the base dielectric or laser skiving operations is necessary (**FIGURE 3**). The base polyimide strengthens the fingers, making them less prone to damage during handling. If adhesiveless base laminate is used, the resulting construction can be hot-bar-soldered through the polyimide base to a matching set of fingers on a rigid PCB. Alternately, anisotropic adhesive can be used to make the connection the same way. Either of these connection methods provides a very low-profile and reliable connection. The downside is it is difficult to inspect the hot-bar-soldered or anisotropic adhesive connections because you would have to look through the polyimide to see the solder or adhesive joint. Some designers will specify the polyimide material *between* the fingers be removed. This isn't free,

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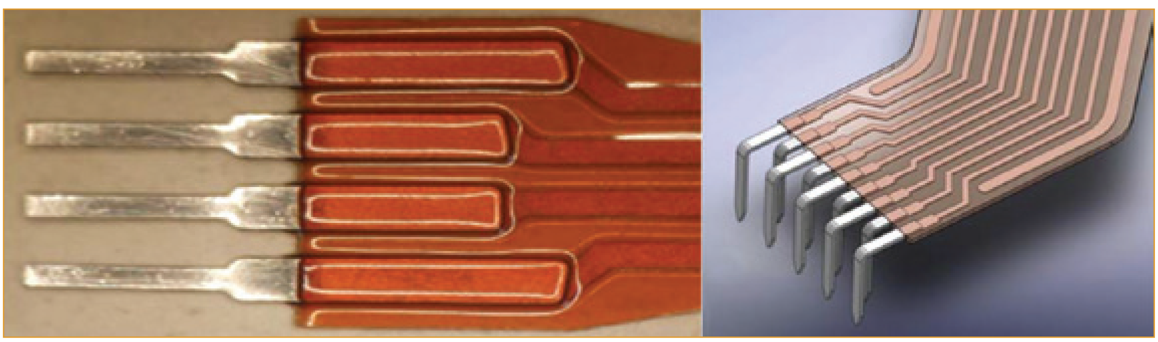

FIGURE 1. Sculptured fingers can be formed to fit the application.

but it adds only modest cost to the finished flex. The base polyimide remains on the back side of the fingers to help strengthen them, but the material between the fingers is removed to permit inspection of solder joints or anisotropic adhesive connections. If anisotropic adhesive is used, and the polyimide between the fingers removed, be sure the hot bar used to join the flex and rigid PCB has a non-stick finish! If not, there is a good chance the exposed adhesive between fingers could stick to the hot bar.

Keep in mind *all* these options will result in a more fragile connection than standard connectors, and I *highly* recommend not using them in dynamic applications. Even when used in static applications, it is advisable to look at ways to ruggedize the connection area to protect it from damage. The most common method is a coat of semi-rigid epoxy over the connection area. A less-expensive option is to add a strip of pressure-sensitive adhesive to the flex adjacent to the connection area. The release liner can be removed just prior to lining up the fingers and can aid in holding the flex in place during hot-bar soldering or laminating processes. □

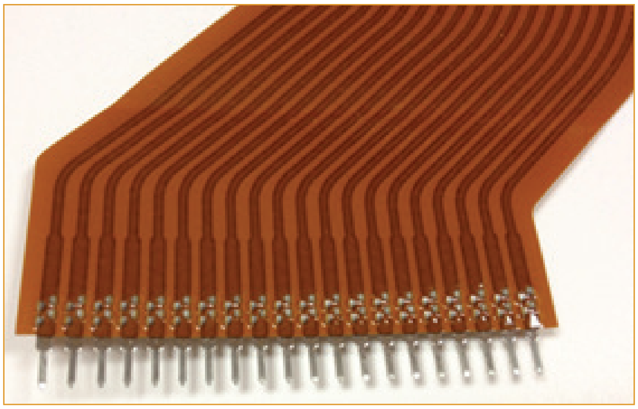

FIGURE 2. IDC contacts pierce through insulation to make contact to copper traces.

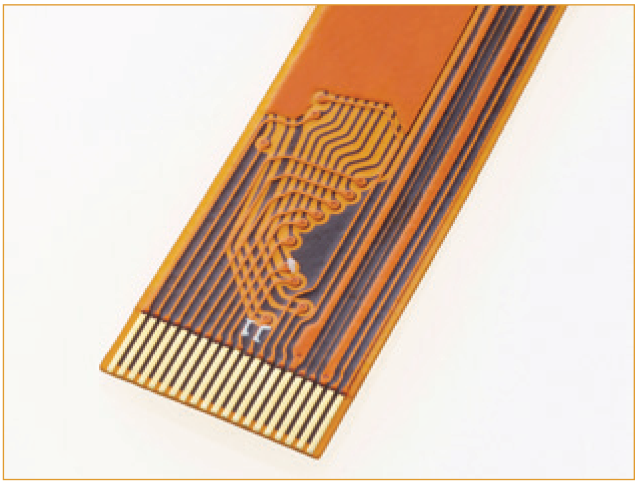

FIGURE 3. Supported fingers are the most robust and cost-effective of the discussed options.

Material Gains, continued from pg. 26

tilayer PCB fabrication. With a lower Dk, the trace width can be wider, thereby increasing its effective data carrying capacity, while at the same time easing manufacture, reducing pressure on end-of-line yield. Historically, however, lowering Df tends to drive up Dk. The latest PTFE materials offer a new tradeoff between these important parameters, permitting low-loss materials with Df in the region of 0.0015 to have Dk about 2.6. These properties offer a much better tradeoff between trace width and layer thickness than previous low-loss materials, enabling large, high-speed multilayer boards that are affordable and reliable.

Currently, we regard the latest PTFE low-loss, low-Dk materials as exotic. With familiarity, they will undoubtedly be standard, especially when the next generation arrives to deliver even greater performance. □

The Future of AI is EMBEDDED

What PCB designers need to know to bring AI hardware to the device level. by **ZACHARIAH PETERSON**

A few buzzwords dominated headlines in 2020, many centered around Covid-19 and politics. Those who follow trends in technology probably noticed one area saw an explosion of growth: artificial intelligence. Unfortunately for the hardware developer, the tech world's interest always seems to be drawn to the software side of AI.

The software industry has quickly embraced AI to the point where many software-driven services incorporate some element of AI to provide a meaningful user experience. As of the first quarter of 2021, it's getting difficult to find a SaaS platform that *doesn't* use AI for some specialized task. SaaS-ification is fine, and it's creating a wealth of productivity tools that businesses can mix and match to make their processes more intelligent. And there are the big players like Facebook, whose AI models run quietly in the background, determining which advertisements and inflammatory memes you're most likely to click.

What about the hardware side? What is its role in the AI ecosystem, and how is AI used in embedded systems? The reality is on-device AI with the same capabilities found in a data center is a long way off, but many companies are working to make these platforms a reality. When you examine many use cases, there is major motivation to move user-facing AI tasks outside the data center and run them directly on the device. What some in the software world don't realize, and where embedded systems designers play a major role, is this requires specialized hardware that is starting to proliferate into the market. Some of these new hardware-driven AI developments are being created by familiar names in the electronics industry, while others are being introduced by startups, research labs, the US government, and some surprising names from the tech sector.

What does this mean for the average PCB designer, and what do they need to know to bring AI hardware to the device level? Although these tasks may appear challenging, PCB designers are instrumental and already have many of the skills needed to implement on-device AI.

On-Device AI Compute Challenges

The goal in bringing AI onto the device is to reduce reliance on the cloud, meaning there would be no requirement for an internet connection to do (at minimum) inference tasks. In fact, not all AI tasks need to be run in the cloud; the compute power in data centers is overkill for many practical inference tasks. To rely less on the cloud, you need to diligently design systems to provide comparable levels of computing power on the device. This is not, however, a simple matter of stacking multiple CPUs/GPUs on a PCB, as was the trend in 2019-20.

AI-driven hardware must overcome multiple "walls" to enable fast, power-efficient AI on the device:

- Memory wall: The problem here is not just memory capacity but also memory speed. Faster read/write access to data in memory reduces total time required for inference and training tasks.
- Heat wall: Anyone who has heard the fan on their CPU or GPU spin up to high speed knows high compute tasks generate a lot of heat. AI is no different, but reducing the number of bit transfers during computation reduces cooling requirements and total system size.
- Size wall: Beyond the heat wall, it's desirable to continue reducing system size by packing more features into smaller spaces. Some existing commercial off-the-shelf (COTS) components are simply too large to enable compact embedded AI products, while also satisfying the other areas on this list.
- Compute wall: Efficient on-device AI requires much greater compute power in smaller packages, which then requires redesigning the fundamental architecture of transistor-based logic circuits.
- Autonomy wall: I coined this term while writing this article, and hopefully it illustrates the type of ecosystem that can be created between embedded AI products, data centers, and edge computing assets. Certain tasks may be best left in the data center, while others are best performed on the device. The lack of efficient hardware in the latter area creates a situation where embedded AI systems are only "intelligent" when they have cell service or are in WiFi range.

As mentioned above, the goal is to eventually get AI out of the data center, but the industry initially responded by transplanting data center hardware to embedded devices, basically replicating data center computing (and hardware) on a smaller scale. Newer products are changing that dynamic, and we should expect the range of available products to continue growing.

What's Available Now?

In 2021, multiple processor options and hardware platforms are addressing each of these areas. According to *Fortune Business Insights,* the size of the AI chipset market stood at $8.14 billion in 2019, and the industry is expected to grow to $108.85 billion by 2027, equivalent to a CAGR of 38.9% during the forecast period,[1] with available components and chipsets primarily spanning across GPUs, FPGAs, specialty processors, and supporting components. Some newer options focusing on lightweight devices with small footprints are entering or are in production, while others have been available for some time. Below are just a few examples of components targeting a range of applications essential for truly autonomous devices:

- Google Coral: Google realizes the potential in the embedded AI market, and has responded with a purpose-built AI processor for a range of applications. This component runs on a single PCIe Gen2 lane/USB 2.0 and targets just about anything that can be compiled from TensorFlow Lite.
- Intel Movidius: Some may remember the Movidius USB accelerator stick, which plugged into a desktop and could be used for AI development. Now Intel is marketing its Movidius VPU product for computer vision applications.
- Nvidia GPUs: We shouldn't be surprised Nvidia is pushing hard into this area with newer GPU products. As the undisputed leader in GPUs, with many of its products present in the world's most powerful supercomputers, expect Nvidia to continue producing smaller, more power-efficient products like the Jetson Nano platform.
- Baidu Kunlun 2: The Kunlun 2 AI processor was scheduled to go into production in December 2020. This component targets cloud-to-edge applications, with the goal of breaking the autonomy wall.
- Maxim Integrated MAX78000: The MAX78000 is a lightweight AI processor targeting voice recognition, but it nicely illustrates the push to bring AI into embedded devices that have less resemblance to a typical computer. Don't be surprised when other names in the semiconductor sector follow suit with competitive components.
- MediaTek APUs: First released in 2019, MediaTek's AI processor units (APUs) have been adapted into larger parts of its product portfolio. These processors target embedded devices at all levels, with the newest SoC product targeting AI on 5G smartphones.

This list is not exhaustive and is not intended to be an endorsement. In addition to the companies listed here, a smattering of startups and research laboratories are developing competitive products based on totally reengineered transistor architectures. Si is still the material of choice, but MoS_2 is proving an extremely promising alternative in terms of MAC count and power efficiency. These hardware platforms aim to streamline MAC operations in neural network models with an optimized cascaded fabric (targeting the compute wall) with less power consumption and implementation cost compared to general computing architectures.

Device Architecture and the Embedded AI Ecosystem

The great thing about many of the examples listed above is they can be paired with a range of existing MPUs, FPGAs, and even MCUs, either directly or through an interface bridge. MCU/FPGA-SoC/MPU-based solutions carry smaller cost compared to pure FPGA or GPU-based systems. These types of designs are easier to implement for most embedded designers: Arm Cortex cores still dominate, and manufacturer support for existing MCU/MPU tools can be made immediately extensible to these newer platforms.

The high-level block diagram in FIGURE 1 shows how these components can fit into an embedded system. The AI processor section is shown as an external component, as this is how many components are designed to be used, although newer AI-capable SoCs are likely to follow the broader integration trend seen with many other components.

FIGURE 2 shows how embedded AI-capable devices interface with the edge and the cloud, as the level of compute involved in each area. Lightweight inference tasks can be performed on the device, with the throughput, level of parallelization, and available tasks dependent on the type of processor placed on the device. Higher compute training and inference tasks can be performed at the edge or in the cloud, depending on the amount of data and time required. The benefit of this model is mission-critical inference tasks can be performed in the field without an

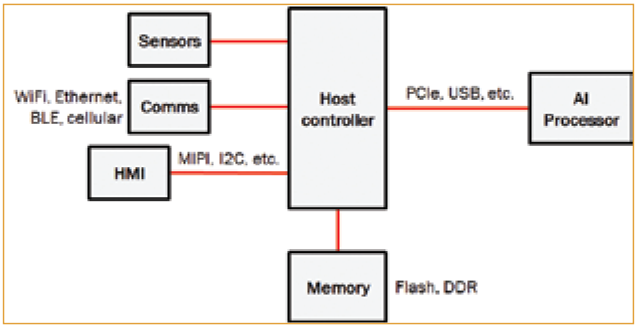

FIGURE 1. High level system block diagram for integrating AI processing into embedded systems.

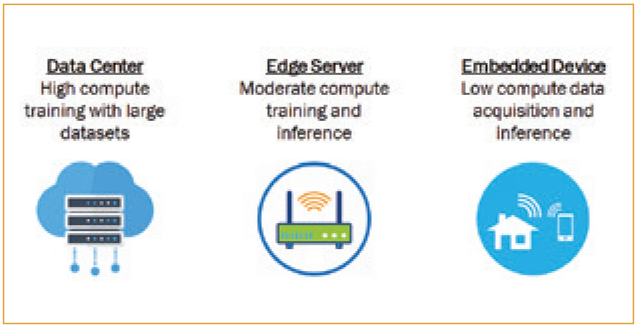

FIGURE 2. AI-capable embedded products in the connected ecosystem.

internet connection. Once an embedded device encounters an internet connection, software/firmware updates can be pushed back to the device. Today's cloud services currently enable this type of ecosystem and integration among multiple services.

Because these components run on the back of existing high-speed (PCIe, USB, MIPI, etc.) and low-speed (I2C, SPI, UART, etc.) protocols, the high-speed PCB designer will be familiar with implementing these components. What's left for the designer to think about? The challenge isn't necessarily one of layout and routing. It's about creating a design that enables a meaningful user experience. At the end of the day, AI is worthless if it does not provide value to the user, even if it's only perceived value.

The other point to consider is the place of the product in the larger computing ecosystem. With PCB designers also playing the role of embedded engineers, they'll have to act more like systems engineers and less like layout engineers. Think about the level of autonomy the product requires, and select AI-enabled processors with this in mind. If we take AI out of the data center and embed it in the field, design reliability becomes critical in many applications, such as aerospace, smart infrastructure, industrial automation, and automotive. Security remains a critical challenge for IoT products and embedded systems in general,[2] and solutions to these challenges will permeate all levels of the AI-enabled embedded ecosystem (device, edge and cloud).

Looking to the Future

We live in a world where AI is used behind the scenes in many tech products and services, but it has also been SaaS-ified to death. Advances in AI-centric ICs provide a new generation of products that enable much more resilient applications in robotics, IoT, industrial automation, and much more. Eventually, as the foundational embedded AI hardware platforms and the ICs that enable them evolve, they will filter back into the data center. I predict less reliance on typical GPUs for the high compute power needed to train machine learning models used in AI, or more specialized GPUs like those in Nvidia's portfolio. PCB designers will continue to be a driving force at all levels, especially because these specialized components will use high-speed computing interfaces requiring meticulous layout and routing. As we gain a deeper understanding of human intelligence and perception, future ICs for embedded AI products may have an entirely new architecture we can't imagine yet. ❑

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Designer's Notebook, continued from pg. 21

silver alloys as the base. The solderable parts will be tinned, with other plating possible. Placement considerations are driven by fitting as much into as little space as possible. Watch the component headroom under the shield, including any webbing and overhang.

Mouse holes: To bury or not to bury the transmission lines; that is the question. Traces can route in or out of the shield on the surface layer through a series of slots located along the base of the wall. Walls with a continuous footprint require internal routing or cutting out a so-called mouse hole in the bottom of the wall where a trace can pass under.

Sometimes the available space demands a special shape for the shield, even though we plan for these things. When generating a bespoke footprint, follow some of the examples by leaving the pattern of mouse holes so that same shield could potentially be used for other purposes or accommodate future growth.

The mouse hole should be at least as high as the dielectric thickness to the reference plane. The width will consider the trace geometry but also the wavelength in some circumstances. Guidelines will range from a quarter of a wavelength to a twentieth, depending on isolation goals.

Holes in the top of the shield are not just for appearances or weight savings, though they accomplish that. The holes in the top work in concert with the lower slots for convective airflow. Another common feature is a few pegs built into the walls that require sizable plated through-holes in the board.

Think about clustering aggressors apart from victims during the floor planning and keep the geometry conducive to being corralled by a Faraday cage. Use the schematic diagram to document which enclosure each component will live in. The earlier you start thinking about isolating the good citizens from the frat boys, the better the outcome. ❑

Laws of PHYSICS

Signals and energy move in the spaces, not in the traces.

by RALPH MORRISON

When a principle of physics is accepted, it explains phenomena everywhere in the universe. The law of gravity works on matter, whether the masses are located on earth, in the sun and or among the stars. The law must transition at the atomic level where the particles must follow the laws of quantum physics. There may also be a transition when dimensions are those of the entire universe. For the world, we can sense there is only one law.

The laws I want to talk about are the basic laws of electricity. I am not referring to circuit theory laws as described by Kirchhoff or Ohm, but to the laws governing the electric and magnetic fields. These fields are fundamental to all electrical activity, whether the phenomenon is lightning, ESD, radar, antennas, sunlight, power generation, analog or digital circuitry. These laws are often called Maxwell's equations.

The energy we get from sunlight travels in space. The energy comes to us as electromagnetic waves. This means there are both electric and magnetic fields present in the light. There are no wires. This field energy is moving at the speed of light.

Visible light is electromagnetic field energy where the wavelength is 10^{-7} meters. Radar is electromagnetic wave energy where the wavelength is 10^{-2} meters. Utility power is electromagnetic wave energy where the wavelength is near 10 million meters. Lenses can direct light energy; waveguides can direct radar energy; and copper conductors can direct the energy at power frequencies. Thus, we direct energy flow at different frequencies by using different materials. We have learned how to control where we want the field energy to go.

If we accept the idea that fields carry energy in space, it must be true at all frequencies. That is the law. If it is true for light, it must also be true for 60Hz power and at DC. For utility power, the energy travels in the space between conductors, not in the conductors. This is not the picture presented by circuit diagrams, where energy seems to be carried by conductors. In digital circuits, the signals and energy travel in the spaces between traces or between traces and conducting surfaces.

Buildings have halls and walls. People move in the halls, not the walls. Circuits have traces and spaces. Signals and energy move in the spaces, not in the traces. ▫

RALPH MORRISON spent more than 50 years in electronics engineering and authored eight books, including *Solving Interference Problems in Electronics, Grounding and Shielding Techniques in Instrumentation,* and *The Fields of Electronics: Understanding Electronics Using Basic Physics.* He passed away in December 2019. He authored this essay in 2010, and it was provided to PCD&F by his protégé Dan Beeker.

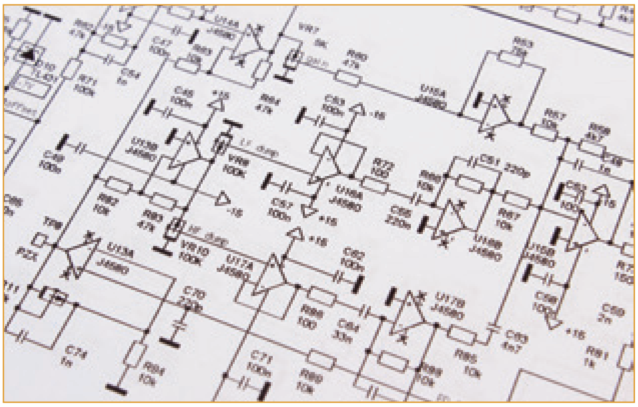

FIGURE 1. Circuit board schematics suggest energy moves through conductors. The laws of physics say otherwise.

Application of Nonlinear Regression for Determining PCB FINISH THICKNESSES

Commonly available tools can determine the relationship between gold thickness and plating time. by PATRICK VALENTINE, PH.D.

Regression analysis utilizes the relationship between quantitative variables to predict one variable from one or more other variables. These relationships are either functional or statistical. Functional relationships have perfect fits. For example, ice cream cones cost $1 each, so one can buy 10 ice cream cones for $10 or 20 ice cream cones for $20. Statistical relationships typically do not have perfect fits. For example, cholesterol levels and body weight have a non-perfect fit. It is commonly accepted that the term "regression" describes the statistical, not the functional, relationship between variables.[1]

A regression model is a formal means of expressing the general tendency of a dependent variable (Y) to vary with the independent variable (X) systematically. The independent variable (X) is also referred to as the predictor variable. George Box (2007) states, "all models are approximations. Essentially, all models are wrong, but some are useful. However, the approximate nature of the model must always be borne in mind" (p. 414), implying there are random errors present, hence the nonperfect fit.[1,2] The expression of the general tendency of a dependent variable (Y) and an independent variable (X) is potent in many different fields.

Regression analysis provides the researcher with three essential purposes: 1) explanation, 2) control and 3) prediction. Explanation describes the statistical relationship between the dependent variable (Y) and the independent variable (X). Control allows the researcher to set bounds on the independent variable (X) to achieve a controlled output range of the dependent variable (Y). Prediction enables the researcher to answer "what if" questions; e.g., setting the independent variable (X) to a non-common value outside of the control range will likely produce what given output of the dependent variable (Y)? Many times, these three purposes overlap in practice. Regression analysis becomes a unique statistical tool for researchers, process engineers and others in various fields.

Regression models have many different types. These models include, but are not limited to, simple linear, multiple linear, nonlinear, orthogonal, calibration, logistic, and Poisson.[1,3] Simple linear regression is a basic regression model with only one predictor variable (X), and the regression function is linear. Simple linear regression models are considered first-order models. The regression equation has no parameters (β_0 intercept or β_1 slope) expressed as an exponent, nor are they multiplied or divided by another parameter. The predictor variable (X) appears only in the first-order. Simple linear regression is a good starting point for exploring statistical relationships. Nonlinear regression is a different animal.

Nonlinear regression models are not first-order models. The regression equation has parameters (θ) theta 1, theta 2, etc., that may be expressed as exponents, multiplied or divided by another parameter, etc. The predictor variable (X) may or may not appear in the first-order. When constructing a nonlinear regression model, the model itself must be chosen, along with the parameter (θ) starting points (theta 1, theta 2, etc.).[3,4] Selecting the model and parameter (θ) starting points (theta 1, theta 2, etc.) requires effort on the researcher's part.

Researchers may not know the actual model tendency of the dependent variable (Y) and the independent variable (X). Without this knowledge, it is challenging to choose a nonlinear model and its starting parameters. In these cases, combining a mechanistic model with an empirical model is a practical approach.[3] Mechanistic models are constructed purely from physical considerations, whereas empirical models are built from data. Small pilot runs can be used for data gathering if no data exist. Combining a mechanistic model with an empirical model provides the best of both worlds. A scatterplot of the data can be constructed and a plausible nonlinear model determined by juxtaposing the scatterplot with graphs of nonlinear models.[4] The most challenging part of nonlinear regression is determining the parameter (θ) theta 1, theta 2, etc., starting points. Microsoft Excel provides a solution.[5]

The Solver is an add-in embedded in Microsoft Excel. The Solver is a sophisticated optimization program that enables one to find solutions to complex linear and nonlinear problems. Solver minimizes the sum of the squared difference between data points and the function describing the data.[6] The Solver uses an iterative process that first requires the researcher to decide the initial starting parameter (θ) values for theta 1, theta 2, etc. Solver's first iteration computes the sum of squares difference. The next iteration involves changing the parameter values by a small amount and recalculating the sum of squares difference. This iterative process is repeated multiple times to achieve the smallest possible value of the sum of squares. A computer algorithm is used for this iterative process.

The researcher can choose from one of three Solver computer algorithms. The three algorithms are 1) Simplex LP Solving method, 2) generalized reduced gradient (GRG), and 3) Evolutionary Solving method. The Simplex LP Solving method can be applied only to linear problems, whereas the GRG and Evolutionary Solving methods can be used for nonlinear problems. The GRG runs faster than the Evolutionary Solving method, but the algorithm can stop at a local optimum, not necessarily at the global optimum. The Evolutionary Solving Method is based on natural selection theory, which makes it run slower, but it is more robust than the GRG algorithm. Using the GRG Multistart option is a good compromise between speed and robustness.

A Worked Example

Electroless nickel immersion gold (ENIG) is the most common printed circuit board final finish in the world. The immersion gold is deposited on the metallic nickel by galvanic corrosion (Equation 1). As the nickel becomes covered with gold, the rate of the gold deposition decreases. The optimum gold thickness is typically around 50 nanometers (nm). If the gold deposit is too thin, the underlying nickel can oxidize during component assembly, resulting in incomplete solder joint formation, i.e., patent defects. If the gold deposit is too thick, it can cause excessive galvanic corrosion of the underlying nickel, resulting in insufficient solder joint reliability; i.e., latent defects.

$$Ni^0 + 2Au^{-1} \rightarrow Ni^{+2} + 2Au^0$$

EQUATION 1. Galvanic corrosion of metallic nickel by ionic gold.

The ENIG process engineer develops a mechanistic model based on Eq. 1 and expects to see the immersion gold plating rate taper off over time. To what extent the immersion gold plating rate tapers off is unknown to the process engineer. Next, the process engineer collects data, under controlled conditions, on gold thickness versus immersion plating time **(TABLE 1)**. Replicates are run to test lack-of-fit during analysis. The process engineer creates a scatterplot **(FIGURE 1)** and then fits a simple linear regression to the data in Table 1 **(FIGURE 2)**.

TABLE 1. Immersion Gold vs. Plating Time

Time (min)	Gold (nm)
0	0.0
2	28.2
2	28.3
4	43.0
4	37.4
4	39.9
8	52.3
8	49.5
8	48.8
12	57.3
16	64.0

The process engineer examines the scatterplot in Figure 1. The scatterplot reveals a nonlinear pattern. There appear to be different slopes from zero to two minutes, two to four minutes, four to eight minutes, and eight to 16 minutes. The scatterplot results corroborate the mechanistic model developed from Eq. 1.

Next, the process engineer examines the simple linear regression seen in Figure 2. There is evidence the simple linear regression fit is inadequate for this empirical model. While the adjusted R-squared value of 74.8% may be acceptable in some circumstances, the simple linear regression reveals a nonlinear pattern. Of more concern is the statistically significant ($\alpha = 0.05$) p-value of 0.001 for the lack-of-fit, indicating the model does not correctly specify the statistical relationship between gold thickness and the plating time; a higher-order term in the model is needed. To further explore the model, the process engineer uses the simple linear regression equation in Figure 2 to predict gold thickness at eight minutes, seen in Eq. 2. The lack-of-fit problem causes the prediction interval for the eight-minute plating time to be broad. The mechanistic and empirical models provide the process engineer enough evidence to warrant fitting a nonlinear regression model.

$$\textit{Gold (nm)} = 20.8 + (3.2 \times 8) = 45.6nm$$

$$\textit{95\% Prediction Interval} = 25.7 \textit{ to } 67.5nm$$

EQUATION 2. Expected gold thickness with eight-minute dwell time, linear fit.

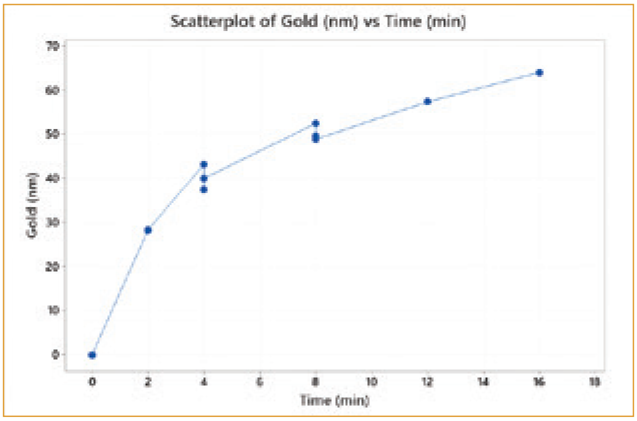

FIGURE 1. Scatterplot of the data in Table 1.

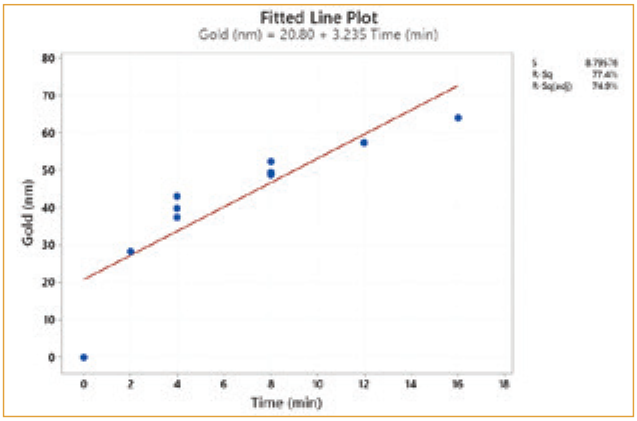

FIGURE 2. Simple linear regression of the data in Table 1.

The process engineer now must find a nonlinear regression function that closely matches the scatterplot in Figure 1. Searching through Minitab's nonlinear regression design catalog, the process engineer finds the Michaelis-Menten function, which appears to be a good fit **(FIGURE 3)**. The Michaelis-Menten function describes the rate of reaction as a function of substrate concentration: in this case, gold thickness versus time. The Michaelis-Menten function aligns well with the mechanistic model developed from Eq. 1. The Michaelis-Menten function has two parameters (θ), theta 1, and theta 2, which need starting values determined. The process engineer now turns to Microsoft Excel Solver.

The process engineer then builds the Michaelis-Menten function in Microsoft Excel **(FIGURE 4)**. Five essential inputs are needed: 1) fit, 2) residuals, 3) sum of square errors (SSE), 4) theta 1, and 5) theta 2. In Figure 4, the input values and mathematical equations are listed in cells A16 through B20. The

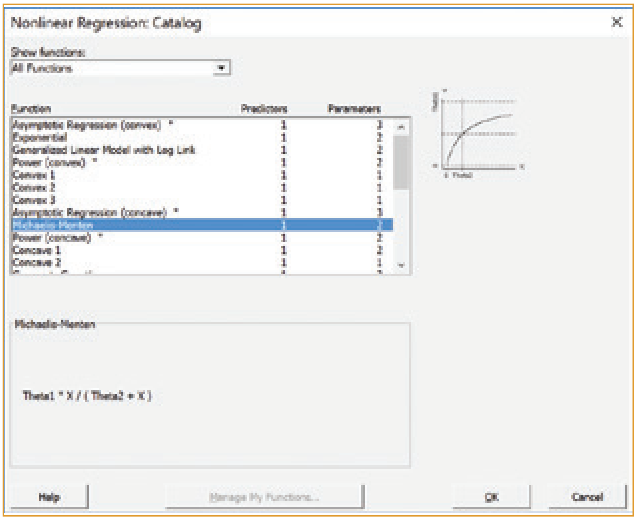

FIGURE 3. Michaelis-Menten nonlinear function.

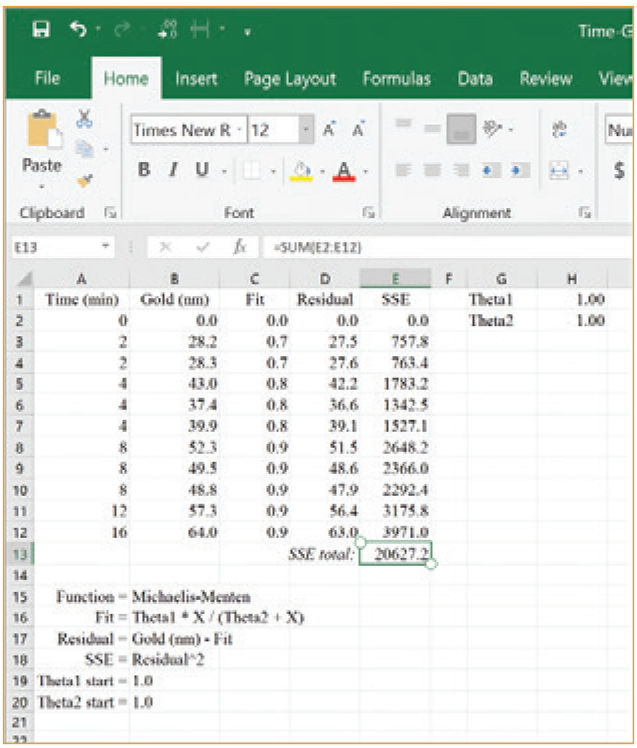

FIGURE 4. Michaelis-Menten nonlinear function setup in Microsoft Excel.

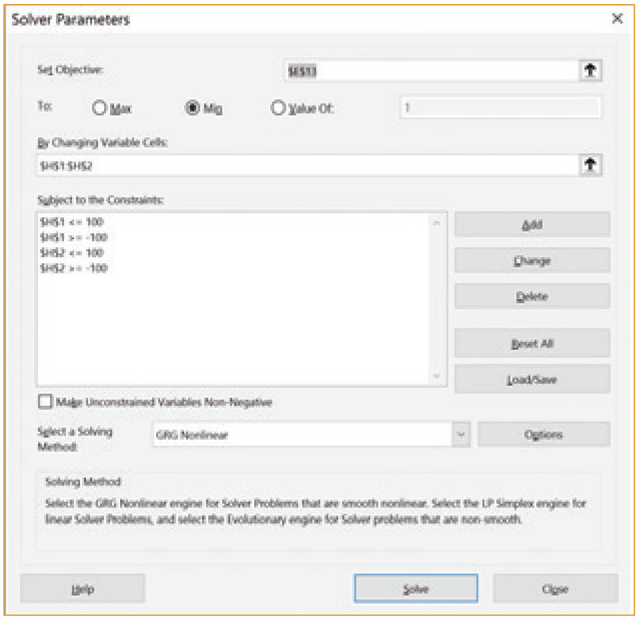

FIGURE 5. Solver setup in Microsoft Excel.

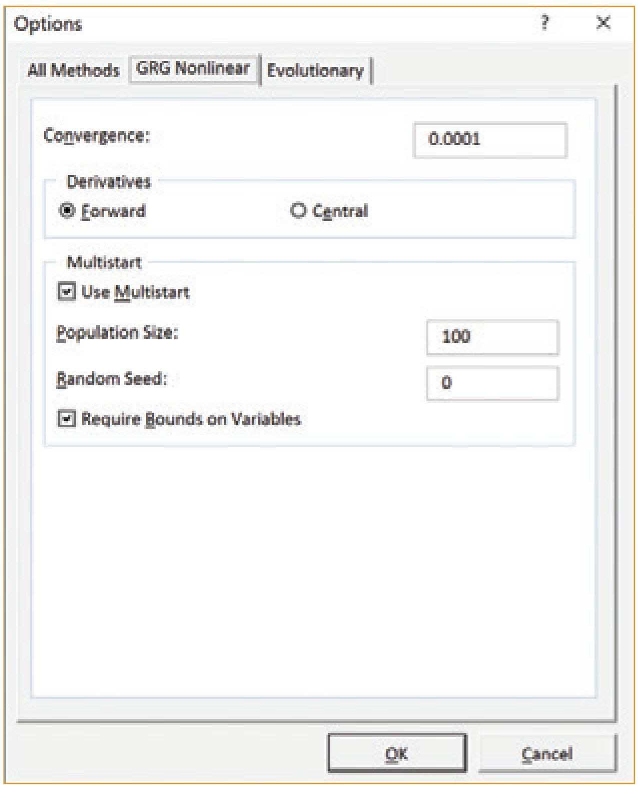

FIGURE 6. Solver multistart option in Microsoft Excel.

starting parameters (θ) for theta 1 and theta 2 are set at 1.0 for convenience. Next, the process engineer needs to set up Solver.

Seven crucial inputs are needed for Solver: 1) set objective cell, 2) to value, 3) by changing variable cells, 4) subject to the constraints, 5) make unconstrained variables non-negative, 6) select a solving method, and 7) multistart option. The process engineer inputs the values shown in **FIGURES 5** and **6**. The "objective cell" is assigned to the total SSE; the "to value" is set to minimize; the "changing variable cells" are assigned to theta 1 and theta 2; constraints are added to the "subject to the constraints" (note: the multistart option requires constraints); "make unconstrained variables non-negative" is unchecked; the "solving method" is set to GRG, and the "multistart" option is checked. The process engineer sets the "subject to the constraints" from -100 to +100 to permit wide latitude for the multistart option. Unchecking the "make unconstrained variables non-negative" permits Solver more freedom in finding a global solution. The process engineer runs Solver, and the results are shown in **FIGURE 7**.

Solver has found a global solution for this nonlinear problem. The SSE has been minimized to 41.7. Optimum parameters (θ) for theta 1 (73.9) and theta 2 (3.4) have been found. The process engineer now transfers the optimum values of theta 1 and theta 2 into their statistical software package, fits the nonlinear regression, and checks the diagnostics. The nonlinear regression is shown in **FIGURE 8**, the residual plots are shown in **FIGURE 9**, and the eight-minute gold thickness prediction using the nonlinear regression equation is shown in Equation 3.

$$\text{Gold (nm)} = 73.9 \times 8 / (3.4 + 8) = 51.8\text{nm}$$

$$\text{95\% Prediction Interval} = 46.6 \text{ to } 56.9\text{nm}$$

EQUATION 3. Expected gold thickness with eight-minute dwell time, nonlinear fit.

The nonlinear regression shown in Figure 8 fits the data well. The lack-of-fit p-value is 0.473, indicating a lack of evidence to reject the null hypothesis; i.e., the model correctly specifies the statistical relationship between gold thickness and the plating time. The residual plots shown in Figure 9 look normal. The prediction interval for the eight-minute plating time shown in equation 3 is narrow and uniform. The nonlinear regression has been validated and can be used to explain, control and predict.

Conclusion

Nonlinear regression analysis is a unique statistical tool for researchers, process engineers, and others in various fields. Nonlinear regression analysis provides three essential purposes: 1) explanation, 2) control and 3) prediction. In many situations, nonlinear regression can explain mechanistic models better than linear regression. Nonlinear regression has its challenges, though, explicitly choosing the appropriate model and its starting parameters. With nonlinear regression design catalogs, one can use intuition to find a suitable model. Microsoft Excel Solver can easily be used to find the starting parameters. Once a nonlinear regression has been fit, a thorough evaluation of the diagnostics is in order. ▫

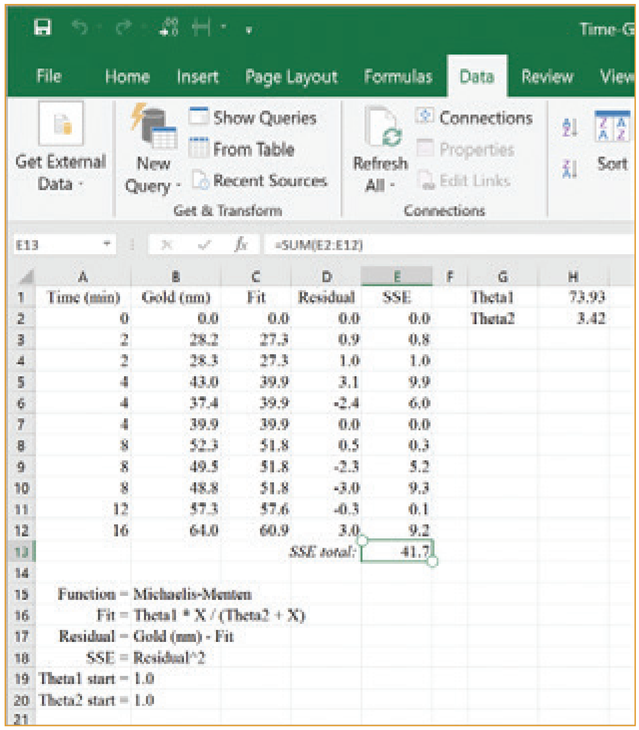

FIGURE 7. Solver solution.

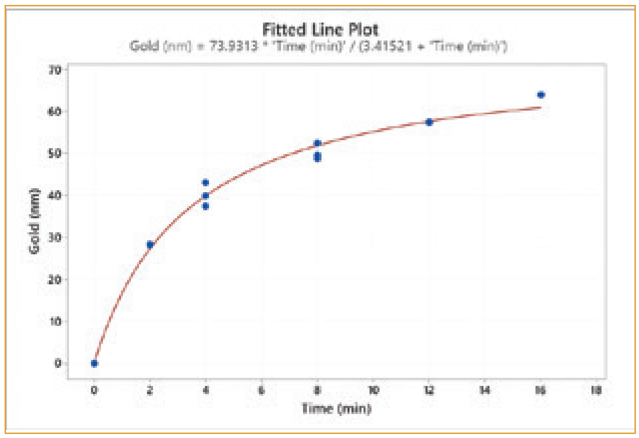

FIGURE 8. Nonlinear regression of the data in Table 1.

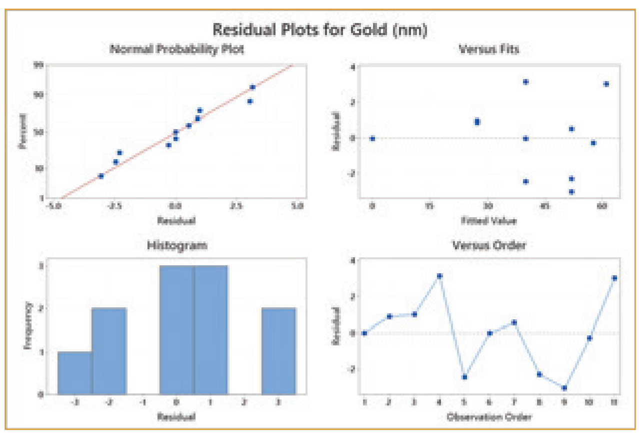

FIGURE 9. Nonlinear regression residual plots.

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Cost-Efficient LASER DEPANELING

Machine and operational costs have shrunk over the past decade. **by PATRICK STOCKBRUEGGER**

For years, the word in the electronics industry has been laser depaneling is expensive. This may have been true for investments in laser machines a decade or more ago, but the situation looks different once operating expenses are accounted for, especially with newer systems. In fact, according to our data, depaneling with laser systems is the most efficient method for a range of applications, and the cutting results are excellent, which means quality standards are also met.

The trend in the price-to-performance ratio for current laser systems, especially with respect to production of rigid PCBs, is obvious: The cost of depaneling based on the effective cutting speed has fallen to approximately one-tenth of what it was a decade ago **(FIGURE 1)**. This dramatic shift is based on three major factors, all based on the rapid advances in laser technology. First, capex cost for laser depaneling systems has decreased to almost 30% of what it used to be a decade ago. Second, overall throughput has improved more than seven times. Finally, the operational costs for energy and maintenance have noticeably decreased.

This phenomenon has two main drivers. Material costs are much lower today than a few years ago, and the performance of laser systems has improved dramatically due to integration of more powerful lasers and more advanced process know-how.

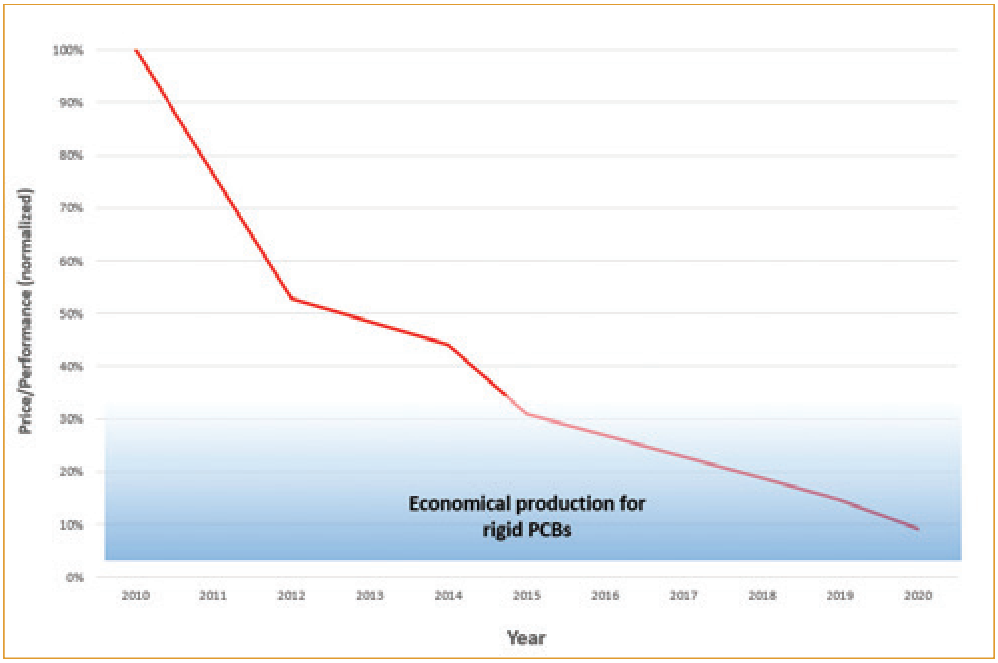

FIGURE 1. Changes in price-to-performance ratio for laser depaneling systems, 2010 to 2020. Source: LPKF

Cutting Upstream Processes

Modern laser systems enable savings in terms of PCB material of more than 30% on average. This is made possible by utilizing a full-perimeter cut through the panels with the laser, rather than cutting tabs of pre-routed boards **(FIGURE 2)**.

With a full-perimeter cut, PCBs can be spaced closely together for minimal material loss, taking full advantage of the narrow kerf width of a laser tool, which is typically around 20µm vs. a 1 to 2mm router bit. This eliminates the space otherwise occupied by pre-routing lanes around each PCB on the panel. Another advantage is the variable and precise laser guidance and the narrowest possible cut to accommodate intricate geometries for optimum material utilization. Through these factors, laser systems realize savings, especially for smaller PCBs.

In addition, the costs of upstream process steps are reduced, and users also profit from indirect savings because of the higher number of PCBs per panel. The handling time for the individual PCB is reduced, and human errors caused by manual handling are minimized.

Unlike with milling machines, there are no significant operating expenses. The laser as a tool has no mechanical wear, and the quality of the laser is constant. There is no need to replace saw blades or router bits, which eliminates related unproductive downtime and cost to replace such parts.

To maintain a constant MTBF and minimum downtime, the preventive maintenance work on laser systems is done at longer and planned intervals and is therefore less disruptive to day-to-day productivity. Common wear parts include laser diodes, which last two to three years and typically cost in the mid four-figures.

Error Minimization

For high volumes, laser machines integrated into production lines are often advantageous. Extensive automation often reduces manual errors.

Lasers in PCB depaneling operations eliminate dust and stress to the PCB, drastically improving production yield. Unlike traditional mechanical depaneling methods, laser depaneling machines do not generate milling dust, which can become airborne and cause quality issues anywhere in the plant, and may cause health problems for employees exposed to these airborne particulates. Lasers do not create the mechanical stresses that are imparted when using a dicing saw or router, which could jeopardize the functionality of sensitive components on the circuit board or even compromise the integrity of the board itself. In addition, laser depaneling systems create absolutely no burr and maintain a much higher tolerance of the board outline, which is particularly important for intricate-shaped circuit boards that must fit into tight spaces (e.g., wearables and sensors). PCB manufacturers achieve higher quality and better yield when laser depaneling systems are being used. These two factors together provide a significant advantage over traditional depaneling technologies.

Energy Efficiency

Even if it seemed at first the energy use for depaneling was negligible for many production facilities, this factor is often considered more carefully today. Over the years, laser performance has risen considerably, while its overall power consumption has dropped significantly. This translates into a sixfold increase in overall energy efficiency – a remarkable factor that can currently only be achieved by laser technology. A modern laser system is effectively depaneling seven times as many boards using the same amount of electrical power compared to a system from a decade ago (**FIGURE 3**).

Conclusion

Modern laser machines for depaneling of rigid and flexible PCBs save on material costs and handling efforts, and improved production quality, which equates to higher yield. The return on this investment is easy math: Although today's depaneling lasers can be 20 to 30% more expensive than a router in capital cost, they overcome this difference with higher productivity, especially for board thicknesses less than 0.62 mils (1.6mm) where lasers are substantially faster. In addition, laser systems capitalize on additional savings of up to 30% in overall board material cost by using full laser cut and eliminate the cost and downtime of permanent tool changes. ❑

Ed.: For a look at how laser depanelers work, click here: https://vimeo.com/524306607

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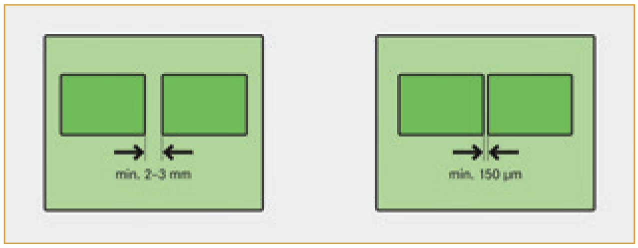

FIGURE 2. Typical distance for routing lanes with mechanical routers (left) and laser depaneling systems (right). Source: LPKF

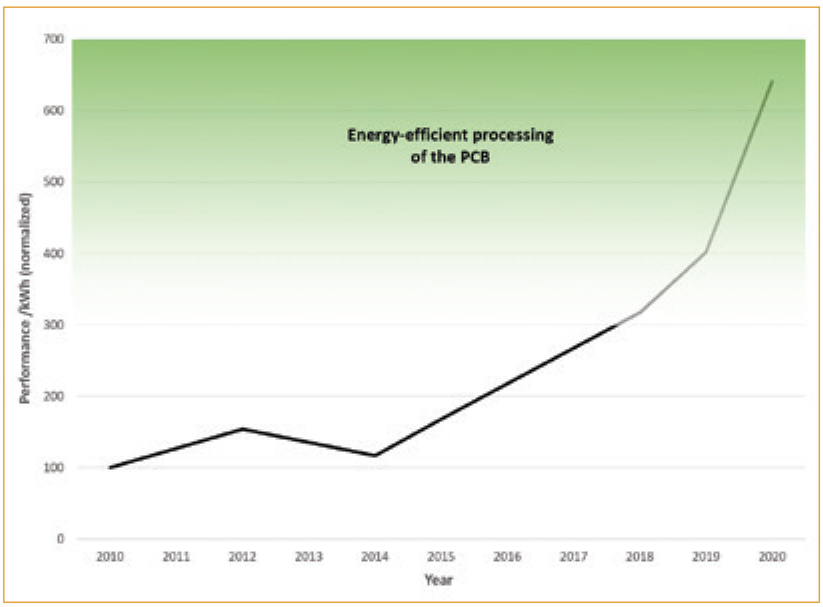

FIGURE 3. Changes in energy efficiency, 2010 to 2020. Source: LPKF

Let Your Factory Speak for Itself

Getting machines to talk to each other enhances output and yields.

IT'S COMMON SENSE, really, and probably one of the most familiar sayings of mankind: Communication is key. Good communication is central to productive relationships, effective business strategy … just about everything, honestly. It's not just communication, however, but communication quality and transparency that result in informed decision-making. This is especially true in the manufacturing setting and is the basis for Industry 4.0. Machines have been cranking out data for decades, but applying them in a meaningful way is, at the core, what Industry 4.0 is all about. Until recently, however, data exchange was largely supplier-specific; proprietary equipment system software could manage tasks rather seamlessly, but communication among disparate equipment brands in relation to PCB movement and traceability was challenging. The IPC-SMEMA-9851 standard provides a solid foundation and is still successfully employed, yet enhancements are required to progress toward a nimbler, automation-friendly solution that permits open and uniform machine-to-machine communication.

"ANALYZING THE DATA STREAM **IN REAL TIME** ALLOWS FULL, CLOSED-LOOP **PROCESS CONTROL** WITHIN THE DEMANDING PROCESS OF **STENCIL PRINTING.**"

How it started. While several stencil printer platforms and everything within their respective ecosystems – board handling equipment, SPI and closed-loop feedback tools – are data rich, self-correcting and optimized for the printing operation, the data generated by printers relating to the PCB characteristics must be passed down the line. That, of course, means the data must be vendor-neutral. Moving beyond simple board recognition from one system to the next, true traceability is required for smart factory effectiveness. Consequently, the Hermes Standard Initiative (IPC-HERMES-9852) was born as the result of more than a dozen equipment vendors unifying behind the cause for an improved open communication protocol, which speaks volumes for the requirement and the customer desire for such a solution. By simplifying the transfer of PCB data between machines regardless of supplier, efficiency and productivity improvement are a given. And, with scalability options, board data can be customized so that when the PCB is passed from, say, the printer to the placement machine, each machine is compelled to recognize the data set, potentially add to it, and transfer that record through the assembly line, making for a more holistic view of the PCB. In fact, these data represent the digital twin of the physical PCB, and Hermes transports the PCB and its digital twin consistently down the SMT line. Integrating Hermes with IPC's Connected Factory Exchange (CFX) standard broadens this line efficiency and communication transparency to the factory, while other MES systems can extend that to the global enterprise.

For the printing operation, the potential efficiency benefits of Hermes are immense. In manufacturing sites that require multiple changeovers per day, for example, the ability to seamlessly reconfigure the printer through automatic conveyor system adjustments, corresponding program-loading and verification of proper material sets (solder paste, stencils, etc.) saves time, the potential for human error and the related costs of mistakes. Optimized board flow management enabled by Hermes raises line efficiency, with board location in-process aiding adjustments upstream or downstream to facilitate a continuous pace. Within the print optimization loop, CFX allows the SPI platform to feed its data stream into a process analysis system, transforming the data into information and then into knowledge, spurring small but continuous process corrections to the printing process. As this column frequently illuminates, the printing operation is affected by many factors. Having the data stream analyzed in real time allows

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full, closed-loop process control within this demanding process. Other data streams that can be transformed into knowledge using the CFX framework include material/logistics/quality of raw materials, work in process (WIP) and finished product. Equipment utilization and predictive maintenance data can also be captured.

How it's going. To be fair, the industry is only at the start and has a long way to go, but the standards are now established. As of last November, 58 suppliers have signed on as members, and factories worldwide are increasingly embracing Hermes, as well as other higher-level powerful communications for factory and enterprise Industry 4.0 manufacturing. For early adopters, such as a North American customer that installed a Hermes and CFX-equipped line in early 2020, immediate improvements have been noted. That assembler commented the cutting-edge connectivity led to significantly reduced setup times and nearly eliminated process variation for extreme productivity. Indeed, the ability to carry out full product changeovers for the entire line with less operator intervention is one example of how this technology can reduce the resources required for low-value routine tasks. Other practical examples are seen at manufacturers of high-end industrial assemblies. These customers have small (<300 units) runs; therefore, many changeovers are performed every shift. Hermes capability saves them considerable time, enabling more productive resource allocation and eliminating potentially expensive errors.

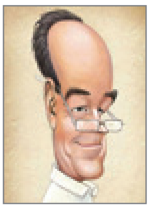
The core of communication is transparency, comprehensiveness and analysis; this is the heart of Industry 4.0. With the Hermes and CFX standards in place and industry adoption on the rise, the lines of communication are open. Welcome to the smart factory. ❑

IPC-HERMES-9852

Spotting Solder Contamination

Gold boards are susceptible to the defect.

BOB WILLIS is a process engineering consultant; bob@bobwillis.co.uk. His column appears monthly.



THIS MONTH WE look at solder spotting, which is often seen after first- or double-sided reflow, most commonly on gold boards. The two examples below illustrate what happens. **FIGURE 1A** shows two spots on a nickel/gold pad, and **FIGURE 1B** shows one spot on a copper OSP pad finish.

Solder spots are basically the result from one or more particles of solder paste in random positions on gold pads. When the board is reflowed, these also reflow and wet the gold. In some cases, they are a cause for rejection, if the gold area is a contact point, bond pad or other functional point. If a spot is random and will not affect the product function, it should be considered cosmetic.

The most common reasons for these faults are board rinses or paste spitting. In the case of rinsing, it starts with poorly printed boards that are sent for cleaning. If the cleaning step is not done correctly, however, paste particles may remain. It's not uncommon with water-soluble solder paste, or paste that has been reflowed with an aggressive profile: Small particles of flux and solder can be ejected from the bulk of the solder during reflow. This Defect of the Month video explains some of the dos and don'ts (https://vimeo.com/525156200).

We have presented live process defect clinics at exhibitions all over the world. Many of our Defect of the Month videos are available online at youtube.com/user/mrbobwillis. ❑

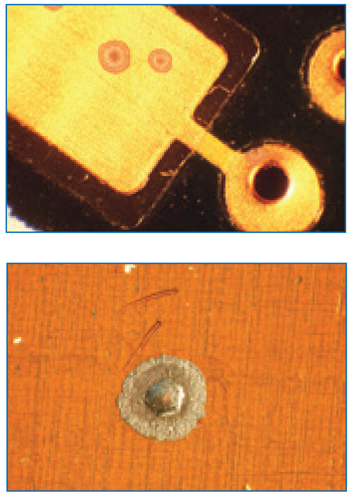


FIGURE 1. Solder spots on a NiAu pad (top) and a single spot on a copper OSP pad finish (bottom).

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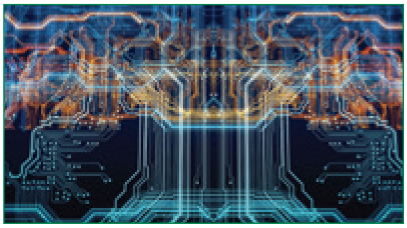
LLC152D70G105ME01 ultra-thin LW-reversed, low-equivalent series inductor MLCC has capacitance value of 1.0µF ±20% for 4 Vdc-rated automotive applications. Is 0204" (0.5 x 1mm) and has max. thickness of 0.22mm. Can be implemented on back of processor package. Construction flips electrodes through 90° so they are positioned on long side of rectangular chip; reverses length-to-width ratio. Achieves low-impedance design.

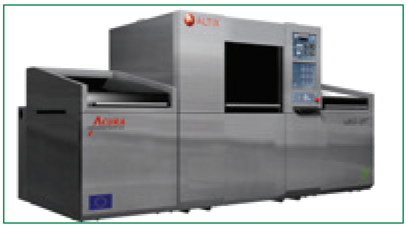
Murata
murata.com/en-us



CADENCE SIGRITY X

Sigrity X signal and power integrity (SI/PI) software features new simulation engines for system-level analysis for 5G communications, automotive, hyperscale computing, and aerospace and defense applications. Reportedly delivers up to 10x performance gain for simulation speed and design capacity. Streamlines setup time for detailed system-level SI/PI analysis by transitioning across different analysis workflows.

Cadence
cadence.com



ALTIX ACURA

Acura Premium contact printer is for innerlayer, outer layer and solder mask processes. Integrates high-performance LED light sources, while keeping collimated light sources optional. Double-sided simultaneous exposure capabilities. Combines wide-angle rocking upper-frame and dual-screen display.

Altix
altix.fr/en

OTHERS OF NOTE

HIROSE FH63S SERIES

FH63S series shielded flexible printed circuit connector has patented single-action flip lock. Features ground pin to work with shielded FFC for EMI prevention and optimum signal integrity. Is 0.5mm pitch and supports HDMI 1.4a, USB 3.0, Embedded Display Pot 1.3, and V-by-One HS protocols.

Hirose Electric
hirose.com

VISHAY EP1

EP1 wet tantalum capacitor has new ratings in B and C case codes. Offers high capacitance per voltage rating and case size. Comes in radial through-hole or SMT terminations in A, B, and C case codes, each with stud-mount option. Capacitance from 3,600µF to 40,000µF in B case code and 5,300µF to 58,000µF in C case code.

Vishay
vishay.com

STACKPOLE RNCF0402

RNCF0402 precision Nichrome chip resistor now has power rating to 0.1W for resistance values from 4.7Ω to 255KΩ for 0.1% tolerances and 25ppm TCR. For applications that normally require 0603 or 0805 resistor. For consumer electronics, computer and telecom equipment, measurement systems, instrumentation, medical monitoring, and high-end commercial audio devices.

Stackpole Electronics
seielect.com

C&K PTS845, PTS850

PTS845 and PTS850 compact tact SMT switches are for portable electronics, including headsets, sports watches, health monitoring devices, Bluetooth accessories, black boxes, and navigation. PTS845 is 4.5 x 3.4 x 3.3mm and comes in three standard actuation forces (80, 160 and 260gf). PTS850 is 5.4 x 5 x 1.8mm and comes in 180 and 350gf versions.

C&K
ckswitches.com

POLAR INSTRUMENTS ATLAS

Atlas for Anritsu ShockLine vector network analyzers is for production testing of PCB insertion loss. Focuses on material qualification and test of high-speed serial data busses at PCB fabrication level. Combines Atlas insertion loss test and data logging software with Anritsu MS46524B-043 43.5 GHz VNA. Addresses Delta-L test needs for emerging PCB designs.

Polar Instruments
polarinstruments.com

TE FREE HEIGHT COM CONNECTORS

Free height computer-on-module (COM) connectors with 0.5mm centerline address vertical, parallel and board-to-board connections that require high-speed data transmission and different stacking heights. Compliant with COM Express Type 7 spec and can be compatible with PCIe Gen 4 protocol. Support up to 16GT/s. Improved signal integrity supported by low insertion loss, return loss, PSNEXT and PSFEXT, whether using both new receptacles and plugs or mating new receptacles with older plugs.

TE Connectivity
te.com

ASM SIPLACE TX MICRON

Siplace TX Micron, for advanced packaging and high-density applications, has improved 20-nozzle SpeedStar high-speed placement head that increases performance 23% to up to 96,000cph, while increasing component spectrum 37%. Handles 25, 20 and 15µm @3Σ to operate with component pitches of 50µm and place 0201m components at full speed.

ASM
asm-smt.com

SCIENSCOPE REEL SMART LITE

Reel Smart Lite (IMS-100) and Reel Smart Pro (IMS-200) incoming material stations provide integration from start to finish. IMS-100 has high-resolution barcode camera system with an image-based algorithm that reads any barcode, even with defects. Reads and stores information of four 7" reels simultaneously. IMS-200 is updated to include automatic loader and label placement.

Scienscope
scienscope.com

VISCOM IX7059

iX7059 heavy-duty inline automated x-ray inspection system has new transport system for workpiece carriers and soldering frames. Transports assemblies with dimensions up to 500 x 500mm and up to 40kg. Performs 2-D, 2.5-D, and 3-D analyses. Resolution range of 8µm to more than 30µm, depending on configuration. Complex inspection objects are irradiated with 130kV or 160kV (optional).

Viscom
viscom.com

OTHERS OF NOTE

ECHO SUPPLY POLYIMIDE MASKING TAPE

Low-ESD polyimide masking tape has width options ranging from 0.125" to 3.0". Is 36 yds. in length. Protects gold fingers on PCBs during wave soldering. Is made with 1-mil-thin polyimide film and 2.4 mils of anti-static silicone adhesive. Removes cleanly from PCBs and has high conformability.

Echo Supply
echosupply.com

MACDERMID ALPHA HITECH CF31-4010

HiTech CF31-4010 is a one-component, high filler content, heat-curable cornerfill. Is epoxy-based material to be dispensed on the corner (corner bonding) or edges (edge bonding) of BGAs. Upon completion of curing process, cured cornerfill helps strengthen soldered, assembled component, permitting it to pass reliability tests such as drop shock, impact bend and thermal cycle. Reworkable.

MacDermid Alpha
macdermidalpha.com

YXLON CHEETAH, COUGAR EVO

Cheetah and Cougar EVO microfocus x-ray systems are upgraded to include visualization with FF CT software as standard. Software remains compatible with volume graphics and corresponding analysis tools. ORYX 1616 high-res flat-panel detector with size of 1280 x 1280 pixels has been introduced; offers field-of-view extension of 50% compared to standard version. Work with much lower radiation dose due to sensitivity. Optional high load capacity.

Yxlon
yxlon.com

PETERS ELPESPEC R 5807

Elpespec R 5807 cleaning agent avoids side reactions in moisture cross-linking silicone coatings. Reportedly uses 1/3 or less concentration compared to other cleaning agents. Is said to provide efficient machine run times, minimized maintenance efforts and higher process stability. Avoids curing reactions within lacquer supply.

Peters
peters.de

INDIUM CW-232

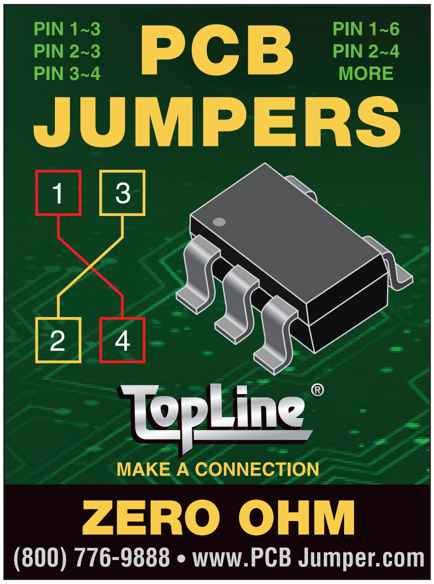
CW-232 flux-cored wire combines wetting speed and spread with low-spatter performance. Is activated rosin flux-cored wire developed to meet requirements of robotic and laser solder applications. Reportedly delivers additional wetting power to achieve higher throughput. Works well in hand-soldering applications. Is compatible with Pb-free and SnPb alloys and HASL, immersion silver, ENIG, and OSP surface finishes.

Indium
indium.com

SAKI JOB DATA CONVERT FUNCTION

Job Data Convert function enables automatic generation of data for board inspection on Saki 3D AOI systems by using component information data generated for pick-and-place machines. Reportedly reduces time to create board inspection programs by directly importing pick-and-place data to automatically generate library for PCBA inspection. Simplifies programming procedures and training for programming.

Saki Corp.
sakicorp.com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In Case You Missed It

Material Procurement

"Selecting Alternate Grade Parts: The Trials and Tribulations"

Authors: Dave Greinke and Christine Metz

Abstract: Selecting a new or replacement alternate-grade part, such as an automotive-grade connector for a military or aerospace system, can be tricky. The best approach uses an already qualified, approved, and preferred part with known reliability and longevity characteristics. However, with lengthening lifecycles for military systems, rapid technology development, material shortages, and other factors, replacements may be needed for parts that are no longer in production or otherwise available. Given this situation, employing established parts management and diminishing manufacturing sources and material shortages (DMSMS) management procedures can assist in finding and selecting alternate-grade parts to fit a system's need. (*Defense Acquisition Magazine,* March-April 2021, www.dau.edu/library/defense-atl/blog/Selecting-Alternate-Grade-Parts-The-Trials-and-Tribulations)

Solder Joint Reliability

"Lifetime Prediction of a SiC Power Module by Micron/Submicron Ag Sinter Joining Based on Fatigue, Creep and Thermal Properties from Room Temperature to High Temperature"

Author: Chuantong Chen, *et al.*

Abstract: Ag sinter joining technology has gained increasing attention for its excellent thermal and mechanical properties, especially for high-temperature applications. This study focuses on the lifetime prediction of a SiC power module by Ag sinter joining based on mechanical properties, including tensile, fatigue, and creep properties from room temperature to 200°C, as well as thermal properties including thermal conduction and the coefficient of thermal expansion. These mechanical properties and thermal properties of sintered Ag paste were evaluated, and the results show mechanical properties of sintered Ag largely depend on the test temperature. The sintered Ag paste tends to soften at high temperature, and the fracture changed from nearly brittle to totally ductile with the testing temperature increase. From the S-N curve, the fatigue is close to the Morrow equation, but not the Coffin-Manson law at room temperature. The finite element simulation of the lifetime based on Morrow's equation for the sintered Ag layer shows there was a crack occurrence with one fourth the side length after 10,000 cycles from -40° to 200°C, but the crack extension area is less than one-tenth of the sintered Ag layer. (*Journal of Electronic Materials,* August 2020, https://link.springer.com/article/10.1007/s11664-020-08410-5)

"Mechanical Reliability of Self-Aligned Chip Assembly after Reflow Soldering Process"

Authors: Mohd Najib Ali Mokhtar, M.Z. Abdullah, Abdullah Aziz Saad and Fakhrozi Cheanis

Abstract: This paper focuses on the reliability of the solder joint after the self-alignment phenomenon during reflow soldering. The aim of this study is to analyze joint quality of the self-alignment assemblies of SnAg alloy solder joints with varying silver content. The results from the mechanical reliability study indicate decreasing trends in the shear strength value as misalignment offset increased. For shift mode configuration in the range of 0-300µm, the resulting chip assembly inspection after the reflow process was in line with IPC-A-610G. Statistical analysis shows the solder type variation was insignificant to the shear strength of the chip resistor. The study concludes the fracture occurred partially in the termination metallization at the lower part of the chip resistor. The copper content of the joint on that area shows the crack occurred in the solder joint, and high silver content on the selected zone indicated the fracture happened partially in the termination structure, as the termination structure of the lead-free chip resistor consists of an inner layer of silver and an outer layer of tin. (*Soldering & Surface Mount Technology,* April 2021, emerald.com/insight/content/doi/10.1108/SSMT-12-2019-0042/full/html)

This column provides abstracts from recent industry conferences and company white papers. Our goal is to provide an added opportunity for readers to keep abreast of technology and business trends.