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# PRINTED CIRCUIT DESIGN & FAB

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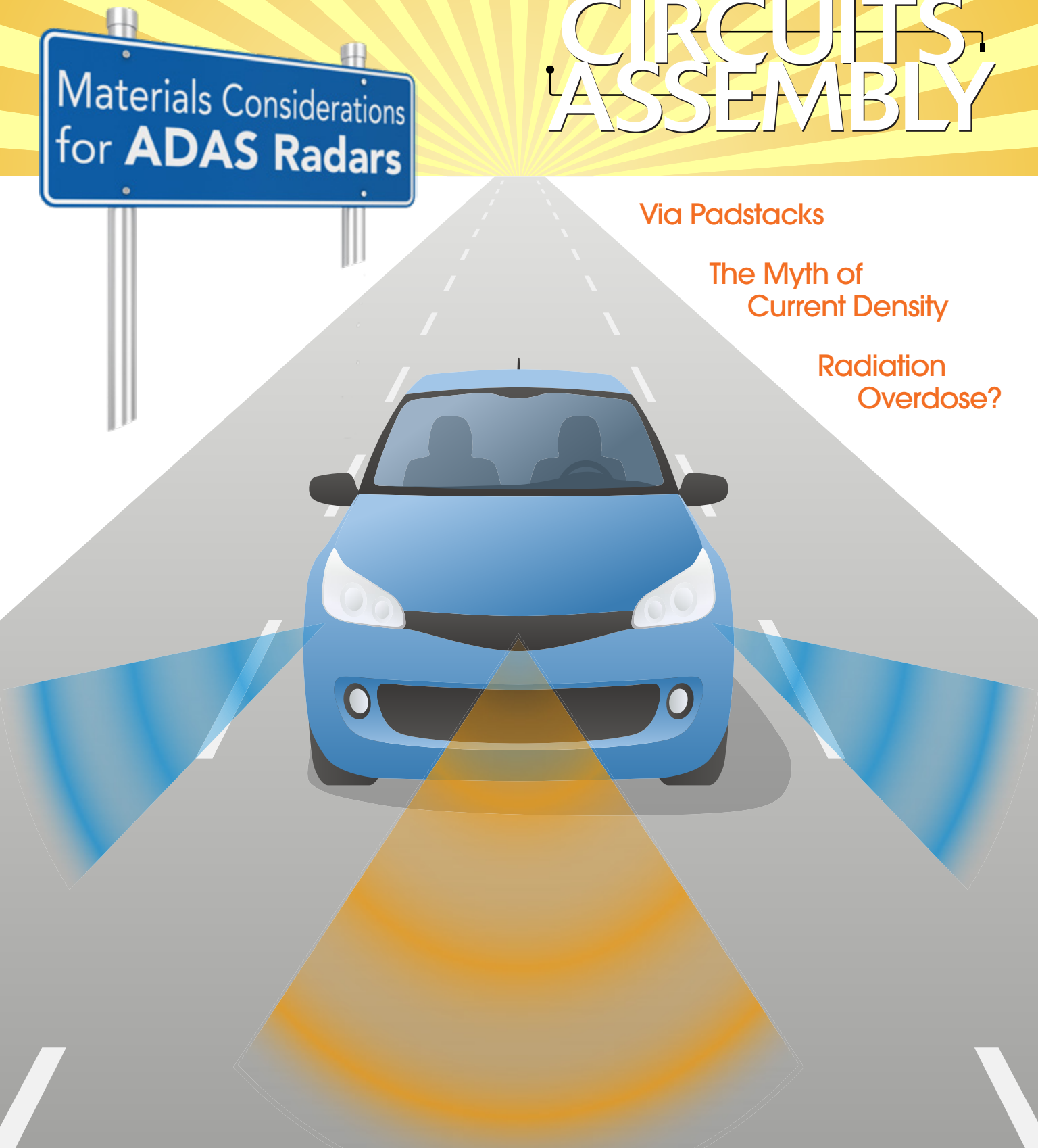


Via Padstacks

The Myth of Current Density

Radiation Overdose?

# ON-DEMAND WEBINAR

## It's All About the Space: A Tribute to Ralph Morrison

- **Introduction by Daniel Beeker**
- **Life, Education and Publications**
- **Ralph's Rules**
  - Field Stays Put
  - Electromagnetic Field Energy
  - The Rule of Triplets
- **How a Signal Propagates on a Microstrip**
- **PC Board Design for Low EMI: Rules**
  - Typical, But Poor, 4-Layer Design
  - Lower EMI 4-Layer Board Stack-Up
  - Lower EMI 6-Layer Board Stack-Up
  - Lower EMI 8-Layer Board Stack-Up
  - Very POOR 8-Layer PC Board
  - Very POOR 10-Layer PC Board
- **Discontinuous Return Paths & Crossing Gaps**
- **Demo-Gap in Return Plane**
- **Difference Between Gapped and Ungapped Traces**

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https://pages.protoexpress.com/ralph-morrison-webinar.html

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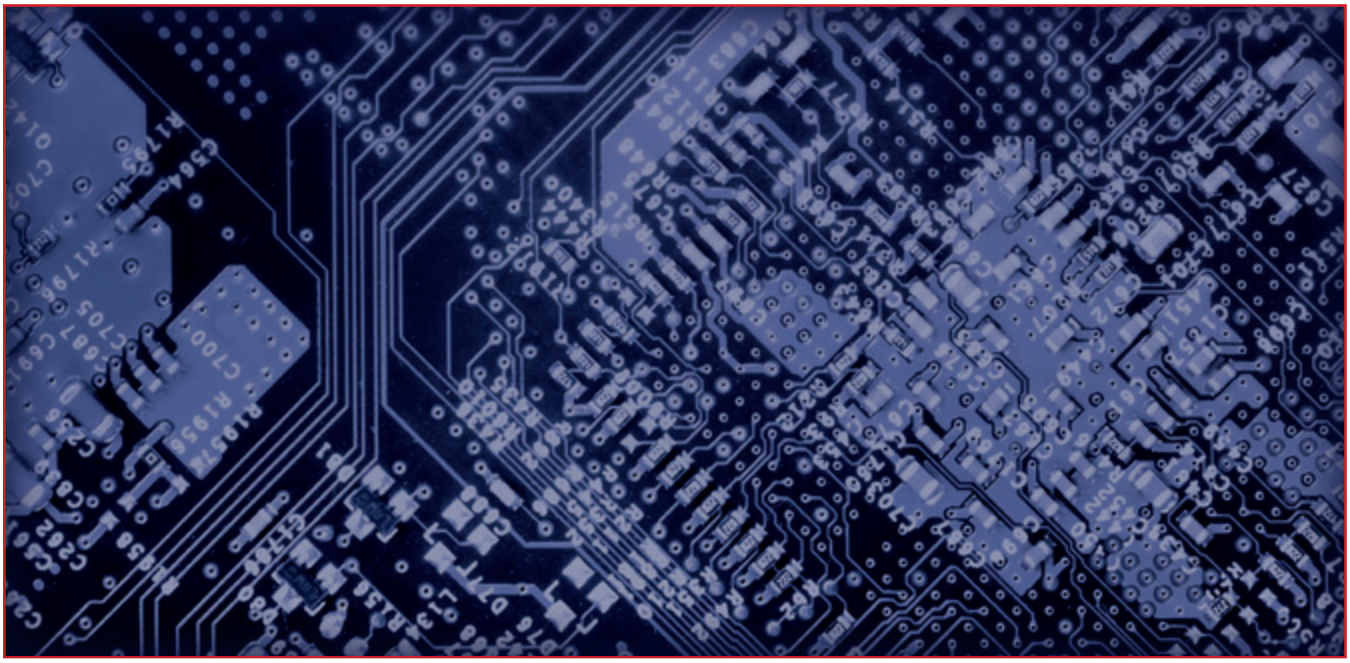

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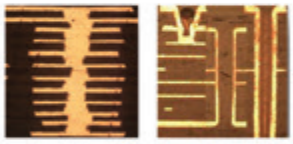
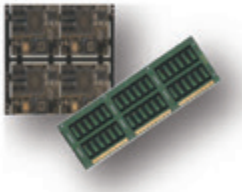
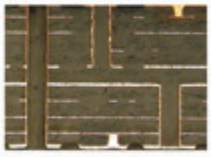
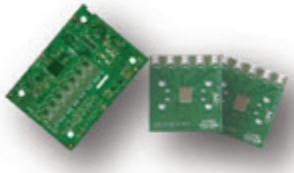


IOT / Build-up Board





Semiconductor TEST B'd
& 5G Network System



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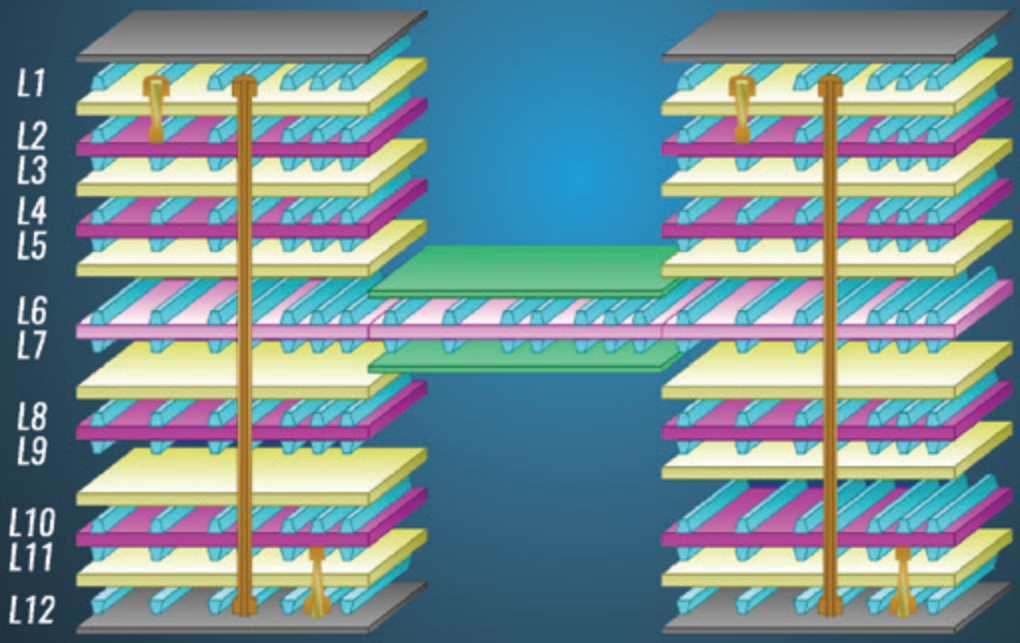


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# PRINTED CIRCUIT DESIGN & FAB CIRCUITS ASSEMBLY

## FIRST PERSON



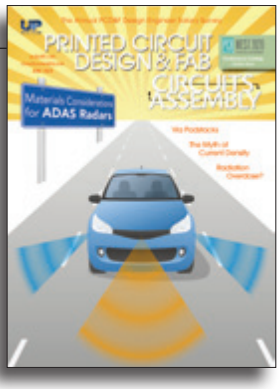
## MONEY MATTERS



## TECH TALK



## FEATURES






## IN THE DIGITAL EDITION



## DEPARTMENTS



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**EDITOR-IN-CHIEF**

# The Virtual Tour

WE'VE SPOKEN AT length in these pages about the virtual factory. But what about the virtual factory tour?

By this, I don't mean the flashy, MTV-style videos found on so many company websites today. Instead, a live plant tour, executed using cameras and PCs.

I have been studying manufacturers to determine whether, in the wake of the coronavirus surge, they are noticing changes in the way customers decide where to put production, and whether that's a permanent change or a temporary fix. According to my unscientific sample, the answers are "yes" and "we're not sure."

Count Teresa Huber, president and chief executive of Intervala, among those seeing changes. The EMS company, which has sites in Pennsylvania and New Hampshire, is substituting video conferencing for onsite meetings and in-person audits.

"We are seeing more video conferencing, and we have processes in place to share documentation on processes, give quality yield data from internal production, interface electronically," she told me. "We are definitely seeing a trend in that being the way things get done. People are getting more comfortable with the idea they may not be able to physically touch where their product is going to be made. We can reassure them through a combination of data, online conferencing, and a lot of customer references."

On SMTC's quarterly conference call, chief executive Eddie Smith said restrictions on travel and factory visits are turning tablets into voyeurs. "We can't allow people in our factories, and so the question becomes can we virtually get approvals from our customers using GoPros and iPads, in terms of the manufacturing process?"

Just prior to the Covid-19 pandemic, Joe Fama, a longtime EMS business development exec who focuses on Southeast Asia, had the same thought, albeit for different reasons. He implemented live virtual tours at a plant he worked with in Vietnam, surmising it could be a substitute for expensive and time-consuming travel.

Fama's tours run the entire factory, from the front door to the production floor. Using FaceTime broadcast via an iPad, the "escort" walks the customer through SMT, clean rooms, inventory, testing, and shipping.

According to Fama, the customers drive the process, much like an actual plant tour. "We ask them, 'Who do you want to see? What do you want to ask them?'" he told me. "The customer plans out what they want to see. We tried to get a candid, unabridged response from the line workers, and if they want, they can meet with the C-level executives and engineering too."

For those considering similar arrangements, he offers these suggestions: "To prepare, make sure the right people are available. From a housekeeping perspective, have the plant in reasonable order, with no debris or confidential materials in the line of site."

Fama draws a distinction between an in-plant visit and its virtual cousin. The in-person audit is more formal, he says, with much more introductions. Virtual, he adds, "is more like an unrehearsed, spur-of-the-moment walkthrough."

"It's an all-day process," he says, but it works well. He says they landed all four prospects that went on the virtual tours yet had not visited the plant in person. One went right into tooling just after the virtual tour, he added.

It remains to be seen whether the changes will be longer term or whether we will go back to normal, whatever normal may be, at some point. "We've all had to adapt and rethink and figure out creative ways to get things done in a very different way," Huber notes.

"Customers who are auditing and making decisions are much more comfortable if they can walk in a factory and talk to people and see it, feel it.

Another multinational EMS with plants in the US and Mexico I spoke with said some customers are deciding to source sight-unseen. They added that others he spoke with said they could see the value of a virtual tour, but if the product is really complex, they probably want to see who they are sourcing it to.

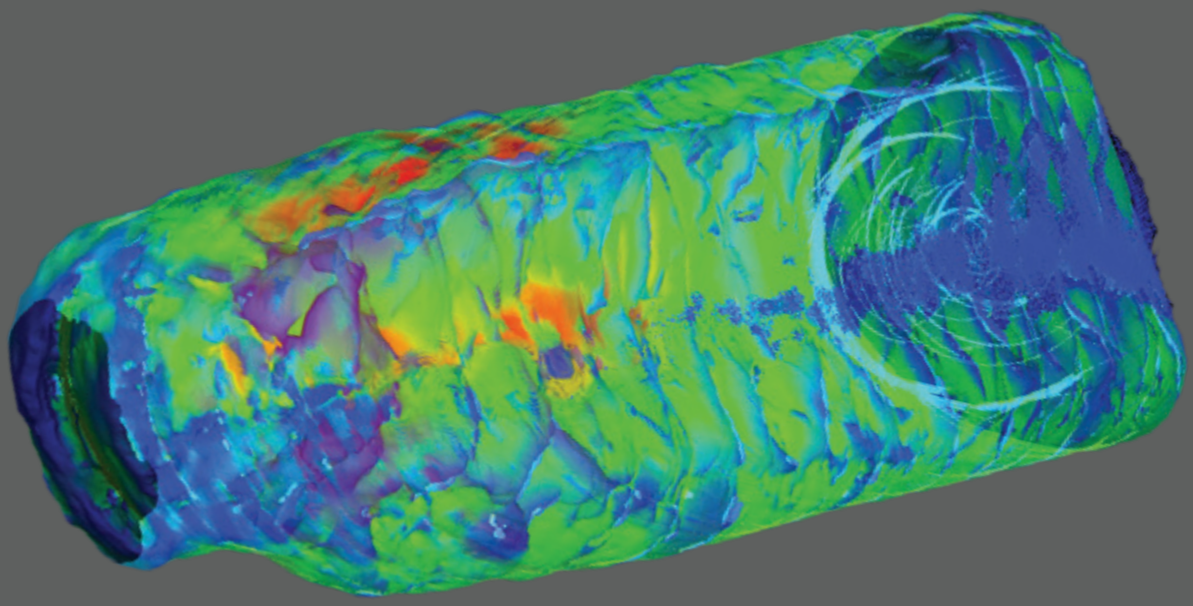
Because the line layout tends to be linear and the factories open, assembly lends itself to virtual tours. Board fabricators might be more complex, especially in the West, where job shops prevail. Still, the fabricators I spoke with felt the concept had some merit.

The overwhelming sense I get is backlogs are firm and business is continuing despite the pandemic. If going virtual can keep the sales process running smoothly, manufacturers should consider it.

mbuetow@upmediagroup.com
@mikebuetow

P.S. The show must go on! Check out the PCB West show catalog at pcbwest.com or in the digital version of this issue.

# Datest's Imaging Technology Illuminates Fossils.



This is a fossil.

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## PCDF People

Collins Aerospace named **Jennifer Waskow** director of engineering systems.

**Karl Dietz**, a PCB materials expert who spent more than 40 years at DuPont Electronics Materials, passed on May 5.

Galaxy Circuits named **Carl Schlemmer** director.

Google awarded a $43,000 grant to a professor of electrical engineering at Missouri University of Science and Technology who is using machine learning to bridge the gap between PCB design theory and the requirements of more complex electronics.

Innovative Circuits promoted **Chris La Croix** to plant manager.

Murrietta Circuits appointed **Kevin McCartney** business development manager.

TE Connectivity named **Martin Bayes** fellow – corporate technology.

Ventec announced **Thomas Brämer** has joined the company as technical sales representative for Germany. He has over 30 years' technical and sales experience in PCBs with Vaas Leiterplattentechnologie, Kubatronik, CCI Eurolam, and others.

## PCDF Briefs

**Apex International** will purchase a PCB plant in Thailand in 2020, which will boost the firm's monthly production capacity 20% to 600,000 sq. m.

**Apple** is contemplating use of in-house chips for one or more of its Mac computers, moving away from its longtime supplier **Intel**.

**Averatek** named **RBP Chemical Technology** distribution partner.

**Caiz Optronics** named **ATIF Holdings** business advisor in anticipation of its entrance into the US fabrication market.

**EMA Design Automation** has partnered with **Dassault Systèmes**.

**EnviroLeach** is gearing up to bring its Canadian circuit board recycling facility to commercial-scale capacity in the next two months.

**FH Bielefeld University of Applied Sciences** purchased a **Nano Dimension** DragonFly Lights-Out Digital Manufacturing system.

**Freedom CAD Services** named **Tech Generators** representative.

## 'The Workbench of the Future': InspectAR Aims to Disrupt Debugging Process

**ST. JOHN'S, NEWFOUNDLAND** – Newfoundland may not appear to be a hotbed for PCB technology, but a team of startup engineers may change that. There, on the Eastern edge of Canada, Liam Cadigan and Darryl Day, who grew up together, were working on degrees at Memorial University, where they met fellow engineering student Matt Noseworthy and budding computer scientist Nick Warren.

The group applied for the SpaceX Hyperloop competition, the Elon Musk brainchild that challenges teams of college students to design and build high-speed pods. The Canadian team didn't win, but its second-place finish was good enough for Cadigan and Day to land jobs at another Musk startup, Neurolink.

There, the two engineers leveraged knowledge gained from the Hyperloop experience, for which they designed control boards and worked on data acquisition. Meanwhile, Noseworthy wrapped up an internship at Wind River, which led to a position there as a firmware developer. At the same time, Warren was in Silicon Valley working as an engineer at Apple.

All along, says Cadigan, they dreamed of launching their own tech company based around a more innovative PCB visualizer. As part of a capstone project, an independent research project for graduating seniors, they turned lessons from computer vision classes into a hypothesis that PCBs, as planar objects, would be well-suited to augmented reality (AR) technology. "That wound up not being true, but it was enough to get us started," he recalls.

That start turned into a method for accelerating hardware development through faster debugging tools. The novel system highlights the nets on a board and captures and shares the metadata with other engineers, regardless of the native tool environment.

In 2018, a friend of Cadigan's happened to be attending the Del Mar Electronics trade show, where he met Mihir Shah. Shah was attending on behalf of Royal Circuits, a printed circuit board fabricator with factories in Northern and Southern California owned by his father, Milan. Prior to joining his father at Royal, Shah worked as an electrical engineer designing and validating boards at Tesla and Axon. He recalls the lengthy amount of time spent bouncing from screen to screen in the lab while debugging PCBs.

Ticking off the various instruments – the functional generator multimeter, spectrum analyzer, the PCB plus breadboard, oscilloscope, power supply, and PCB schematic screen – Shah says, "You have several different screens on your bench, and they all give different pieces of information that, while all relevant, are relevant to different people in the hardware development process – whether you are a firmware engineer or an EE or a technician. If you want to translate that info to others on your team, it's just another place to make mistakes and send the wrong file. So if you send someone a test instruction to probe these pads and send back the results on the oscilloscope or the DMM (digital multimeter), you get an email with 14 attachments, and you don't know what is necessarily referencing what."

And that leads to a lot of time and re-spins – Cadigan estimates the average number is six per design – and, of course, cost. Mihir, who saw the value of this potential workbench of the future, said he was immediately interested in becoming a customer. "I wanted to be able to click one net or component and know what it was and how it was connected. I thought it could be a competitive advantage for Royal."

After getting in touch with the four Canadian engineers, Mihir suggested they all meet up when the team was down in the Bay Area to interview with Y Combinator, the startup accelerator known for giving companies like Airbnb, DoorDash and Dropbox their start. In November 2018, YC passed, but according to Cadigan, just reaching the interview stage with a functional demo was validation they were on the right track.

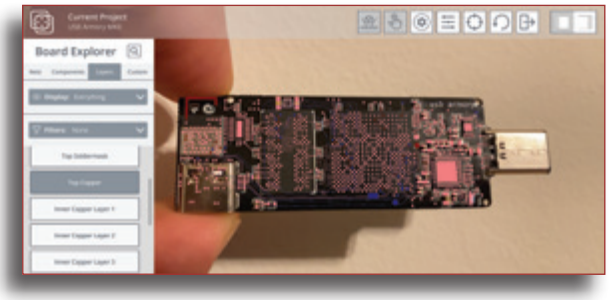
During that same trip, the guys met with Mihir and Milan Shah. Mihir could not stop talking about how impactful and exciting that first meeting was. "We loved these guys. They were earnest, smart, and ready to build something great. My dad loved them. We decided to invest. We could guide them and introduce them to our customers."

The first full system was rolled out in March 2019, and a few months later Mihir Shah joined as chief executive to help build the business and develop a strategy beyond the product itself. Royal Circuit Solutions and Advanced Assembly backed the venture with a reported $850,000 equity investment.

Now called InspectAR Augmented Interfaces, the startup rounded out its vision. The strategy quickly evolved, the founders agree. "We first thought of overlaying designs directly onto the board as an incredible feat that would serve as the ultimate EE product," says Shah, "which is still the guiding principle. Though, as we started developing our product roadmap, we knew it would go way beyond that."

"We realized there was all these time savings," says Cadigan. "It could be a platform where people delegate work, where they need technicians or other people to help. There were so many remote collaboration possibilities. This became even clearer with Covid. You can walk someone through a design much faster. We didn't see that at first."

The InspectAR system can highlight any net, layer or component data on the board without accessing the related native files from the CAD tool directly, Shah says. "It's more intuitive to know where each signal goes. You know what each pin is, no matter which tool you use. And you get all the metadata in one place: pinouts, component datasheets, values, connected nets, and component locations." Overlays for innerlayers use a different color to highlight a trace from L1 to L4, for instance. "With InspectAR," Shah continues, "now, if I have a problem with an IC, I could call the vendor, and they could pour it into my lab. 'Try this; probe that,' and do it in minutes instead of days. It's tele-engineering." While Shah emphasizes the "most important element" is the ability to eliminate the need to constantly switch between printed schematics, EDA tools, loose components, and the board, the coronavirus pandemic brings the full potential of InspectAR into clear view. "Say production is in China, but the engineer can't go over there, so they put InspectAR up, where everyone onsite can view it, and a remote collaborator can join the session and help resolve an issue.




The InspectAR software highlights nets and pulls up pin, component and other data, regardless of the ECAD system.

"Some folks do this kind of probing on Zoom, but it's hard to show what is being highlighted. Using InspectAR, it could be like you are sitting next to them in the lab. You can walk them through what you need to do. With Covid, the application of bringing contextual information into a single place is very exciting."

The InspectAR platform comes in various versions. A free single-user version is designed for hobbyists, and those who want to quickly get a feel for the technology. Users can get value out of inspectAR for free, with a library of "sponsored" boards from Digi-Key, Crowd Supply, SparkFun and more. With 2.0 coming out, the free version will also allow users to create projects for their custom PCBs designed in KiCAD and Eagle. At the professional level, a pay-per-project version has a small yearly fee for the engineering tool. Professional users can also take advantage of desktop support (PC and Mac), along with support for more file formats (e.g., IPC-2581B from Altium and Cadence) and extended collaboration features. For a larger fee, the firm will build an on-device local version for onsite use for enterprise customers.

More than 1,000 users have signed up for the free tool and are enterprise customers in just a few months of being live, in all end-markets: military, aerospace, and so on.

"In two years, we want a larger free user base, and a good percentage converted to using the tool in some kind of professional capacity, whether a single engineer or

**Luminovo**, an AI and machine-learning startup, has raised more than €2 million in pre-seed financing to support its goal to redefine how PCBs are brought from concept to market.

**Nano Dimension** named **Accelonix** agent for the French market.

**Safari Circuits** selected a **CheckSum** ILS test system.

**Technica USA** named **TCT Circuit Supply** sales representative of EMC products.

**Wise** signed an agreement to use **Plasmatreat's** Openair-Plasma in its new Wonderwise 220 surface prep machine.

## CA People

ASYS named **Bob Drake** Southeast regional sales manager.

Bright Machines named **Steve Heinzen** business development director. He spent the previous 20 years in sales and marketing leadership roles at Neo Tech, Tandon Group and Flex.

Europlacer named **John Perrotta** president, global sales and services. He was president of Europlacer Americas for six years and has more than 30 years in SMT equipment sales.

Inovar hired **Jeremy Grubb** as vice president of quality. He spent the past 12 years at L3Harris in supply chain, operations, quality and, most recently, was director of supplier quality.

Libra Industries promoted **Mike Lynch** to director of quality assurance. He has been with Libra for more than 12 years.

Nordson announced **Joseph P. Kelley** as chief financial officer.

Specialty Coating Systems promoted **Tim Bender** (left, top) to president and CEO, replacing the retiring **Terry Bush** (bottom). Bender was named head of marketing in 2003 and joined the executive leadership team as vice president of sales and marketing in 2006.

VJ Electronix appointed **Mark Clemons** general manager. Former GM **Don Naugler** becomes director of technology.

WPG Americas named **Jacqi Chase** business development specialist. She spent 16 years as director of marketing for Sunburst EMS.

## CA Briefs

**3CEMS** added a **Koh Young** KY8030 3-D SPI.

**AIM Solder** named **GR SYS Equipamentos Industriais** distributor in Brazil.

**Cognex** named **Creative Electron** as a Partner System Integrator (PSI).

The **ECIA** said US export restrictions on many technologies to China, Russia, and Venezuela are "exceedingly broad" and have the potential for unintended consequences.

Japanese component suppliers are asking a US court to toss an antitrust suit filed by **Flex**, saying that it should be handled in arbitration.

**Foxconn** plans to build a joint IC packaging and testing plant in Qingdao, Shandong Province, China, as part of the company's efforts to enter the semiconductor industry.

**IEC Electronics** expects to finish construction on its new state-of-the-art electronics assembly plant this summer.

**Integrated Test Corp.** selected a **Mirtec** MV-7U Omni 3-D AOI.

**Intervala** acquired EMS provider **Princeton Technology** for an undisclosed sum.

**IPC** seeks papers for the High Reliability Cleaning and Conformal Coating Conference taking place Nov. 4–5.

**Javad EMS** installed a **VJ Electronix Summit** 1800i rework system.

**Kurtz Ersa** is offering **Interflux's** SelectIF 2040 and PacIFic 2009M VOC-free fluxes.

**Rochester Institute of Technology** recently installed a **Mirtec** MV-3 Omni AOI machine in its Center for Electronics Manufacturing and Assembly.

**Spectra-Tech** acquired five **Mirtec** MV-6 Omni 3-D AOI systems.

**Synapse Electronique** installed two **Universal Instruments** Fuzion Platform production lines in its Shawinigan, Quebec, EMS facility.

**Variosystems** acquired **Solve Engineering** for an undisclosed sum.

in a group," Cadigan says, outlining the company goals.

Currently it works with CAD tools from Altium, Autodesk Eagle, Cadence, and Kicad, and integrates with distributors like Digi-Key and Mouser. InspectAR is also adding integration with different lab tools, like an oscilloscope that connects to WiFi. "If that can be connected to the tool, it will be more powerful," Cadigan says.

InspectAR plans to launch rev. 2.0 of its signature product in about a month. The next revision performs 3-D object tracking, rotations to enable 3-D viewing at more angles, and scanning calibration. Another feature is new parsing technology. The bill of materials parser receives the component datasheets live, Shah explains. "For on-device users, we can integrate local PLM and custom BoMs." A web connection is required for users who want this in real-time, although InspectAR is working with major parts distributors on caching, so the data will be present longer.

Other potential developments: smart work orders that communicate electronics knowledge bidirectionally, enabling interactive AR guides that can be distributed to individuals. "You can track that documentation and put it into your management software to make it useful for teams," Shah notes. An ECAD-agnostic mobile version could allow users phone access for viewing and determining a feature or a net without opening a PC.

In the meantime, the staff numbers 11 and is expected to double in 12 to 18 months. Shah is part of Autodesk's Technology Center program in San Francisco, while the rest of the staff is in Newfoundland. The team seeks sales staff, more software developers and "anyone who is excited about making augmented reality software for PCBs," says Cadigan, now chief product officer. (Day has become CTO, Noseworthy CIO and Warren COO.)

Asked whether the company will ultimately relocate to the Silicon Valley, Shah dismisses the idea. Sharing a photo of the company's idyllic workspace in St. John's – a wall of glass overlooking the waters of the Atlantic – he says the combination of location, engineering talent and relatively low overhead makes Newfoundland the perfect place to build the workbench of the future. (MB)

## NCAB Buys Bare Board Group

**BROMMA, SWEDEN** – NCAB Group signed an agreement to acquire 100% of the shares in Bare Board Group for $12 million. BBG had revenue of approximately $30 million in 2019.

"We are very happy to join forces with BBG," said Martin Magnusson, president of NCAB Group USA. "NCAB Group USA and BBG together will take on a leading position in the US PCB market. This brings additional value to our North American segment, with increased ability to offer our customers superior quality and service, as well as more volumes to our existing factories. BBG's supply chain management and factories are mainly located in Taiwan, which is a great supplement to our existing factory base and allows for more options in order to satisfy our customers' PCB demands in the future. We have the same value-driven organization and the same focus on giving our customers excellent quality and service." (CD)

## Creation Technologies Acquires ATS

**BOSTON** – Creation Technologies acquired Applied Technical Services, expanding Creation's manufacturing facilities and design centers operating across the US, Canada, Mexico, and China. No financial terms were disclosed.

"We are investing to broaden our capabilities and reach with the addition of the ATS team, who share our values of providing exceptional customer service and outstanding quality," said Stephen P. DeFalco, chairman and CEO, Creation Technologies.

The acquisition expands Creation's capabilities in the aerospace and defense, medical, and tech industrial markets. It adds locations in Everett, WA, and Hermosillo, Mexico, each offering three automated SMT lines, as well as automated through-hole, ICT, flying probe, and functional test capabilities. (CD)

**METALS INDEX**


**WATCHING THE FALL?**

| US electronics equipment shipments | % CHANGE JAN. | FEB. | MAR. | YTD% |
|---|---|---|---|---|
| Computers and electronics products | -0.1 | 0.3 | -0.2 | 1.6 |
| Computers | 3.8 | 0.0 | -2.6 | -14.5 |
| Storage devices | 9.0 | -1.4 | -4.4 | 32.8 |
| Other peripheral equipment | 2.8 | -1.2 | -0.4 | 9.6 |
| Nondefense communications equipment | -1.4 | -0.4 | 2.3 | 6.0 |
| Defense communications equipment | -17.2 | 4.2 | 3.7 | -9.4 |
| A/V equipment | -10.0 | -4.5 | -13.4 | -31.1 |
| Components[1] | 1.7 | -0.3 | -1.5 | 9.0 |
| Nondefense search and navigation equipment | 0.5 | -3.9 | -2.9 | -3.9 |
| Defense search and navigation equipment | -0.5 | -0.2 | 0.2 | 3.7 |
| Medical, measurement and control | 0.9 | -0.9 | 0.7 | -2.2 |

[r]Revised. *Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: U.S. Department of Commerce Census Bureau, May 4, 2020

**US MANUFACTURING INDICES**

| | DEC. | JAN. | FEB. | MAR. | APR. |
|---|---|---|---|---|---|
| PMI | 47.8 | 50.9 | 50.1 | 49.1 | 41.5 |
| New orders | 47.6 | 52.0 | 49.8 | 42.2 | 27.1 |
| Production | 44.8 | 54.3 | 50.3 | 47.7 | 27.5 |
| Inventories | 49.2 | 48.8 | 46.5 | 46.9 | 49.7 |
| Customer inventories | 41.1 | 43.8 | 41.8 | 43.4 | 48.8 |
| Backlogs | 43.3 | 45.7 | 50.3 | 45.9 | 37.8 |

Source: Institute for Supply Management, May 1, 2020

**KEY COMPONENTS**

| | NOV. | DEC. | JAN. | FEB. | MAR. |
|---|---|---|---|---|---|
| Semiconductor equipment billings[1] | 9.1%[r] | 17.8%[p] | 22.7% | 26.6% | 20.1% |
| Semiconductors[2] | -10.7% | -5.4% | -0.35% | 5%[r] | 6.9%[p] |
| PCBs[3] (North America) | 1.08 | 1.09 | 1.05 | 1.15 | 1.15 |
| Computers/electronic products[4] | 5.50 | 5.47 | 5.45 | 5.49[r] | 5.49[p] |

Sources: [1]SEMI, [2]SIA (3-month moving average growth), [3]IPC, [4]Census Bureau, [p]preliminary, [r]revised

# Hot Takes

- **Worldwide IC unit shipments** will fall 4% this year, the first-ever back-to-back annual decline. And the overall memory market is expected to be flat. (IC Insights)
- **Advanced packaging** for data center servers, AI accelerators, and 5G infrastructure is a potential growth area in 2020. (TechSearch International)
- **Semiconductor sales** totaled $104.6 billion during the first quarter, up 6.9% from 2019. (SIA)
- **Tablet shipments** fell 20% year-over-year to 24.6 million units during the first quarter. (IDC)
- **Electronics** now account for 40% of the cost of a new vehicle. (Deloitte)
- **Taiwanese** manufacturers said **orders for electronic products** in March increased 24%, compared to the same period last year. (Taiwan Department of Statistics)
- Nine **EMS transactions** took place in Q1. (Lincoln International)
- **The smartphone output** this year will slump 11.3% to 1.24 billion units. (TrendForce)
- **Global PCB end-use demand** was down 4.6% in 2019, and PCB output was $68.3 billion, down 1.2% year-over-year. (TPCA)
- **Worldwide PC shipments** fell 8% year-over-year in the first quarter, the largest quarterly drop since 2016. (Canalys)
- **Most US firms in China** currently have no plans to relocate production to other parts of the country or abroad due to the coronavirus, but there is less certainty about the long term due to growing worries over US-China. (Pricewaterhouse Coopers)
- **The global electronics adhesives market** is projected to reach around $14 billion by the end of 2027, growing at CAGR of 12.1% from 2020 to 2027. (CMI)
- Some 90% of **component manufacturer** representatives expect Covid to have a "serious to severe" impact on their business during the next two to three months. (ECIA)

# I Forgot a Work File. Will DFARS Mind if Someone Emails It to Me?

Working from home brings many Covid epiphanies.

AS I RELUCTANTLY get used to social distancing, wearing face masks in public and continually washing my hands, many "aha!" moments have occurred. These have been about the new realities of dealing with the global disruption from Covid-19, as well as the changes we will most likely live with once we've survived the pandemic, or at least the first round of it. In no particular order, they include:

Zoom, Zoom, ZOOM! I am not tech savvy or social media conscious, so it should be no surprise that three months ago I had never heard of Zoom. I know about it now! I spend a good portion of each day, including weekends, on a Zoom "call." At first it was family trying to connect from the various places they were hunkered down. But then I began receiving requests from customers and suppliers to schedule a Zoom meeting to discuss one or another thing. Zoom enables those working remotely to participate with the few still working out of their office or factory. Zoom is user-friendly, and unlike WebEx, easier for those working at home to manage.

What I find intriguing about the use of Zoom is how those working at home can put up a background picture or just talk with a blank screen to avoid those on the Zoom from seeing their cluttered kitchen or den. It certainly reduces potential embarrassment for some who work from home. But imagine, anyone can get a picture of a world-class manufacturing plant – or process line – or shelves of "inventory" for display so viewers think *that* is their plant. Oh, the potential here is limitless!

The little things! What did you leave in your office while working at home? Passwords, fobs, files with instructions to access some web account you only need to do once in a blue moon, all of which seem to happen during the pandemic. Many folks I have spoken with have had to go into someone else's desk to grab a file or password, then scan and email it to a coworker working at home. Many customers have found it difficult to get signoffs for purchase orders, as the key person working from home does not have access to some file or software to review or approve. Ditto financial managers, who are missing just one of the two factor authorizations needed to perform a task. Working from home works well for many, but some effort is needed to make it work for all.

NIST-800-Cybersecurity, *et al!* With everyone working remotely, who cares about cybersecurity? More than one person I know is working from home using a home PC running Windows XP or Windows 7, neither of which is still supported by Microsoft. Cybersecurity no no! Surprise! They cannot access some, if not most, of their company IT databases. But not to worry, there is *always* a workaround. Some take pictures of documents with their phone and text them to a coworker, who then uploads the photos into a file/document and then emails that file to a remote coworker. Even companies with the most robust IT infrastructure and resources to set up employees to work from home on company-supplied computers are cringing when the at-home employee needs to print a document and does so on a non-secure printer or via a wireless device on their home (read: non-NIST-compliant) network.

I doubt when DFARS/NIST developed the various protocols outlined in the volumes of cybersecurity documents and requirements, they ever envisioned so many users working from remote locations. My guess is a zillion revisions to NIST-800 will be released soon. Possibly all the cellphone and cable companies will be required to comply to the NIST requirements. Can't wait to see how they accomplish that.

Cubicle, oh cubicle! The brainchild of some office architect in the 1960s, the art of the cubicle has been refined through the years. Today's office environment focuses on collaboration; the physical proximity allows us to bounce ideas off coworkers, interact with colleagues, and build a sense of camaraderie for the common, corporate good. Well, back to the drawing board! Manufacturers, service providers and commercial real estate brokers are discussing how to *separate* people, including enabling some to work from home, and others to split shifts to reduce interaction and promote social distancing.

The office of the future may look remarkably like the office of the past, with discrete offices and spread-out traditional desks that enable six feet between each employee. Equally shared workspace, where three people share a desk, but only one is in the office on a given day, may also become standard. Cafeterias or lunchrooms offer their own challenges and may need to undergo a social distancing redesign.

Shop floor elbow room! Like the office, many are looking at their manufacturing shop floor and rethinking how close process lines should be, or how to make a work "cell" appropriate for social distanc-

*continued on pg. 19*

**PETER BIGELOW**
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# Marketing and the Post-Covid 19 World

Ramp the advertising programs and support them with content tied to sales efforts.

IN MY APRIL column, I discussed the communications strategies that were most important as Covid-19 began to change our working lives. This month, I look at communications strategies that *will* be most important as we resume the new normal working world. As I write this, the strategy for reopening businesses is just being formulated. From everything I've seen reported, it appears the strategy will be a rolling relaxation of restrictions, which means geographic advantages for companies in places that either had minimal infection rates or have successfully flattened their curves. Rolling increases of restrictions are also likely if a region starts to see new spikes in infections.

From an electronics manufacturing services (EMS) provider perspective, what does that mean? First, consider what Covid-19 has done to this business sector. Many EMS providers remained operational at some level thanks to product mixes that included essential products that support infrastructure or medical needs. However, even those companies typically are working at reduced levels and have experienced employee angst about virus risk. Customers with nonessential product are in some cases cutting forecasts dramatically and in other cases will have a lot of pent-up demand. Those trends depend on whether the product is something buyers have simply been waiting out the quarantine to purchase or will likely not purchase for months after the quarantine ends. When you overlay today's trends on a post-Covid-19 world, it translates to manufacturing constraints, supply-chain constraints, plus pockets of oversupply. If a large part of the US gets back to work by May 1, it is likely that pent-up demand will continue to be a factor. If the quarantines in place in mid-April extend through May in a large part of the country, it is hard to predict what the demand landscape will look like. Datacom, industrial and medical products will likely remain strong, but consumer demand will drop dramatically.

The international picture is also a factor. While most of Asia and parts of the EU are either back to work or planning to get back to work shortly, Mexico is just starting to feel the impact of the virus, and the inefficiency of Mexico's state governments in determining essential businesses is going to impact EMS facilities. Companies with good Mexican legal counsel and strong relationships with their local maquiladora associations are likely to do better than those without those relationships. The global supply chain remains imbalanced, which means logistically that transport chains are also imbalanced. Even if a manufacturer can produce, it may not be able to get that product from point A to B as quickly as its customer needs. OEMs also cannot get their products from point A to B as quickly as their customers may need.

> "Focus social media, web, advertising or whitepaper content on how you solved supply-chain challenges."

From a marketing perspective, it becomes important to get into the mind of prospects and customers. The scenario I've just laid out has created frustration and destroyed every 2020 forecast and budget in existence. It also shows the weak spot of supply-chain consolidation. Sourcing strategies that have geographic variety are now more relevant. So, while little will change immediately, sourcing teams are likely compiling lessons learned right now and formulating new sourcing strategies. As a result, EMS marketing activities should align with the lessons-learned mentality that sourcing teams are likely to embrace. Here are my thoughts on marketing strategies most likely to work:

- Prospects that evaluated your company but elected to stay with current suppliers are low-hanging fruit. Sourcing teams aren't going be excited about jumping on planes for a few months. Consequently, companies they've already evaluated may be the first they consider if they need to shift production due to capacity constraints at their current suppliers or decide to begin moving production from China. Sales teams should build relationships by providing educational content on recent customer success stories in the areas of project transfers, mitigating supply-chain constraints or ability to support unanticipated surges in demand. Workplace infection mitigation strategies should also be highlighted. Also, determine if there is a way to support virtual facility audits, should a prospect that has previously toured want to take a next step without travel.
- LinkedIn, blogs, article placements and advertising should expand. Trade shows are going to be

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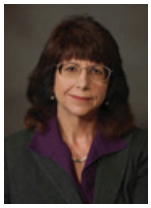

unlikely for months. Even if third-quarter trade shows are held, many companies may be restricting business travel to discretionary events, so attendance will be down. At the same time, OEMs will be reevaluating sourcing strategies. From a marketing standpoint, it is important to have strong, targeted messaging reaching as much of the market as possible. Companies with limited budgets can use social media, blogs and PR to get out that message. However, advertising is likely a good investment for the rest of the year because it acts like a road sign directing readers to your more detailed educational content.

- Messaging matters. In a stable market with little differentiation among suppliers, decisions get made on price. In a chaotic market, decisions get made based on a sourcing team's perception of which company is most likely to address the challenges their team is facing. The biggest challenges today are getting projects transferred quickly, managing supply-chain constraints, addressing spikes in demand, supporting legacy product, staying operational and addressing logistics challenges. Companies with geographically dispersed facilities and those with facilities in areas that are remote enough to have not seen infection have a competitive advantage. Companies whose social media, web, advertising or whitepaper content discusses how they have solved some or all of those challenges, or highlights the geographic resiliency of their facility locations, are going to be more competitive than those talking about capacity or equipment.
- Transparency still matters. It is still important to be honest in communications about operational constraints with employees, customers and prospects. Marketing messages shouldn't overstate a company's ability to deal with regional constraints. In situations where constraints exist, it can be helpful to discuss a company's ongoing efforts to restart production as quickly as possible. Enhance customer retention by helping them understand what is being done to negotiate reopening with local governmental authorities, how furloughed employees are being retained, what infection mitigation practices are in place in each facility and how project recovery activities will be handled. In the absence of information, sourcing teams will develop their own recovery plans.

Covid-19 has caused massive disruption around the world. However, chaos always opens the door to opportunity for those who look for it. Start planning and executing post-Covid-19 marketing strategies. This will be an educated sell that requires content that addresses how an EMS provider is going to solve common challenges. Consequently, marketing programs that work will have detailed content backing up whatever advertising is done and strong linkage to sales efforts. ▫

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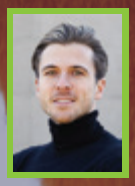

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# The PCB Podcast

# Your PCB Supplier Was Acquired. What Now?

Understand what the transaction means for customers.

YOUR PCB SUPPLIER has been acquired. Will this acquisition benefit you as a board buyer? Or will it lead to higher prices and a reduced level of service?

The answer may depend on how you react.

Vendor acquisitions can cause supply-chain disruptions, especially when the acquiring firm has a competing product line. Few PCB buyers seem to understand the real economics involved, or why they happened in the first place and what it means to them as customers.

Acquisitions usually fall into two categories: Either the acquiring firm buys the present customer base and its revenue stream, or it acquires some leading-edge or dissimilar technology of the acquired supplier – like a rigid supplier acquiring a flex manufacturer, for example. Either way, the goal of the acquiring firm is to catapult its sales efforts.

Interestingly, PCB suppliers that both manufacture and broker – whether in the US or abroad – may build boards for one another *and* broker from each other. Many board buyers don't realize how much overlap there is among manufacturers.

And that means, more than likely, when a similar supplier buys another, the acquisition is an attempt to grab a greater share of the market, rather than to accelerate an innovation strategy.

For the customer, the question is will they benefit? In practice, the relationship with the supplier and the level of service received is likely to change. What should you do to protect your business?

*You* should oversee your supply chain, not your supplier. While you may not notice changes in your relationship with the acquired vendor right away, take a close look at your PCB purchasing process. Don't wait to be visited by the new supplier team, especially if the acquired firm was a big part of your PCB spend. Request a meeting sooner rather than later. Pay attention to how receptive the new supplier is to the meeting and be ready to ask many questions to get the lay of the land.

Try to ascertain where your orders stand with the larger entity. What often happens when a larger supplier swallows a smaller competitor that builds similar product is customers immediately become smaller fish in a bigger pond. What was 5% before may now be only 0.5%. Ask the new entity what percentage your sales represent for them. Bigger is better.

Will you still be considered a target account for the larger vendor? Will the potential for superior PCB buying power of the large entity offset your company's (potentially) reduced significance?

Realistically, you will have less leverage on pricing and service. In fact, the newly enlarged supplier may even raise prices to politely shed customers no longer seen as desirable.

Plan on personnel changes happening after a merger, so ask now how the new vendor intends to ensure a smooth customer service transition. The support staff you've worked with for years may be laid off to avoid duplication of costly services. The supplier's sales representatives may now operate under a different incentive structure that makes their relationship with you less important. Or sales reps may be let go.

Review any written agreements you have with the supplier and those with your customers. Do they contain a clause about changing possible subcontractors? Once a supplier is acquired, the new company is likely to try to move your business to PCB manufacturing locations that support *its* business operations, not necessarily to those best for your orders. Because of your customers' specific requirements, let the new vendor know which orders can't be moved and get it in writing that they will comply.

Also, update and review whether the new entity can maintain the nondisclosure (NDA), hold harmless, and service level agreements you require. Are payment terms the same? Delivery times? What about the RMA process? Does the new entity have a different warranty policy? Who is in charge of quality? And be sure to give them a copy of your most recent PCB fabrication spec. (If you don't have a fab spec, make it a priority to create one.)

In addition, develop a Plan B, especially if both vendors were supplying your company PCBs prior to the acquisition. Instead of two companies competing for your orders, you now have only one vendor who may not be as motivated to remain price-sensitive on your PCB orders.

Reach out to alternative PCB vendors for quotes, as they may be eager to give you price breaks and offer you a higher level of service, regardless of your annual PCB buy. At the very least, having an alternate source for your PCBs gives you more leverage with your new, larger vendor.

If the acquisition experience is not a good one for your company, cut the supplier loose by slowly migrating business elsewhere. Seek out other manufacturers. You can also bypass the broker altogether and deal directly with offshore manufacturers. That is now easier than ever before.

Either way, being prepared now will protect your PCB purchasing in the future. ❑

**GREG PAPANDREW** has more than 25 years' experience selling PCBs directly for various fabricators and as founder of a leading distributor. He is cofounder of Better Board Buying; greg@boardbuying.com.

# The Nuts and Bolts of a Via Padstack

Or why aspect ratio rules all.

**JOHN BURKHERT JR.** is a career PCB designer experienced in military, telecom, consumer hardware and, lately, the automotive industry. Originally, he was an RF specialist, but is compelled to flip the bit now and then to fill the need for high-speed digital design. He enjoys playing bass and racing bikes when he's not writing about or performing PCB layout. His column is produced by Cadence Design Systems and runs monthly.

THE HUMBLE VIA comes in many flavors. By connecting one layer of a conductor pattern to another, vias have connected the world. My career has depended on them as part of the hardware I used to design for others to use. A foundational innovation in electronics brought plated through-holes to the masses. As a leap forward from wire-wrap technology, multilayer printed circuit boards put a "mainframe" in each of our pockets almost overnight.

From the first plated through-hole to the latest, the trend is to support higher-density interconnect. The key driver in plating holes is the aspect ratio, the hole's width relative to its depth. For a through-hole, the depth is the thickness of the PCB. Most reputable fabricators can handle a 10:1 ratio, such that a common 0.062" board thickness will require a minimum finished hole size 0.006" (**FIGURE 1**).

Finished hole size is just what it says on the tin. The initial drill will be one- or two-thousandths of an inch larger than the finished size to account for the thickness in the copper "barrel." The barrel is created by drilling through-holes and electroplating the top and bottom of the board prior to etching away the circuit pattern. There are two complete sheets of copper of a starting thickness. As those are plated up, the prepared holes get their plating. That is all the copper that is added to form the barrel. Other protective layers come later.

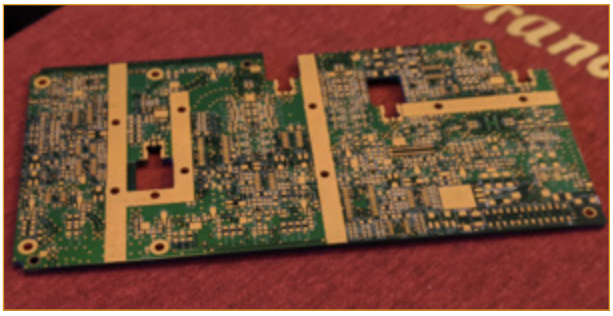

**FIGURE 1.** Ten layers of technology.

The point is the optimum amount of barrel wall thickness depends on the outer layer geometry of the PCB. Trace width and especially airgap depend heavily on the thickness of the copper on the outer layers. Most of the time, there is a different set of rules for inner- vs. outer layers in terms of trace width and space. Up to a point, a larger hole will be easier to plate. As the smaller holes approach maximum aspect ratio, the plating must be more aggressive. Pressing on the factory capabilities inevitably leads to more X-outs. As yield drops, unit prices rise.

If board density permits, a 0.013" hole with a 0.25" capture pad is the sweet spot for low-cost PCBs. This would have good current capacity but could be too much a discontinuity for a high-speed link. In that case, a 0.008" finished hole through a 0.018" pad is a good compromise and a go-to size for most plated through-hole designs. While inches were used, for the most part expect the metric system to apply.

With a solid via plan, the user can influence what to do when a via is not connected on a layer. I've been told a plated pad on the no-connect layer could expose the signal to magnetic coupling when the vias share an opening in the ground plane. I've also been told the extra annular ring helps anchor the via's barrel. That little extra copper that became the barrel could use those the same way a 55-gal. barrel has ridges. (I write gallons because "208.198 liters?")

Live a little. When a layout can afford to spread out on the top layer, it is a chance to get to a useful routing grid. Consider the number of channels that will route between each via. While it is tempting to pair each via to the SMD pad, optimizing the fan-out at the device can help at the connector end. A row of vias will create a slot in the ground plane. Those who simulate circuits like that are apt to provide some guidance if you ask. If not them, then the Federal Communications Commission might like a word.

Typically, the start and endpoint vias are the only ones you get with a high-speed bus. Slick fan-out will uncross P/N disagreements and get each member to an agreeable latitude to route to the receiver pin. Space around the signal via can become a coax in the z-axis by surrounding the via with three ground vias. This extreme care is normal when dealing with RF. Data rates of 2.5Gb/s deserve that kind of care as well. We want to avoid vias, but if we're doing them, we're doing them right.

Blind, buried, microvias — now what? Freedom from the tyranny of through-hole PCBs happened (to me) around the turn of the century. Optical gear in the 10Gb/s space was competitive and constrained by

*continued on pg. 19*

# PCB Design Starts with the Materials, but Choosing is Tougher than Ever

A call for performance-centric materials specifications.

THE COMBINATION OF rising performance expectations and intense commercial pressures means choosing the right substrate materials for new-product designs is more important than ever. A wider selection of materials, with more finely nuanced properties, increasingly complicates making the "right" choice. Help is available from suppliers and industry bodies. But designers can also help themselves by being more willing to share information with their suppliers.

As PCB industry veterans, we know well the board is typically the last part of the project specified when a new product is designed. On the other hand, it's the first item needed when serious development begins. Designing the circuitry to go on the PCB obviously gets most of the attention, but the substrate itself is usually the lowest priority in engineers' minds. When the time finally comes to consider it, teams will often simply default to the same materials used previously. As performance demands imposed on successive product generations continue to intensify, and factors such as conductive anodic filament (CAF) formation that seriously affect reliability become more critical, this approach is increasingly unsatisfactory.

As the industry has come to understand more about how the substrate properties influence performance and reliability under various operating conditions, so the number and diversity of material types available has increased. In the past there were only a handful of options open to designers. Today, international specifications offer over 100 different material categories to choose from. Designers, understandably, struggle to connect the specifications with the properties sought. It doesn't help that these specifications are usually based on chemical composition. As the breadth of choice on offer continues to increase, it's almost impossible for electronics engineers to relate to them. I have been calling for some time for the industry to move to performance-centric specifications that are easier for engineering communities to interpret.

Getting help is essential, because struggling alone risks underspecifying or overspecifying the material for the application at hand. Neither is good: underspecifying risks the product coming up short in a way that could be beyond any realistic remedy. Overspecifying, to be "on the safe side," can be commercially disastrous in ultra-competitive markets such as consumer technology. The chosen materials also need to be readily available in any location globally where the product is to be manufactured. Some resins, for example, are only available in certain domestic markets and are difficult to procure elsewhere.

So, what to do? Qualifying or testing materials helps to understand their performance and properties but is expensive and time-consuming for companies to undertake independently. Pooled testing, where groups of companies get together to do specific tests and share the results, is one response. Also, the HDP User Group (hdpug.org) has several active programs including the Lead-Free PWB Materials Reliability project, which is currently in phase 6. I have run various phases of this project. It benefits from pan-industry participation and has established a comprehensive set of analyses that cover Dk and Df, CAF, thermal stress, and other tests on standardized test coupons. Ventec has contributed several materials to this program, including one of the materials in the latest phase 6 tests.

Designers can also take advantage of another emerging trend among suppliers, which is to present carefully curated sets of materials for specific application areas. Our material guides, for example, bring together products with properties suitable for automotive or aerospace and further subdivide them according to target applications and operating environments, such as under-the-hood or in-cabin. In this way, suppliers effectively contribute their expertise to help customers short-list products that can meet their requirements. This helps by simplifying and accelerating selection, narrowing the focus to materials that are fundamentally suitable.

Helpful though this is, as suppliers we often need designers to express their requirements directly if we are to provide the right material for the right task. During my time in the industry, I have been involved in a few cases where large OEMs have been too sparing with information, particularly about the intended application and operating environment, and ultimately were obliged to recall large numbers of units from the field. With just a little more willingness to share information, the problem could have been avoided, rather than remedied at high financial and reputational cost.

While it's understandable for any OEM to be wary of sharing information about its IP and product strategies, cases like these highlight the value of trust between OEMs and their suppliers. I have called before for greater openness and trust. As materials selection becomes more complex and, at the same time, more important to get right the first time, there is more to gain by finding ways to be open and more to lose by keeping traditional barriers in place. □

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# Can Rigid-Flex Have Different Layer Counts in Different Areas?

Yes, but there are performance and cost tradeoffs.

YOU HAVE STARTED a new design. The chassis is defined, and you are thinking about how everything could be connected. Unlike the past, you are thinking about the interconnect strategy early in the design process, rather than at the last minute. Now you must decide what will be connected as an integrated rigid-flex and what might need to be done separately. So many design options are available right now. Here is where the question comes up: What if my layer counts are not consistent everywhere?

When faced with this, don't worry. Rigid-flex allows us to design in almost any configuration. Each has performance and cost tradeoffs. Let's review few of the more common design styles.

Combo board. This design joins two processor boards. However, the left board has more functionality and therefore requires more layers. What to do? You could make the left board 14 layers and the right board eight layers, as you may think that would save money (**FIGURE 1**). That is not the case, however. In fact, it is *more* expensive to leave it as 14 layers on one side and eight layers on the other. This is because circuits are built in a panel format, and the material for all 14 layers exists in all areas. Tooling is developed to remove material where it isn't wanted. Thus, you pay for all the material and then pay to have it selectively removed. In addition, the eight-layer side needs to be drilled and plated first. Then the rest of the 14 layers get added, drilled and plated again. This means paying for double processing. To avoid this cost, we recommend both boards have all the material for 14 layers. If the layers aren't needed, add nonfunctional pads or extra planes. Who doesn't like another ground plane?

The octopus. Maybe you have a design with a main processor/backplane board, with arms coming off in many directions (**FIGURE 2**). The main board has 12 layers. There are flex arms, each with flex layers terminating at an I/O connector end. At these ends, you only need four to six layers to pin it out. You might stop there, thinking it will be lower cost if no material is added where it is not needed. Again, it is cheaper to leave the extra material there.

Sometimes, however, you may have a constraint. In some cases, there is not enough space in the box. Alternatively, maybe the connector you need only comes with shorter pins. If that is the case, you may need to reduce the layer count. Don't fear. It can be done; it just takes extra processing. Your supplier can help you with the design to minimize cost impacts.

The overlapper. In this type of design, multiple flexes need to exit the main board in the same x-y plane (**FIGURE 3**). Their terminations overlap or sit on top of each other in a staggered fashion.

This is a bit more complex, and there is no way to make all the rigid ends the same. In this type of design, the main portion of the board needs at least two more layers than the two rigid tails combined. This is because this type of board is constructed as two separate boards: one for the top and one for the bottom tail. Then, they are laminated together between additional rigid layers. These additional rigid layers serve two purposes. First, they provide for additional routing in the main board to connect top and bottom. Second, that material creates a pouch around the previously fabricated tail ends to protect them for the remainder of the circuit fabrication. In

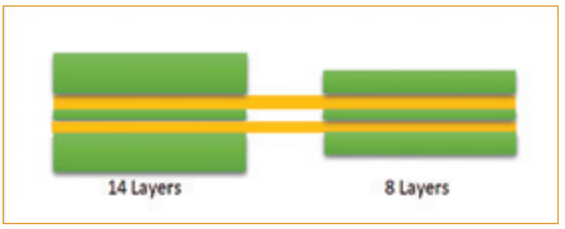


**FIGURE 1.** The combo design varies the number of layers in each board.

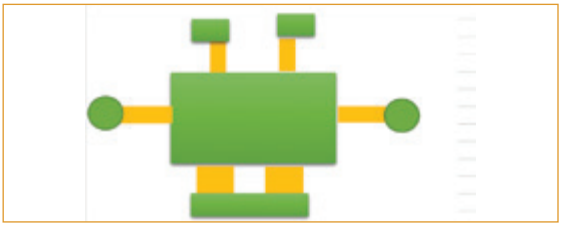

**FIGURE 2.** A board with arms coming off in many directions, like an octopus, is less expensive to build if any extra material is left intact.

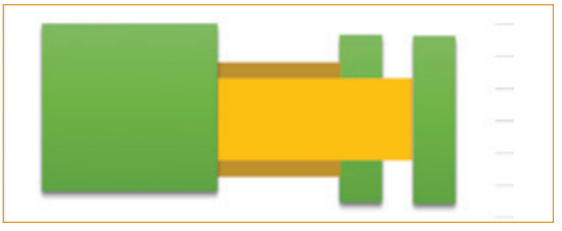

**FIGURE 3.** If multiple flexes need to exit the main board in the same x-y plane, the main portion of the board needs at least two more layers than the two rigid tails combined.

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this case, we must have more layers at the main board than we have at the tails. In these types of designs, ENIG is a preferred final finish, rather than solder.

There is a way around this if you revisit how you get from point A to point B. If you have space, you can jog one of the flexes around the rigid section of the shorter tail, and then back down to your longer termination end (**FIGURE 4**). In this way, all three rigid boards have the same layer count. This significantly reduces material and process cost. It also eases assembly.

Several variants on this exist where the flexes may need to overlap but terminate in different areas. Provided the rigid ends terminate with the same material sets, the impact to the unit cost can be managed.

All these options can be achieved, but each comes with a distinct cost. Select a design that gives all the connectivity you need without incurring unnecessary premiums.

**FIGURE 4.** By routing one of the flexes around the rigid section of the shorter tail, all three rigid sections can be the same layer count.

Once again, congratulations for thinking about the circuit options early in the design phase. This is where you can get the most performance and functionality and the lowest cost. Remember less is not always better. □

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*ROI, continued from pg. 12*

ing. Firms are looking at redeploying staff to second or third shifts to reduce the number of people in close quarters. At least one manufacturing engineer I know has been tasked with redesigning the manufacturing operation so people can be six feet or more apart. He claims that will be a colossal logistical endeavor based on the size and complexity of equipment to be moved. Others are talking about plexiglass "walls" between machines, much like can be seen today at grocers, to separate people. Like the office, the shop floor will look different and may expand as social distancing requires.

The past few months have impacted everyone. However, it looks more and more like the impact is just beginning, and we all need to rethink how we do business, from where, and how close to our coworkers. The lasting change from Covid-19 may not be how many contract the disease, but how we all recalibrate our day-to-day life at home and at work going forward. □

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*Designer's Notebook, continued from pg. 16*

form factor. Chromatic dispersion along the fiber was a problem the company was solving using a 0.5mm pitch device. This is the point where the usual via can't help.

The beauty of a microvia (**FIGURE 2**) is it can be used within the SMD pad. Precious space that would be taken by fan-out vias can be used for more components. Via-in-pad technology is mainstream for RF and digital alike. Shorter inductive loops are possible for the decoupling capacitors using via-in-pad technology. Using a finish of ENIG (electroless nickel immersion gold) is common because it improves flatness. A flat pad provides a more consistent solder joint. Power devices, or anything with a ground pad, benefit from microvia-in-pad solutions.

It comes back to the aspect ratio. A via made by a laser must be wider than it is deep. That means the dielectric must be thinner to make a useful via size. HDI (high-density interconnect) is defined by this process. In today's world, a PCB designer will do well to master the intricacies of microelectronics. There will always be through-hole applications, but the balance has shifted toward the shallow end of the pool. Jump in with care. □

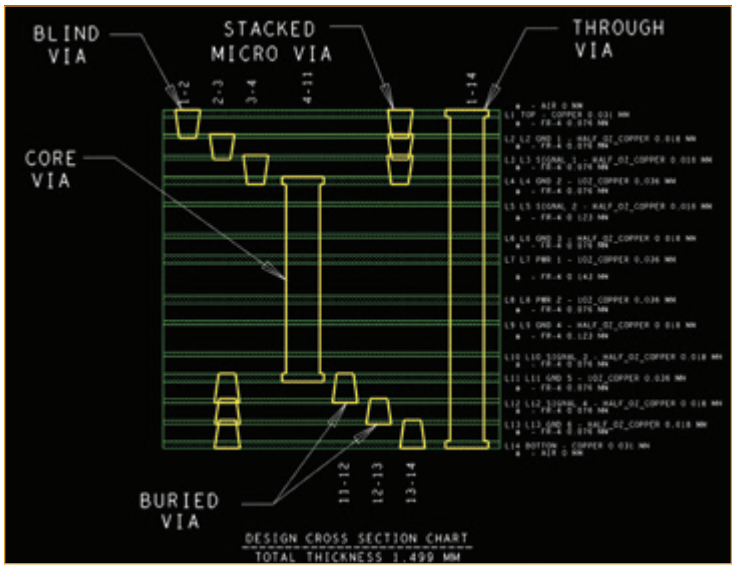


**FIGURE 2.** Vias come in many flavors, as shown here.

# Life During Covid 'Wartime'

Despite the pandemic, our new website is about to be unveiled.

THIS MONTH, I'LL share updates on the progress the PCEA staff is making toward establishing a web presence and report on what the PCEA is preparing in support of the PCB engineering community.

Although PCEA chapter activities have been limited because of restrictions due to Covid-19, PCEA Chairman Steph Chavez offers his perspective on the challenges of staying connected without using traditional means. Last, I share our most updated list of professional development and event opportunities, although some may be affected by the Covid-19 outbreak. Stay tuned for more updates.

## PCEA Updates

"This ain't no party. This ain't no disco. This ain't no foolin' around."–"*Life During Wartime," Talking Heads*

As we physically isolate ourselves to prevent the spread of Covid-19, our work cannot stop. Many still have day jobs to tend to; you might be working from home, or you might be required to mask-up and join coworkers on the front lines of an essential business. Our industry's needs and domestic responsibilities have not changed, but how we process them has. Adaptation is a key to those of us working at the PCEA to build a new organization. Now, more than ever, we are relying on the internet and online meetings to evolve our ideas and act on them.

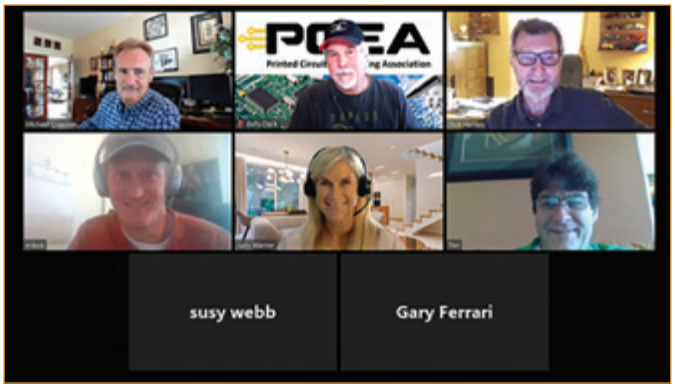


**FIGURE 1.** Left to right, top to bottom: Mike Creeden, Kelly Dack, Rick Hartley, Mike Buetow, Judy Warner, Tim Mullin (Susy Webb and Gary Ferrari not pictured).

The PCEA website. As we approach a target release date for the PCEA website, I joined an online meeting from my basement office to review content for the site. As I donned my ear pods and plugged in my camera, I couldn't get the tune "Life During Wartime" by the Talking Heads out of my head. As each invitee checked in on the screen, I felt an appreciation for the depth of experience that even this small portion of PCEA members brought to the table. Vice chairman Mike Creeden led the meeting, and I quickly discerned this group was not here to party, disco, or fool around; they were meeting to execute and accomplish (**FIGURE 1**). They were armed with cameras, mics and headsets, using the best means possible to share their ideas for planning to serve the PCB engineering community with a viable website.

Starting any effort, such as developing a new website, can be a daunting task. An important purpose of our site is to establish a base platform to continue our growth as an organization. Most of us think we know what needs to be basically communicated on a website, but section headers and click logic for a site like ours requires knowledge of electronics and industry topics and resources, as well as experience in psychology, etc. The PCEA is blessed to have a couple of master web communicators on board. Judy Warner and Mike Buetow are easily recognizable publishing powerhouses in the electronics world and have provided many hours of their time to help forge the site, for which we all are grateful.

Keep an eye out for the rollout of our new website set for around May 15 at pce-a.org (**FIGURE 2**). At the site, you will see the PCEA is a nonprofit organization, and you can read our mission statement and *raison d'etre*. Dive deeper, and you will find information on our international engineering network chapters, including seven new ones that will be established soon. There is a feedback page where you can join our mailing list, as well as an education area, which will help you fulfill your professional development by offering many resources; there are too many to list here, but they are all too valuable to pass up!

Moving forward. On behalf of the PCB chapter leadership, we hope you are doing well. This has been quite a month, and the isolation challenges affecting printed circuit engineering and our local chapters are real. I've read from some of our chapter leaders about postponements of chapter meetings and some stagnation of activities due to our present shelter-in-place conditions.

Chairman Steph Chavez and I discussed the realities of how chapter members are being challenged. Some are working from home; some may have no

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work at all. Covid-19 restrictions have cast a lot of unique conditions on our community. We have asked chapter leaders for feedback or stories from our members, which we will share in the coming months. As the PCEA continues to organize, we will find our niche for helping our members as they "hunker down" with their unique local conditions. We are actively forming means by which our members and the entire PCB engineering communities can use this time to tap into resources that will help them prepare for when the world reopens.

Share your stories and photos. In the meantime, we are looking for heartfelt stories from our readership who would like to provide personal stories with regard to how your PCB engineering, manufacturing or connected job has been affected, and how you are coping and adapting. Your personal accounts might help all of us adjust our focus on how we can help.

We would love to read any content or reports you have to share, which we may include in this column. Photos? Heck yes! We'll take all the isolation photos of you performing your PC engineering tasks that we can print.

Please send stories and photos to kelly.dack.pcea@gmail.com.

## Message from the Chairman

*by Stephen Chavez, MIT, CID+*

The Covid-19 pandemic has reshaped our daily lives and work environments. Most of us are working remotely or in isolation in one form or another these days. The industry is getting hit hard. Our country and the world are going through some tough times. Many feel a bit stir crazy from staying in place almost 24/7, with limited outside social interactions due to "social gathering restrictions" in response to fighting the spread of this virus.

I, too, feel cooped up. My only outside interaction nowadays is that not-so-frequent trip to the local grocery store. Wearing a face mask in publicly populated areas is not something I have gotten used to yet. Part of our communication as humans is facial expressions. I feel wearing face masks makes our public interactions with one another a bit cold and impersonal. It takes away that simple gesture – a smile – that we usually give without hesitation to others. Sometimes a simple smile can make someone's day.

I miss in-person, face-to-face chats that always included a handshake or a hug because I am a people person. Isolation may be tough, but I know it is helping. Please join me in sending prayers to all our first responders who are going above and beyond to help keep us safe. Thank you! God bless you and keep you safe.

The negative impact of this pandemic is being felt everywhere. From many business closures, cutbacks, furloughs and layoffs unfolding across the board throughout the globe, these are tough times. But during these tough times, we do what we always do: We adapt and overcome.

Now it's virtual meetings. WebEx, GoToMeeting, and Zoom, to mention a few, seem to be our way of life. It was once thought that only certain professions used these types of tools for remote collaboration; today, these tools are almost as common as cellphones. Almost everyone is adapting and using these tools. Kids in grade schools are using them daily to continue their education.


**FIGURE 2.** Website screenshot.

With domestic and international travel at an extreme low, many have taken to this virtual lifestyle. I, like many others, find myself jumping from one online meeting to another, and in some instances, participating in two meetings at the same time. I never used my laptop and cellphones as much as I do now. I live on them!

I'm not alone in doing this, however. So many others have adapted to this new "normal" as well, such as members of the PCEA Executive Board. With most of us on this board having day jobs, a lot of passion, hard work, dedication and extra effort are going into getting this right. Things are moving fast, to say the least.

We continue to solidify the foundation of the PCEA. Our website is a work in progress with a new and improved version ready this spring. The team working on this is doing an outstanding job so far. I'm truly looking forward to its official release. The PCEA business structure is also coming together as planned. We should be ready for an official virtual open house soon.

As always, I highly encourage you to get involved. Join the PCEA by visiting our website and registering as a member to become part of the PCEA collective. Reach out to me (stephen.chavez.pcea@gmail.com) or Kelly Dack to get more information as well.

## Professional Development and Events

It has been our custom to highlight all upcoming industry events to look out for in 2020. We can only remain hopeful that these events will not be affected by Covid-19.

- Jun. 22–25: Realize LIVE 2020 (virtual)
- Sept. 8–11: PCB West (Santa Clara, CA)
- TBD: AltiumLive 2020 (San Diego, CA)
- Nov. 11: PCB Carolina (Raleigh, NC)

Spread the word. If you have a significant electronics industry event that you would like to announce, please send me the details at kelly.dack.pcea@gmail.com.

## Conclusion

No matter your part in this industry, let's continue to move forward together by finding solutions for the unknown and having hope for the future. ❑

# Stop Thinking about CURRENT DENSITY and Via Temperature

Via temperature is determined by the temperature of the trace associated with the via, not the current itself. **by DOUGLAS G. BROOKS, PH.D.**

Many designers and some EDA design tools place heavy emphasis on current density when sizing traces for a given current. Current density is current/unit area. Thus, it does make some intuitive sense that trace temperature might be proportional to current density: the higher the current, the higher the current density, and therefore the higher the temperature. But it is much more complicated. Following this design rule blindly may lead to significant design errors, especially when designing vias for allowable current. And a few examples will illustrate why.

Simple case. **FIGURE 1** illustrates two microstrip traces on a board. Trace B is thinner and wider than Trace A, but they both have the same cross-sectional area. And, they both carry the same current. Therefore, they have the same current density. But they *do not* have the same temperature.

The thinner, wider Trace B will have a significantly lower temperature than Trace A. The reason is the most important cooling factor is thermal conduction away from the trace through the dielectric. Trace B, with the greater surface area in contact with the dielectric, will cool more efficiently and will therefore have the lower temperature.

Thermal concept. We are all familiar with the expression $I^2R$. Traces heat by $I^2R$ power dissipation. The variable I represents current, so we can also express it as $C^2R$, where C is the current. Now heating is a point concept. That is, traces heat at a point, and the temperature of a trace will be different at different points along the trace if the resistance changes. So, we can think of the expression $C^2R$ as power dissipation per unit length. Now R (per unit length) is resistivity divided by area, or $\rho/(w*th)$. Thus, we conclude the change in temperature, $\Delta T$, is proportional to

$$\Delta T \propto C^2\rho/(w*th) \quad \text{(Eq. 1)}$$

where: $\Delta T$ = change in temperature
C = Current
$\rho$ = resistivity
w = trace width
th = trace thickness

Since $C/(w*th)$ is current density, J, and resistivity is a constant, we conclude the change in temperature is proportional to current density *multiplied* by current (not just current density).

$$\Delta T \propto C*J \quad \text{(Eq. 2)}$$

Derived equation. In our book[1], Dr. Adam and I derived an equation that fit the external IPC- 2152[2] external current/temperature curves very well. It is

$$\Delta T = 215.3 * C^2 / (W^{1.15} * Th^{1.0}) \quad \text{(Eq. 3)}$$

where: $\Delta T$ = change in temperature in °C
C = Current in amps
W = Trace width in mils
Th = Trace thickness in mils

Recognizing that $C/(W*Th)$ is current density, J, this equation can be converted to

$$\Delta T = 215.3 * C * J / (W^{0.15}) \quad \text{(Eq. 4)}$$

Thus, the equation we derived in our book is consistent with the Thermal Concept section above.


**FIGURE 1.** Microstrip traces with equal current density can have significantly different temperatures.

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**From IPC-2152 data.** We can easily look at the relationship between current density and trace temperature using the IPC data themselves. **TABLE 1** is derived using the various external curves in that publication. It selects data points such that the cross-sectional area of the traces will be the same. Then with constant current, we achieve a selection of temperature points with constant current density. But as can be seen from Table 1, the trace temperature is not constant with current density and does not depend on current density.

**Current density and vias, Case 1.** Perhaps the most significant misuse of the relationship between current density and trace temperature has to do with via temperatures. It is almost universally assumed (it seems) that current density is directly related to via temperature. We have shown in our book that that assumption is *totally* false. Via temperature is *not* related to the current through the via. It is determined by the temperature of the trace associated with the via[3]. Reason: The via is much smaller than the trace, and the trace acts as a significant heat sink for the via. It is (almost) true that no matter how much current is put through the via, the via temperature cannot rise much higher than the temperature of the parent trace.

We confirmed this with experimental results.[4] Two traces were each fabricated on a 63-mil-thick FR-4 board. They were nominally 6" long (3" on the top layer and 3" on the bottom layer) 0.5 oz. traces plated with 1.0 oz. copper, connected by a 10-mil via plated to a nominal 1.0 oz. thickness. One trace was 27 mils wide and the other 200 mils wide. But in each case, there was only a single 10-mil-diameter via. The results are shown in **TABLE 2**.

The results are evident in the table. But note tests a and d, in particular. A 4.75A current heats the 10-mil via to 64.5° when there is a 27-mil-wide parent trace. But an 8.55A current only heats the via to 44.5° when the parent trace is 200 mils wide. This confirms the *current does not determine the via temperature*. The parent trace does. Provided the parent trace is sized correctly, the via temperature will not rise much higher than the parent trace temperature.

Special asides:

a. Note current density through the via has nothing to do with the via temperature.

b. A current of 8.55A through an isolated via (without a parent trace) or through a 27-mil-wide trace will melt the via or trace in less than 1 sec.

**TABLE 1.** Data Points from Selected IPC-2152 External Current/Temperature Curves

| Thickness Oz. | Thickness Mil | Width (Mil) | Current A | Current Density* | ΔT °C |
|---|---|---|---|---|---|
| 0.5 | 0.65 | 300 | 10 | 0.051 | 47 |
| 1.0 | 1.3 | 150 | 10 | 0.051 | 50 |
| 2.0 | 2.6 | 75 | 10 | 0.051 | 55 |
| 3.0 | 3.9 | 50 | 10 | 0.051 | 61 |

*Amps/mil$^2$

**Current density and vias, Case 2.** At one point in our book, we ran a series of simulations comparing trace and via temperatures for traces with different widths and currents. The results are shown in **TABLE 3**[5]. We ran a multiple regression analysis comparing via temperature to trace temperature and current.

The resulting equation is

$$Tvia = -7.07 + 0.88*Ttrace + 4.85*C \quad \text{(Eq. 5)}$$

With an $R^2$ of 0.996

where: Tvia is the via temperature, °C
Ttrace is the trace temperature, °C
C is current, amps

The equation suggests via temperatures are lower than the parent trace temperatures for lower currents and begin to exceed the trace temperature by a few degrees as the current increases. This is exactly what we see in the experimental results.

When current density is added to the regression, it does not make a statistically significant contribution to the via temperature. This is further support for the argument that via temperatures depend on the parent trace temperature, *not* on current density.

## Conclusion

Relying on the current density to make layout decisions is using the wrong metric. At best, relying on current density

**TABLE 2.** Measured Results of Via Tests

| Test | Trace Width (Mils) | Current A | Trace Temp. (°C) | Via Temp (°C) |
|---|---|---|---|---|
| a | 27 | 4.75 | 66 | 64.5 |
| b | 27 | 6.65 | 114 | 109 |
| c | 200 | 4.75 | 30.5 | 31.5 |
| d | 200 | 8.55 | 40.5 | 44.5 |

**TABLE 3.** Various Current/Temperature Simulation Results

| Trace Width (mm) | Trace Thickness (mm) | Area (mm$^2$) | Current A | Current Density A/mm$^2$ | Trace Temp. (°C) | Via Temp. (°C) |
|---|---|---|---|---|---|---|
| 0.4 | 0.035 | 0.014 | 2 | 142.9 | 91.4 | 82.4 |
| 0.4 | 0.035 | 0.014 | 2.3 | 164.3 | 123.2 | 109.9 |
| 0.66 | 0.035 | 0.0231 | 3 | 129.9 | 86.9 | 80.9 |
| 0.66 | 0.035 | 0.0231 | 4 | 173.2 | 166.7 | 152.9 |
| 1.2 | 0.035 | 0.042 | 3 | 71.4 | 47.9 | 48.7 |
| 1.2 | 0.035 | 0.042 | 4 | 95.2 | 74.1 | 75.8 |
| 1.2 | 0.035 | 0.042 | 5 | 119 | 115.5 | 118.8 |
| 1.8 | 0.035 | 0.063 | 5 | 79.4 | 70.8 | 76.8 |
| 1.8 | 0.035 | 0.063 | 6 | 95.2 | 100.2 | 110.2 |
| 2.5 | 0.035 | 0.0875 | 6 | 68.6 | 68.1 | 77.6 |
| 2.5 | 0.035 | 0.0875 | 7 | 80 | 90.3 | 104.9 |

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will lead to inefficient layout decisions, but at worst it can lead to poor decisions and significantly wasted board real estate. □

## NOTES

1. Douglas G. Brooks, Ph.D., and Johannes Adam, Ph.D., *PCB Trace and Via Current and Temperatures: The Complete Analysis,* 2nd edition, 2017. See Equation 5.5, p. 47.
2. IPC-2152, "Standard for Determining Current-Carrying Capacity in Printed Board Design," August 2009.
3. Via current, temperatures and current density are covered extensively in Brooks and Adam, Chapters 7 and 8 and Appendix A6.
4. Douglas Brooks, Ph.D., "Empirical Confirmation of Via Temperatures," PCD&F, February 2016. Table 2 is reprinted from that article.
5. See book referenced in Note 1. Table 3 is adapted from Table 7.2 on p. 86.

**DOUGLAS BROOKS, PH.D.**, has a master's in electrical engineering from Stanford and a Ph.D. from the University of Washington. For the past 27 years he has owned a small engineering service firm (ultracad.com) and written two books and numerous technical articles on printed circuit board design and signal integrity. He published *PCB Trace and Via Temperatures: The Complete Analysis*, 2nd Edition," with Johannes Adam in 2017.

# It Was Predicted for Years. ENGINEERS Are Finally Taking Over PCB DESIGN.

Recent salary survey results suggest newcomers may be entering the field. **by CHELSEY DRYSDALE**

Each year PCD&F surveys the PCB design community concerning issues surrounding their profession. For years, the feedback has had one connecting thread: Many PCB designers are experts with decades of experience. Their retirement has loomed large and has been widely anticipated, accompanied with concerns – and a little trepidation – about who will replace them. In conference classes and site visits in recent years, companies have discussed how they are working with educators at universities and local colleges to inform engineering students about industry opportunities. Recent survey results hint their efforts may be starting to pay off. And the time for boomer retirements is here.

PCD&F conducted its annual design engineers' salary survey in early 2020, receiving 254 qualified responses from bare board designers, managers and design engineers. Data compiled included job titles and functions, ages, years of experience, education, location, types of projects, annual salaries and sales, job satisfaction and challenges, ECAD tools used, and years left in the field, among other data. While year-over-year changes are shown, they are for comparison only, and should not be assumed to be definitive.

**Job titles and functions.** When PCD&F last published its salary survey in early 2019, senior designers ruled the field. For the most recent dataset, which includes some 254 respondents, the percent of senior designers responding is 39%, which coincides with respondents' ages and years of experience, to be covered further below. Relative to past years' surveys, the number of senior designers is down considerably.

Another 17% identified as PCB designers, 13% said design engineers, 8% are senior engineers, and 12% are hardware engineers (**TABLE 1**). Fewer PCB design managers took the 2020 survey (nearly 4%) compared to past years. All other job titles had 2% or less of responses each.

The percentage of respondents indicating PCB design is their principal job function is down, at 64% of responses in 2020, compared to 74% in the prior survey (**TABLE 2**). PCB engineering (13%), systems design (8%), and design/layout management (6%) all rose against previous surveys.

Likewise, the percentage of time spent each week on board design has dropped from the previous data (**FIGURE 1**). Some 17% spend 100% of business hours on board design, down

**TABLE 1.** Respondents by Job Title

| | 2020 | 2018 | 2017 | 2016 | 2015 | 2014 |
|---|---|---|---|---|---|---|
| Senior PCB designer | 39% | 59% | 56% | 52% | 52% | 54% |
| PCB designer | 17% | 13% | 14% | 15% | 16% | 20% |
| PCB design manager | 3.5% | 5.5% | 9% | 9.1% | 9% | 8.2% |
| Design engineer | 13% | 6.7% | 8% | 7.6% | 8% | 6.8% |
| Hardware engineer | 12% | 8.5% | 3.3% | 6.5% | 4.2% | 3.3% |
| Senior engineer | 8.3% | 1.8% | 5% | 3.4% | 3.2% | 1.9% |
| Principal engineer | 2% | 2.4% | 2.7% | 2.2% | 3.2% | 1.9% |
| CAD librarian | 2% | 1.8% | 1.3% | 1.8% | 2.2% | 1.4% |
| Electronics technician | 1.2% | 0.6% | 0.7% | 0.9% | 1% | 1.2% |
| Technical director | 1.2% | 0.6% | 0% | 0.7% | 0.8% | 0.5% |

*Numbers might not total 100% due to rounding. n = 254. Note: No data were collected in 2019.*

**TABLE 2.** Principal Job Functions

| | 2020 | 2018 | 2017 | 2016 | 2015 |
|---|---|---|---|---|---|
| PCB design | 64% | 74% | 75% | 70% | 73% |
| Design/layout management | 5.9% | 4.9% | 7.6% | 11% | 9.5% |
| PCB engineering | 13% | 10% | 9% | 9.6% | 8.9% |
| Systems design | 7.9% | 4.2% | 2.3% | | |
| Engineering management | 2% | 0% | 2% | 3.6% | 2.8% |
| ECAD librarian | 2% | 3% | 1.7% | 1.6% | 2.4% |
| Applications engineer | 1.6% | 0.6% | 1.3% | 1.6% | |
| Engineering consulting | 2% | 1.2% | 0.3% | 0.7% | 2.2% |
| Design support (drafting) | 1.2% | 0% | 0% | 0.2% | 0.4% |

*Numbers might not total 100% due to rounding. n = 254*

from 20%, while 32% spend 76 to 99% of their time designing, down from 40%. Thirty-four percent of respondents spend less than half their time on board design, up from 10% in the beginning of 2019.

What design engineers are doing more of is buying things. While the percentage of respondents who specify software ticked up, boards and assembly services jumped (**TABLE 3**). Design engineers are also making more calls on down-the-line products like solder and testing.

Experience. PCD&F's past surveys have reflected a veteran-heavy industry with few signs of a younger generation replacing aging designers. If this year's survey is any indication, change is afoot. More than a quarter of 2020 respondents are 35 years old or younger, compared to less than 10% in the last survey, and designers between ages 51 and 70 account for 53%, down from 62% (**FIGURE 2**).

Some 36% of respondents have 15 years of experience or fewer, about half of which have fewer than five years in the industry (**FIGURE 3**). At the end of 2018, about 16% said they have 15 years of experience or fewer, with 7% in their first five years. Nearly 34% of respondents have more than 30 years of experience, compared to 40% in the prior data.

Asked how many more years they plan to work as a design engineer, nearly 27% said 16 or more years. Three-fifths plan to leave the profession within the next 10 years, so while emerging designers are entering the field, the industry still needs more of them.

On a scale of 1 to 7, with 1 being lowest (completely dissatisfied) and 7 being highest (highly satisfied), designers were asked about job satisfaction. Results indicate designers are less happy than they were a year ago. Considering the timing of the survey during a global pandemic, that's hardly a surprise. Seventy-nine percent of respondents have some level of satisfaction, while 12% are mildly or totally dissatisfied.

Salaries. Less than half of designers (47%) are at or above their company's salary range for their position, down from 57% over a year ago. According to 2020 results, respondents'

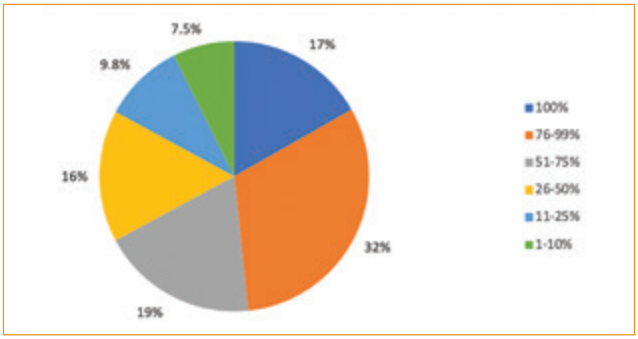


**FIGURE 1.** Weekly percentage of time working on board design.

**TABLE 3.** Product/Service Purchases Evaluated, Recommended, Specified or Approved

| | 2020 | 2018 |
|---|---|---|
| ECAD software | 75% | 74% |
| CAM software | 26% | 24% |
| CAE software | 15% | 16% |
| MCAD software | 14% | 12% |
| Prototype PCB services | 56% | 44% |
| Volume PCB fabrication services | 33% | 26% |
| Design services | 38% | 35% |
| Connectors and cables | 37% | 24% |
| Active/passive components | 35% | 24% |
| FPGAs/PLDs | 16% | 14% |
| Assembly services | 32% | 23% |
| Solder mask | 21% | 12% |
| Substrate materials | 21% | 19% |
| Computers and peripherals | 18% | 17% |
| Solder materials | 18% | 10% |
| Epoxies and finishes | 15% | 6% |
| Consulting services | 15% | 13% |
| Test/measurement services | 22% | 13% |
| None of the above | 10% | 15% |

*Respondents could choose more than one answer*

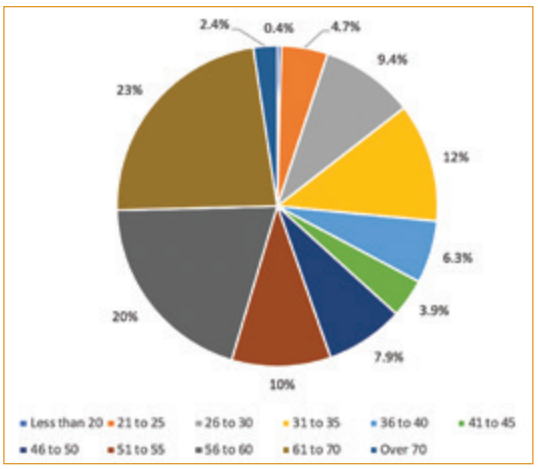


**FIGURE 2.** Current age.

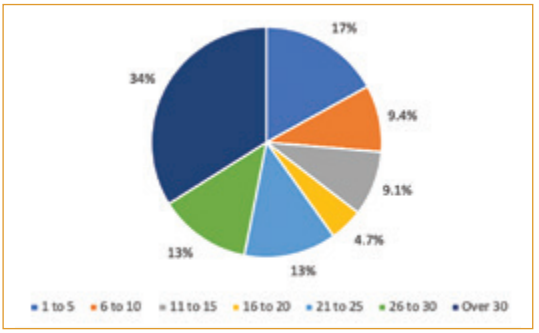


**FIGURE 3.** Years of experience.


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*written by*

## Charles Pfeil

Charles Pfeil has spent over 50 years in the PCB industry as a designer, owner of a service bureau, and in engineering management and product definition roles at Racal-Redac, ASI, Cadence, PADS, VeriBest, Mentor Graphics, and Altium. He was the original product architect of Expedition PCB.

salaries are simultaneously higher on the low end *and* the high end compared to the lead-up to 2019. More than 21% of the 254 people who took the survey this year said they make $50,000 or less, compared to 9% last time (**TABLE 4**). Another 25% bring in more than $110,000 annually, up from 18%. Some 40% have salaries from $70,000 to $110,000, compared to 55% in the last survey.

**TABLE 4.** Average Annual Salary by Segment

| | Total | 4-Yr. Degree | 2-Yr. or Less | AGE =/<40 | AGE 41+ | Male | Female | Manager? | N. America | Europe | SE Asia/ China |
|---|---|---|---|---|---|---|---|---|---|---|---|
| <$10,000 | 5.5% | 9.1% | 0% | 14.3% | 1.2% | 5.7% | 3.9% | 4% | 1.1% | 2.4% | 75% |
| $10,000 to $15,000 | 2% | 2% | 2% | 3.6% | 1.2% | 2.2% | 0% | 1.7% | 0.6% | 2.4% | 0% |
| $15,001 to $20,000 | 0.8% | 1.3% | 0% | 2.4% | 0% | 1% | 0% | 0.6% | 0% | 0% | 0% |
| $20,001 to $25,000 | 2.4% | 3.3% | 1% | 6% | 0.6% | 2.6% | 0% | 1.2% | 1.1% | 7.3% | 0% |
| $25,001 to $30,000 | 2.4% | 3.9% | 0% | 2.4% | 2.4% | 2.6% | 0% | 2.3% | 0% | 7.3% | 0% |
| $30,001 to $40,000 | 3.5% | 4.6% | 2% | 8.3% | 1.2% | 4% | 0% | 4% | 0% | 17.1% | 0% |
| $40,001 to $50,000 | 4.3% | 3.9% | 5% | 7.1% | 2.9% | 4.8% | 0% | 2.9% | 1.1% | 12.2% | 0% |
| $50,001 to $60,000 | 7.9% | 7.1% | 9% | 8.3% | 7.7% | 8.3% | 3.9% | 7.5% | 5.1% | 19.5% | 25% |
| $60,001 to $70,000 | 7.1% | 8.4% | 5% | 9.5% | 5.9% | 7.5% | 3.9% | 6.9% | 5.7% | 12.2% | 0% |
| $70,001 to $80,000 | 5.9% | 3.9% | 9% | 3.6% | 7.1% | 6.1% | 3.9% | 7.5% | 5.1% | 12.2% | 0% |
| $80,001 to $90,000 | 11% | 9.1% | 13% | 7.1% | 12.4% | 10.1% | 15.4% | 12.6% | 14.2% | 2.4% | 0% |
| $90,001 to $100,000 | 12% | 12.3% | 11% | 7.1% | 14.1% | 11.4% | 15.4% | 10.9% | 15.9% | 0% | 0% |
| $100,001 to $110,000 | 11% | 9.7% | 13% | 6% | 13.5% | 11% | 11.5% | 14.4% | 14.8% | 4.9% | 0% |
| $110,001 to $120,000 | 5.1% | 3.3% | 8% | 2.4% | 6.5% | 5.3% | 3.9% | 5.8% | 7.4% | 0% | 0% |
| $120,001 to $130,000 | 8.7% | 5.2% | 14% | 3.6% | 11.2% | 7.5% | 19.2% | 4.6% | 11.9% | 0% | 0% |
| $130,001 to $140,000 | 2.4% | 2% | 3% | 2.4% | 2.4% | 2.6% | 0% | 2.9% | 3.4% | 0% | 0% |
| $140,001 to $150,000 | 2% | 2.6% | 1% | 1.2% | 2.4% | 1.3% | 7.7% | 2.9% | 2.8% | 0% | 0% |
| >$150,000 | 6.7% | 8.4% | 4% | 4.8% | 7.7% | 6.1% | 11.5% | 7.5% | 9.7% | 0% | 0% |

*Numbers might not total 100% due to rounding. n = 254*

More than half of respondents receive an annual bonus (51%), with 38% receiving a bonus of 1 to 3% of their salaries; 30% receive 4 to 7% of their salaries; and 31% receive more than 7% of their salaries.

Over 45% of respondents' salaries rose 1 to 3% in the past year; 13% rose 4 to 6%; 9% rose 7 to 10%; and almost 8% rose more than 10%. Twenty-two percent said their salaries haven't changed in the past year. Most respondents (95%) still have the same job as last year.

Most of this year's respondents aren't in a managerial position (69%). Some 27% have 1 to 5 staff members reporting to them. Ninety percent are male.

Educational opportunities and benefits. Half of respondents' employers support tuition reimbursement, while 58% provide on-the-job training. Some 47% support classes at conferences, and 33% provide company-sponsored classes. Mentoring occurs at 29% of respondents' companies, and 17% support college classes. Twenty-six percent do not support any educational opportunities listed in the survey.

Health and dental insurance always lead the list of benefits offered, this time with 83% and 71% of responses, respectively. Other benefits are as follows:

- Life insurance (65%)
- 401(k) plan (58%)
- Telecommuting (33%)
- Company pension or retirement plan (31%)
- Stock purchasing plan (27%)
- Profit sharing (22%)
- Sabbatical (8%)
- Daycare facilities (2%)

More than 11% of respondents' companies do not provide benefits. The majority (66%) said their benefits haven't changed in the past year, while 12% have more benefits offered, or the same benefits at a lower cost. Some

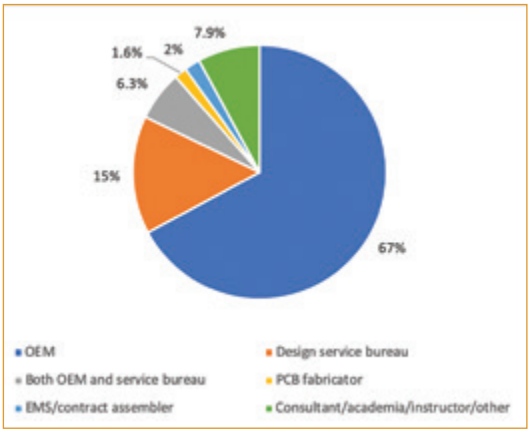


**FIGURE 4.** Company type.

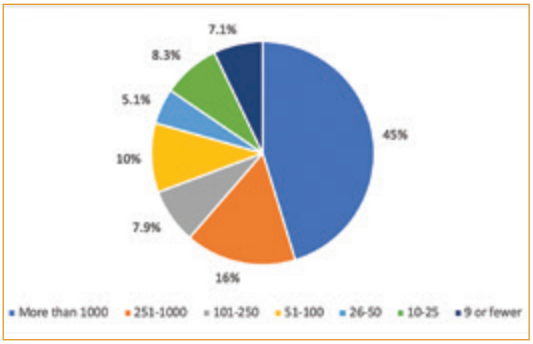


**FIGURE 5.** Company's total number of employees worldwide

**TABLE 5.** Highest Level of Education

| | 2020 | 2018 | 2017 | 2016 | 2015 |
|---|---|---|---|---|---|
| High school | 2% | 4.2% | 3.3% | 5.8% | 4.4% |
| Some college - no degree | 15% | 25% | 24% | 23% | 23% |
| 1- to 2-year associate's degree | 22% | 30% | 38% | 31% | 33% |
| BA/BS degree in non-engineering field | 6% | 5.5% | 4.7% | 4% | 5.2% |
| BS degree in engineering or related field | 37% | 27% | 24% | 28% | 26% |
| Master's degree (any field) | 7.3% | 7.3% | 5.3% | 7.1% | 8.6% |
| Ph.D. (any field) | 2% | 1.2% | 0.3% | 0.5% | 0.4% |

*Numbers might not total 100% due to rounding. n = 254*

22% have fewer benefits, or the same benefits at a higher cost.

Education. For the first time, a majority of respondents have bachelor's degrees. Respondents with bachelor's degrees in engineering or a related field garnered more responses than in the past (37% compared to 27%) (**TABLE 5**). Master's degrees were up compared to last year as well. Nearly 38% said they have attended some college or have an associate's degree.

Of those with four-year degrees, 70% have degrees in electrical engineering, while 20% have other engineering degrees.

Certifications. Thirty-five percent of designers who took the 2020 survey are IPC certified, with 57% CID and 43% CID+.

Employers. Two-thirds of survey respondents work for an OEM (**FIGURE 4**). Another 15% said they work for a design service bureau. More respondents consider themselves consultants/academics/instructors than the prior survey (8% compared to 6%). Most respondents work for larger companies (**FIGURE 5**).

Location. Some 63% of respondents are in the United States, with 20% on the West Coast, including Arizona (**FIGURE 6**). Another 15% are in Central/Western Europe, and 6% reside in Canada.

Projects and technology trends. When asked what types of projects and/or technologies respondents engineer, design, or lay out, they checked all that apply in **TABLE 6**, with a few notable shifts. Compared to the last survey, single-sided PCBs dropped from 53% to nearly 44%, while 12-plus-layer PCBs fell from 66% to 45%. Flex/rigid-flex PCBs are also down (45% compared to 53%), as are microvias/HDI (47% compared to 63%). Embedded systems (30%), chip-scale packages (23%), SoCs (28%), and enclosures (26%) all saw increases in responses.

According to this year's results, more than half of respondents produce 10 or fewer

*continued on pg. 38*

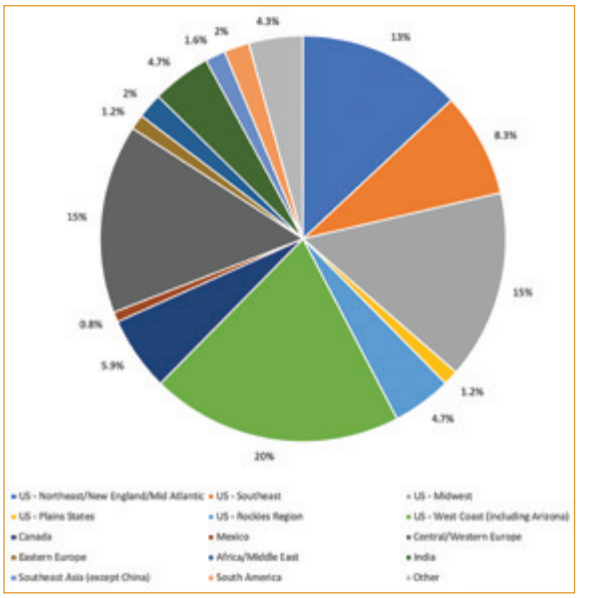


**FIGURE 6.** Respondents by location.

**TABLE 6.** Projects and Technology Trends

| | 2020 | 2018 | 2017 | 2016 | 2015 | 2014 | 2013 | 2012 |
|---|---|---|---|---|---|---|---|---|
| Single-sided PCBs | 43.7% | 53.3% | 50.2% | 52.5% | 54.7% | 56.5% | 56.5% | 47% |
| Double-sided PCBs | 82.7% | 81.8% | 84% | 83% | 82.6% | 83.6% | 81.5% | 81% |
| 4 to 6 layers | 79% | 82.4% | 86% | 82.6% | 84.8% | 83.2% | 83.4% | 84% |
| 7 to 10 layers | 57.5% | 69.7% | 75% | 65.2% | 68% | 68.6% | 65.8% | 61% |
| 12+ layer PCBs | 45.3% | 65.5% | 63.1% | 60% | 59% | 61% | 56.3% | 53% |
| Flex/rigid-flex PCBs | 45.3% | 53.3% | 57.8% | 53.1% | 55.3% | 53.1% | 49.9% | 44% |
| FPGAs/PLDs | 41.3% | 38.2% | 40.2% | 36.8% | 35.7% | 43.3% | 40.4% | 36% |
| Microvias/HDI | 47% | 63% | 55.2% | 49% | 51.5% | 51.1% | 45.4% | 38% |
| RF/microwave circuitry | 36.6% | 47.9% | 41.5% | 41.5% | 41.7% | 39.9% | 42% | 36% |
| BGAs | 60.2% | 64.9% | 64.5% | 65.2% | 65.3% | 66.6% | 67.7% | 58% |
| ASICs/ICs | 35% | 30.9% | 37.5% | 30.4% | 31.9% | 33.2% | 29% | 28% |
| Embedded systems | 30% | 18.8% | 15.6% | 21.2% | 19.8% | 17.9% | 22.1% | 15% |
| Chip-scale packages | 23% | 16.4% | 18.6% | 16.3% | 19.2% | 12.6% | 13.3% | 11% |
| SoCs | 28.4% | 17.6% | 16% | 15.1% | 16% | 13.7% | 12.6% | 9% |
| SiPs | 16% | 10.9% | 10.3% | 11.2% | 10.2% | 9.9% | 11.2% | 10% |
| Enclosures | 26% | 17.6% | 19% | | | | | |
| Optoelectronics | 31% | | | | | | | |
| Package-on-package | 11.4% | | | | | | | |

*Respondents could choose more than one answer. Numbers might not total 100% due to rounding. n=254*

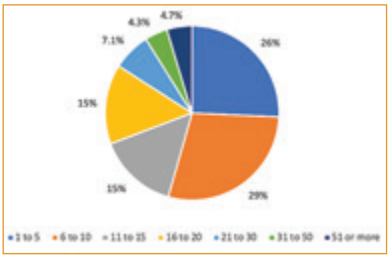


**FIGURE 7.** New designs each year.

# HIGH-END SYSTEMS Product Needs

SiP, MCP and DDR5 support faster speeds and higher power requirements. by KARTIK ANANTH and DALE BECKER

*Ed.:* This is the sixth of an occasional series by the authors of the *2019 iNEMI Roadmap.* This information is excerpted from the roadmap, available from iNEMI (inemi.org/2019-roadmap-overview).

New high-end computing system technologies becoming available for such applications as servers, telecom and the cloud must meet bandwidth, power, thermal and environmental challenges. Advanced packaging technologies that can drive integration and increase functionality, at acceptable cost and risk levels, will be key enablers for the sector.

## Integration Trends

Advanced silicon integration technologies, such as through-silicon vias (TSVs), are enabling 2.5D silicon interposers and 3D chip-stacking, providing high-density interconnect, and therefore, high bandwidth capability between components. Memory modules have started to use this already, and they will continue to expand. More compute elements are also starting to use TSV and novel packaging technologies to enable heterogenous integration by combining compute "chiplets" with I/O memory chiplets integrated either via 2.5D substrate level or 3D stacking.

System-in-package (SiP) and multichip package (MCP) technologies can optimize cost and provide more integration in a package. Integrating voltage regulation and silicon photonics with processor chips or bridge chips will increase. The growth in mobile systems has been the driver for development of these packaging architectures. High-end systems will also adopt packaging technologies such as SiP and MCP because they permit higher numbers of interconnect pins, more memory in a condensed space, and more cores without increasing the power envelope.

Optical interconnect will be used more broadly. First, transceivers and active optical cables (AOCs) will be used more broadly for in-frame communication, potentially replacing copper interconnect in backplanes or cables when the cost, power and bandwidth tradeoffs justify the switch to optical. Integrating optical devices into packaging to reduce trace length and, thus, power demand for high bandwidth interfaces will demand advanced packaging and leverage SiP and package-on-package (PoP) for increasing integration at the package level.

The desire for higher levels of integration of optics will favor adoption of silicon photonics. Silicon photonics, especially with vertical cavity surface emitting lasers (VCSELs), will lower cost and allow shorter rack-to-rack, or even within the rack, types of interconnections for high-density, high-bandwidth interconnections. System-level cost management, integration density, and power limit tradeoffs must be carefully considered as development of silicon photonics is pursued.

## Electrical Considerations

Electrical interconnection will continue to be the dominant interconnection for short-reach communication. Signaling

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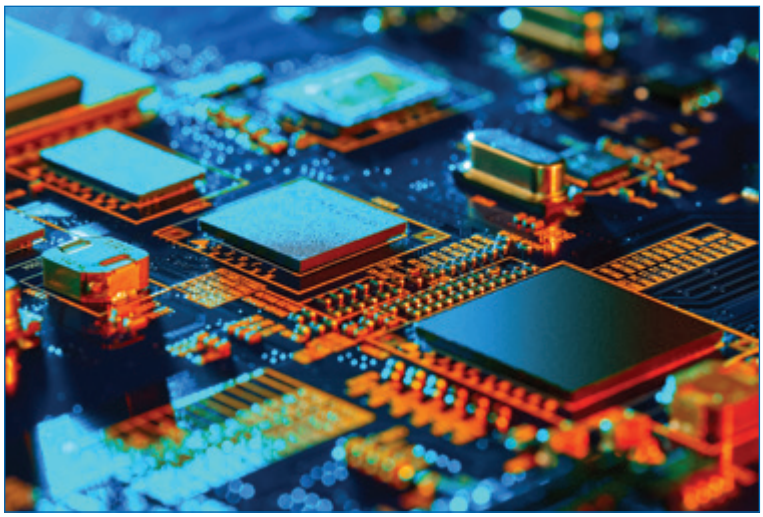

**FIGURE 1.** High-end computing systems will leverage multichip packages for higher bandwidth.

# Materials Considerations for AUTOMOTIVE RADAR DESIGNS

A holistic view of 77GHz radar sensors as a PCBA build, considering fabrication, assembly and packaging materials.

**by LENORA CLARK, PAUL SALERNO and SENTHIL KANAGAVEL**

The Society of Automotive Engineers (SAE) and US Department of Transportation classify levels of vehicle autonomy from 0 to 5. Level 0 incorporates no automation; levels 1-3 have varying degrees of partial assistance to the driver, where the automobile, for example, can control steering, acceleration and deceleration, and even interfere with the driver. Finally, in full autonomy, level 5, the car drives on its own and makes all decisions and reactions to its surroundings.[1]

The automotive market uses a combination of sensors to make these critical decisions. Radar designs are the fastest growing sensors in ADAS today, due to the longer-range capabilities and their resistance to all weather conditions.[2] This research will focus on radar designs, specifically long-range 77GHz radar, to showcase how automotive materials are changing and, through the choice of alternatives to those conventionally used in the space, how product life and reliability can be enhanced.

## Basics of Construction

Circuit board materials. Starting with the backbone of the design, the system requires transmission and reception of radio waves through antennas to gather information on objects around the vehicle. This is made as exposed metal circuits on a dielectric substrate material. The length and width of the trace are specifically defined for the frequency that will be used to propagate the signal. Close attention is paid to trace height, width and shape. The critical nature of this part requires the information that goes out and comes in as a signal is not lost or altered. To ensure minimal disruption, the antenna is created on a "low loss" substrate material. The term low loss refers to dissipation factor (Df), described in physics as a loss rate of energy of oscillation.[3] This is exactly the technology used in airplanes to inform pilots of their surroundings, especially when visibility is limited.

The European Telecommunications Standards Institute (ETSI) and Federal Communications Commission (FCC) developed regulations to phase out 24GHz use for automotive applications. These regulatory changes and the need for increased performance have caused a shift to 77GHz.[4] The increase in frequency requires a change to the substrate used. As frequency increases, more signal is carried on the outer edges of the conductor. This is known as skin effect. As a signal approaches the edges of the conductor, there is more opportunity for dielectric loss due to competing interactions within the design. This includes circuits in proximity to each other.

The 77GHz designs require enhanced low-loss dielectric materials to achieve the level of reduced loss over their 24GHz counterparts. In response, substrate suppliers created dielectric made of polytetrafluoroethylene (PTFE) that are ceramic-filled. These are designed to have specific electrical stability, very different from the traditional resin-filled glass-weave substrates (FR-4) the automotive industry uses for other applications, including infotainment, body control or even engine control. Being in the radio-frequency range requires a very low dissipation factor. By comparison, the Df value of FR-4 is 0.20, while that of ceramic-filled PTFE is 0.002. Yet, there are challenges. These materials cost more and require altered fabrication processes. Due to the critical nature of the safety application, ceramic-filled PTFE is by far the most heavily used for 77GHz radar safety designs.

Polytetrafluoroethylene substrates are well established materials for military, aerospace and some telecommunications applications, but care should be taken when processing, especially when considering the volume these designs will approach as autonomy levels increase. The material is deformable, which means it can scratch or bend easily with handling. It is highly chemically resistant, requiring different cleaning and conditioning preparation steps prior to copper plating. Additionally, ceramic-filled PTFE has a very high porosity that can and will absorb solution throughout the PCB fabrication. Some chemicals will attach to fillers in the substrate. Special attention is to be paid to the process cycle parameters to successfully manufacture the precision required for antenna designs. It is recommended to follow the suggestions detailed by the substrate supplier.

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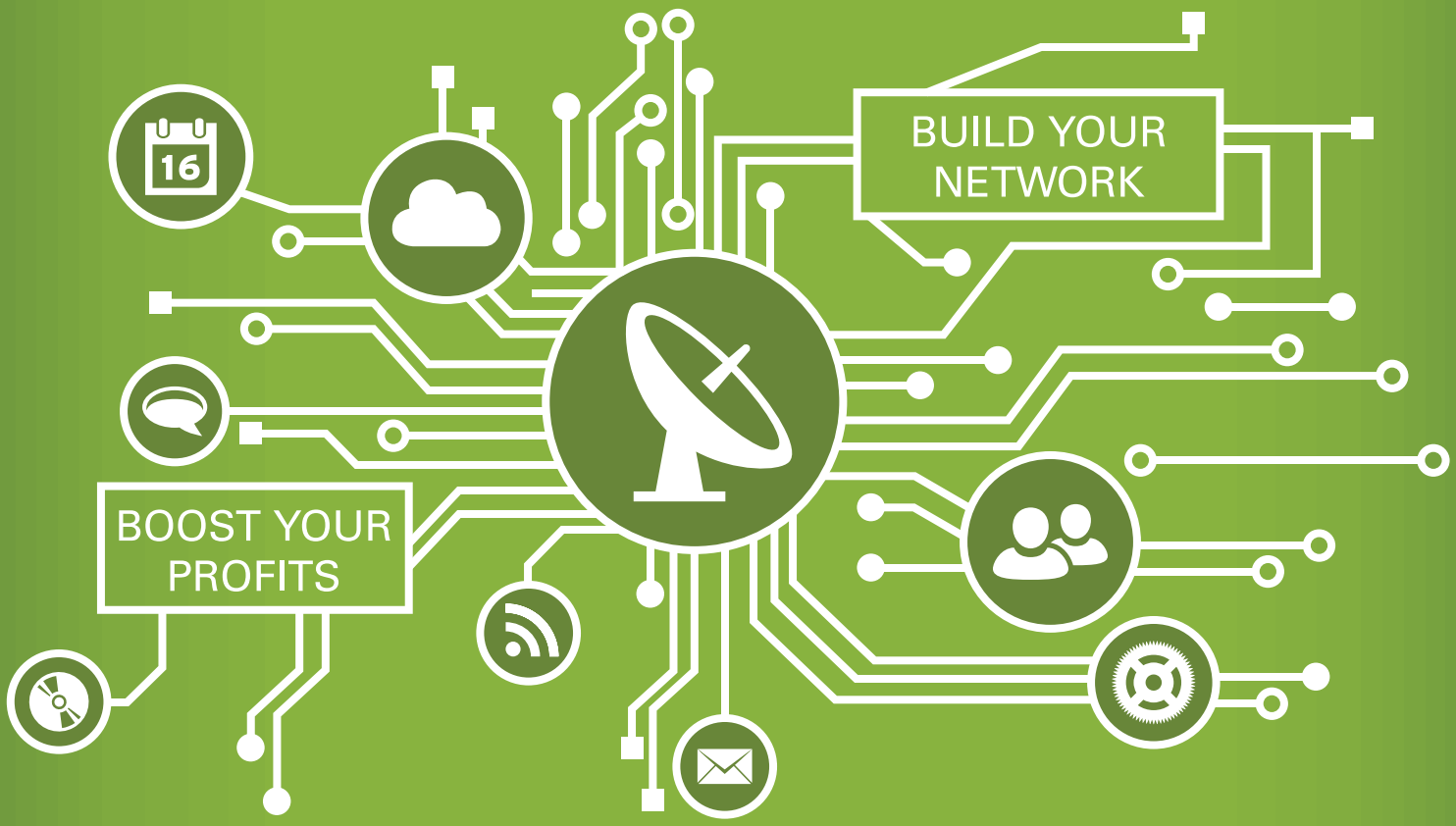


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The base material is the first source of loss associated with the design. A second opportunity for loss is on the conductor or the metal circuit formed as the antenna. The conductor in this work is copper. The fabricator receives the substrate as a thin layer of copper foil, which is printed and etched, then plated to the desired thickness with electrolytic copper plating. The width, height and roughness of that copper is important for signal propagation. The final step of the fabrication process is to coat the copper with a finish that will resist oxidation and preserve the rest of the design prior to assembly, protecting the exposed antenna in end use. Conductor loss can occur depending on the type of surface finish chosen. Here, the types of surface finishes and their effect on insertion loss will be discussed. The testing will determine if coating thickness plays a role in performance consistency.

Assembly materials. The function of an electronic system is driven by semiconductor packages attached to the surface of the PCB. (Details of the packages are discussed in the next section.) These components are joined to the circuit board using a solder alloy. Most assemblies are built by printing a solder paste, placing components on that paste, and conveying through a heated oven to create an intermetallic bond. During this process, flux material prepares the surface for attachment and is volatilized, leaving behind the metal alloy and certain flux residue. The resultant solder joint creates a mechanical bond and an electrical pathway between the component and PCB.

Historically, the automotive market primarily used SnPb solder. In 2010, regulatory changes pushed adoption of lead-free (tin-silver-copper or SAC) alloys.

The most obvious challenge for a solder alloy (in automotive applications) includes harsh operating conditions, as devices operate close to the engine and are exposed to extreme weather conditions. Concerns surrounding product life and reliability are directly connected to the environmental exposures and the expected high-performance processing and function required for life-critical functions.

It is well-documented that thermomechanical forces put stress on the solder joint. Heating the solder joint is realized in two ways, from the function of the design and/or the location of the systems. For example, devices close to the car engine can see operating temperatures approaching 150°C. Thermomechanical stress can result from multiple aspects, such as vibration of the unit or exposure to temperature fluctuations. The most common in all electronic systems is movement of dissimilar materials due to heat. The dissimilar rates of expansion between a stiff component and that of a PCB create a coefficient of thermal expansion (CTE) mismatch that degrades the solder joint over repetitive temperature cycles. Ultimately, the majority of stress from everything moving is directed to the solder joint, which then fractures, rendering a loss of electrical contact from component package to the circuit board.[5]

When an alloy is exposed to prolonged thermal or mechanical stresses, it will experience a deformation called creep. Creep will occur at elevated temperatures when the atoms are most mobile.[6] In the early 2000s, an industry consortium was created to address the challenges in automotive electronics as a result of greater environmental stresses and increased component performance needs. Car makers, tier ones, and material suppliers organized a consortium to develop new alloys that could improve thermal resistance, specifically thermal cycling, while maintaining SAC 305 reflow temperatures. The resulting alloy, Innolot, was patented in 2003 and comprised a SAC-based material with alloying additions to alter the microstructure and enhance creep properties at higher operating temperatures (TABLE 1).[5]

Alloy development incorporates four major areas of focus: solid solution strengthening, diffusion modifiers, grain refinement and precipitate strengthening. Differences in composition will result in microstructure difference, which in turn affect mechanical properties. This work will further illustrate that the Innolot solder alloy will extend the life of a product, even when exposed to significant thermal stresses. Testing will include the surface finishes examined in the insertion loss study mentioned above.

**TABLE 1.** Physical Property Comparison of SAC 305 and Innolot

| Physical Property | Units | SAC 305 | Innolot |
|---|---|---|---|
| Melting temp. range | °C | 217/221 | 212/220 |
| Thermal conductivity | W/mK | 62 | 55.2 |
| Specific heat | J/gK | 0.23 | 0.22 |
| Density | g/cm$^3$ | 7.37 | 7.46 |
| Hardness | VHN | 7 | 15 |
| Young's Modulus | GPa | 49.9 | 46.5 |
| **Tensile strength (25°C)** | **MPa** | **35.23** | **83** |
| **Yield strength (25°C)** | **MPa** | **23.2** | **60** |
| Elongation (25°C) | % | 33.5 | 17.8 |
| Tensile strength (150°C) | MPa | 15.7 | 23 |
| Yield strength (150°C) | MPa | 15 | 21 |
| Elongation (150°C) | % | 46.5 | 20 |
| **Creep elongation at rupture (150°C)** | **%** | **38** | **21** |
| **Creep rupture time (150°C)** | **Hrs.** | **9.1** | **18** |

Packaging materials. As mentioned, the function of any electrical system comes from the IC substrate packages. The final area of discussion for this work focuses on material changes to enhance the reliability of these components. In radar sensor designs, the components generate the radio frequency, direct the energy, and identify the information that is retuned. Moving from 24GHz to 77GHz brings greater resolution to the information gathered surrounding the car. The increased power and processing require a change to the chosen package. Designs supporting 24GHz use quad flatpacks that contained a low input/output (I/O) count, on the order of 32 pins.

The 77GHz designs require increased I/O and, with that, a transition to a ball grid array (BGA) package with about 180

connections. BGAs offer several advantages over leaded components, such as increased density, but without the concern for solder bridging during assembly and greater heat conduction. Heat can travel more easily to the PCB on a BGA. This decreases the heat experienced by the silicon chip during its operating life. Last, and likely most important for the 77GHz radar sensor, the BGA provides low inductance. The short distance between the package and PCB reduces signal loss or distortion.

This main BGA used to function the antenna is called an MMIC or monolithic microwave integrated circuit. In the construction, the die is attached to the substrate using a solder alloy or a conductive adhesive. The final portion of this study will investigate a thermal conductive adhesive attachment of die to the substrate as a tool for thermal management of the die. Pulling heat from the die will extended the package life. Thermal conductivity will be measured to understand the material differences. In addition to longer package life, adhesive is another avenue to eliminate lead in automotive designs. Highly filled silver adhesives, such as the hybrid silver sintering die used to attach materials, can offer performance benefits above and beyond solder materials.

One of the first areas of concern is getting a previously stored package through standard assembly processing. The defect of concern is delamination of the epoxy mold compound from reflow exposure. During storage, packages can absorb moisture prior to assembly. There is a risk the heat from reflow will volatilize the moisture, thereby putting pressure on the epoxy and pushing that epoxy from the rest of the package, resulting in a defect known as "popcorning."

All packages are rated on a moisture sensitivity level grading as documented by J-STD-020D, a moisture sensitivity classification for non-hermetically-sealed surface mount devices (**TABLE 2**).[7] End-users want to ensure components can be stored for an extended time prior to assembly and function reliably in the final build. Although more of a concern for leadframe packages, attention should be paid to all larger devices, especially for critical applications. This testing will ensure changes made for improved thermal transfer from the die will not adversely affect overall package construction.

## Automotive Test Conditions

The automotive industry has always relied on accelerated tests such as thermal cycling in air to predict the quality of a design and its model's ultimate product life expectancy. Principles derived from the Coffin-Manson equation enable predictive modeling of solder joint lifespan by accounting for the effect of plastic deformation of a material over a specified temperature range and dwell time.[6] The resulting equation predicts the rate of deformation of the solder joint will increase as temperature extremes become farther apart and cycle time increases. Radar designs serve a critical role in safety as the automotive industry moves toward complete vehicle autonomy. As such, the performance requirements of the devices are held to a higher standard. Market-defined levels for high- and low-temperature ranges are typically based on expected operating temperatures of the device. For example, interior systems are tested to a lower peak temperature than those for engine control, simply due to the operating environment. Safety systems such as radar start to blur the lines because they may or may not be located in harsh areas. Also, the duration or length of the accelerated tests have been increased for safety systems due to their critical nature.

To simulate the environments of automotive electronics, accelerated tests are used specific to functioning electronics. They include thermal cycling and sensitivity to moisture.

**TABLE 2.** J-STD-20D MSL Classification[7]

| | Floor Life | | Soak Requirements | | | |
|---|---|---|---|---|---|---|
| | | | Standard | | Accelerated | |
| Level | Time | Cond.°C/%RH | Time (hr.) | Cond.°C/%RH | Time (hrs.) | Cond.°C/%RH |
| 1 | Unlimited | <=30/85% | 168+5/-0 | 85/85 | n/a | n/a |
| 2 | 1 year | <=30/60% | 168+5/-0 | 85/60 | n/a | n/a |
| 2a | 4 wk | <=30/60% | 696+5/-0 | 30/60 | 120+1/-0 | 60/60 |
| 3 | 168 hr | <=30/60% | 192+5/-0 | 30/60 | 40+1/-0 | 60/60 |
| 4 | 72 hr | <=30/60% | 96+5/-0 | 30/60 | 20+0.5/-0 | 60/60 |
| 5 | 48 hr | <=30/60% | 72+5/-0 | 30/60 | 15+0.5/-0 | 60/60 |
| 5a | 24 hr | <=30/60% | 48+5/-0 | 30/60 | 10+0.5/-0 | 60/60 |
| 6 | TOL | <=30/60% | TOL | 30/60 | n/a | 60/60 |

**TABLE 3.** Thermal Cycle Test Conditions

| | | Duration (cycles) Requirements | | | | |
|---|---|---|---|---|---|---|
| | Test Condition | Powertrain | Body | ADAS | Chassis & Safety | Infotainment |
| Temperature cycling | -40°/150 °C | 2000 | | 2000 | 2000 | |
| | -40°/125 °C | | 2000 | 3000 | 3000 | 1000 |
| | -40°/105 °C | | | | | 1500 |

Test procedures. For this experimentation, each material change was tested separately to understand its full performance improvement or lack thereof. For a production build, it is recommended to test the parts both separately and as a full construction to understand improvements that can be realized for a specific application. To test the various levels of the PCBA, automotive industry methods were used. All reflow processes were held to the J-STD reflow profile, which is considered a more aggressive profile due to the long soak zone and high peak temperature. For all testing, a peak temperature of

250°C was used. Thermal cycling was tested against an aggressive thermal cycling profile of -40° to 160°C, with 10 min. dwell for 2,000 cycles (**TABLE 3**).

Surface finish effect on insertion loss. To understand insertion loss differences between surface finishes, the microstrip differential phase length method was used. Microstrip test vehicles created from a leading PTFE substrate material specifically used for 77GHz radar designs were fabricated in a production environment. The strips were processed in pairs measuring 50.8mm and 203.2mm (2" and 8") length, each having a width of 0.75". For ease of handling, the 5-mil thick PTFE-based material was adhered to an FR-4 backing layer for rigidity. The test vehicles were plated with the following production-available surface finishes: high-temperature organic solderability preservative (OSP), immersion silver (ImAg) and immersion tin (ImSn). Each finish was coated to both a thin and thick level following technical datasheet process parameters and conditions (**TABLE 4**). This was chosen to illustrate any effect of oxidation due to coating porosity for the OSP and immersion silver, or any influence of the immersion tin intermetallic compound growth. In addition to the microstrips, specific thickness coupons were added for separate thickness measurements based on the requirements for each surface finish. These included strip and UV absorption of the OSP, and coulometric reduction of the tin, to determine pure tin versus intermetallic compounds that may have formed under conditioning.

Factors:

- Surface finish: organic solderability preservative, immersion silver, immersion tin
- Coating thickness:
  - OSP 0.2 and 0.6µm
  - immersion silver 0.15 and 0.25µm
  - immersion tin 1.0 and 1.3µm
- Conditioning: two reflow exposures with 250°C peak temperature

Responses:

- Plated thickness: ultraviolet visible absorption, x-ray fluorescence and electrochemical reduction
- Growth of tin IMC – coulometric reduction analysis
- Appearance before and after conditioning – visible
- Insertion loss

After coating the surface finishes, thickness was determined on thickness test coupons using a UV dissolution method for the OSP, x-ray fluorescence for the silver and coulometric reduction for tin.

Microstrip parts and additional thickness coupons were sent to the Rogers Corp. research facility for insertion loss measurements before and after two exposures to a reflow profile with peak temperature at 250°C in a 7-zone convection reflow oven.

Insertion loss measurements were taken for each circuit across a wide range of frequencies on a Keysight model #N5251A millimeter-wave network analyzer. Insertion loss data were gathered as-coated and after two exposures to the reflow oven. Samples were then returned for post-reflow thickness measurements and appearance observation.

Solder alloy effect on solder joint integrity. The initial investigation of an alternate alloy to SAC in the early 2000s was to improve solder joint reliability for high-temperature applications. Although radar systems are not considered to have the highest operating temperature in a vehicle, they are tested to extreme peak operating conditions to effectively stress the solder alloy and distinguish its performance characteristics.

An active and passively monitored test vehicle was used for the solder joint integrity evaluation. The active test vehicle included 15 BGA-84 components daisy-chained for *in-situ* resistance measurements throughout the thermal cycle conditions. The second test vehicle consisted of passive components such as 1206 and 0805 resistors for shear strength testing measurements at defined intervals. Shear strength testing is a commonly accepted indicator of solder joint reliability, as it

**TABLE 4.** Plating Process Cycles

| OSP | ImAg | ImSn |
|---|---|---|
| Cleaner | Cleaner | Cleaner |
| Rinse | Rinse | Rinse |
| Microetch persulfate-based | Microetch persulfate-based | Microetch persulfate-based |
| Rinse | Rinse | Rinse |
| Precoat | Predip | Predip |
| OSP coating | Immersion silver | Immersion tin |
| Rinse | Rinse | Rinse |
| Dry | Dry | Rinse aid |
| | | Dry |

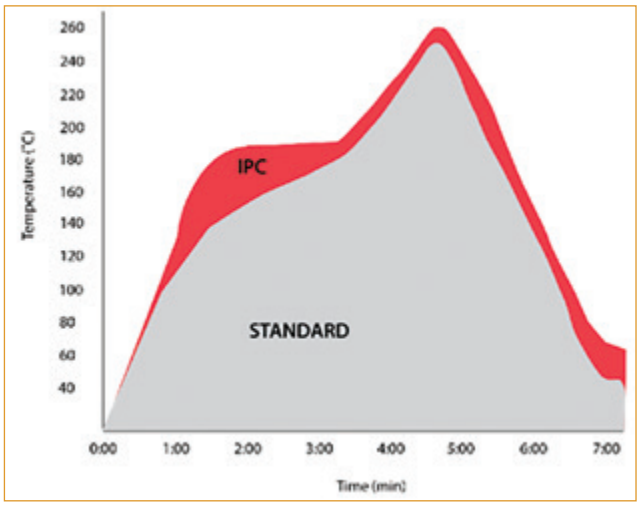


**FIGURE 1.** Comparison of standard reflow profile with soak zone to IPC profile with straight ramp.

relies on the assumption mechanical reduction of a solder joint over thermomechanical aging leads to failure of the electronic circuit. For this work, the same surface finishes used for insertion loss were tested in conjunction with the solder alloys. Only the upper thickness levels were used to reduce the test size. It should be noted this work only includes a portion of the fully executed solderability testing. More information can be shared upon request.

Factors:

- Surface finish:
  - organic solderability preservative (OSP) 0.6µm
  - immersion silver 0.25µm
  - immersion tin 1.3µm
- Solder alloy: SAC 305 and Innolot
- Reflow profile: 250°C peak temperature
- Thermal cycle conditions: -40° to 160°C with 10-min. dwell times at the extremes
- Conditioning prior to shear testing: 0, 1,000 and 2,000 thermal cycles at -40° to 160°C

Responses:

- Electrical resistance in excess of 20% of initial resistance for five consecutive readings per IPC-9701A
- Shear strength (kg)

In total, 15 components per test vehicle and three test vehicles (**FIGURE 2A**) per condition were measured. Including three surface finishes in the evaluation resulted in a total of 540 measurements taken. The BGA designs were arranged in a daisy chain to allow *in-situ* measurements. Failures were identified as a condition where electrical resistance of the device increased in excess of 20% of initial resistance for five consecutive readings per IPC-9701A.

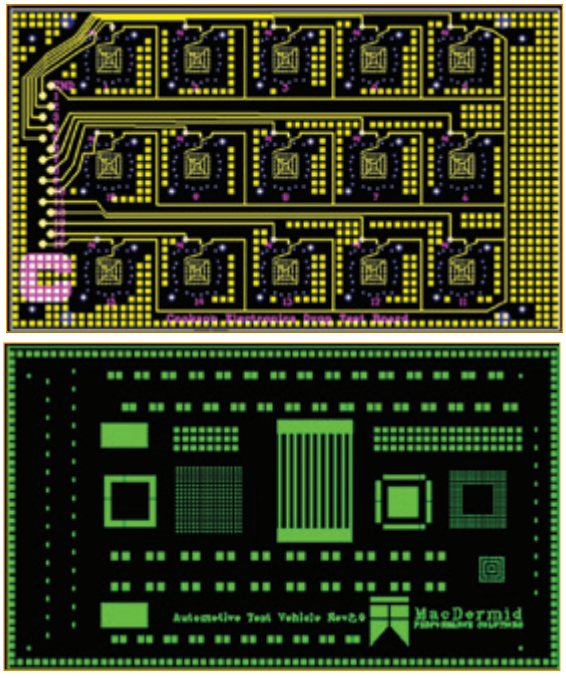

**FIGURE 2.** a) Thermal cycle test coupon containing BGAs. b) Automotive test vehicle for shear strength evaluation.

Shear strength was analyzed before and after 1,000 and 2,000 thermal cycles. Shear testing was executed on the 1206 resistor for the "automotive test vehicle" in **FIGURE 2B**. Parts were tested for high-speed shear (1,000µm/sec.) evaluation at 0, 1,000 and 2,000 cycles to estimate the effect of thermal cycling on solder joint strength. The test vehicle is an 8-layer board and includes multiple BGAs, LGA, MLF and resistors for evaluation.

**Material choice for enhanced thermal management from the die.** As device complexity increases and motor vehicles are asked to do more, the subsequent increased processing power leads to increased heat generated.[8] Removal of this heat from the die within the IC substrate will promote improved performance of the package and extended life. Standard ICs use materials that remove 2-10W/m-K. Today, greater thermal transfer is a necessity. For advanced safety systems such as the MMICs used in the radar designs, the desire is greater than 10W/m-K. It is common to use a thermally conductive adhesive for heat transfer from die to leadframe. A new thermal conductive adhesive available can be used with metal or substrate attachment. The material combines micron silver flake, thermoset resins and diluents to form the die connection.

To prove the performance of this material, thermal conductivity was measured at 175°C for a 60-min. exposure. Laser flash equipment was used to measure the thermal conductivity of the die attach material. The effective thermal conductivity (K-eff) is typically measured in a multilayer format. This enables the analyst to understand all factors of contact resistances at the interfacing surfaces.[9] A plastic BGA measuring 7mm x 7mm was used to test the performance of the thermally conductive epoxy in comparison to the conventional material. In a production environment, the material was inkjetted in an "x" pattern on the substrate, followed by die placement. The epoxy was cured at 175°C for 60 min. The die was then wire-bonded, and the package was completed with final encapsulation. Parts were analyzed by x-ray for any evidence of delamination after MSL 3 preconditioning.

## Results

**Surface finish effect on insertion loss.** In agreement with previous work executed by Rogers, the OSP and immersion silver resulted in the same insertion loss as the bare copper

**TABLE 5.** Insertion Loss Measurements at 77GHz

| OSP | As Coated (dB/in) | 2x Reflow (dB/in) |
|---|---|---|
| OSP 0.2µm | -1 | -1.05 |
| OSP 0.6µm | -1.03 | -1.02 |
| ImAg 0.15µm | -0.99 | -1.01 |
| ImAg 0.33µm | -0.99 | -0.99 |
| ImSn 1.0µm | -1.57 | -1.6 |
| ImSn 1.3µm | -1.6 | -1.77 |

control[10] when analyzing from 0 to 80GHz. The graphs for both finishes overlay regardless of coating thickness or reflow conditioning. Immersion tin had the greatest loss compared to the bare copper control, and as the frequency increased, the delta between the two became greater (**FIGURE 3**). Tin also showed a significant difference when comparing as plated to post-reflow conditioning.

When focusing on the 77GHz measurement, the insertion loss comparison between finishes becomes clearer (**TABLE 5**). The tin insertion loss is about 0.2dB/in greater than the bare copper, OSP and immersion silver. This might not be a concern for lower frequencies, but it becomes a concern for systems operating at higher frequencies. In addition, the thicker tin deposit has greater losses after reflow conditioning.

It is known immersion tin thickness changes with heat exposure, which is not a characteristic for OSP or immersion silver. Pure tin was measured on the same coulmetric equipment to determine thickness change after the two reflow conditions. Three readings per sample were taken to calculate an average. The sample initially coated with 1.0µm of pure tin averaged 0.2µm remaining, which results in an estimated intermetallic compound (IMC) layer of 0.8µm. The samples plated to 1.3µm had 0.35 remaining pure tin and an estimated IMC layer of 0.95µm. The changes in insertion loss could be attributed to the greater amount of IMC compound. Additional work will be done to get a more precise answer for why the tin performance is different with reflow conditioning.

Only the thin OSP coating displayed a change in appearance after reflow exposure. It can be described as a slight darkening with more iridescence. Even with the slight change in appearance, there was no detriment to insertion loss. Immersion silver did not experience any appearance change, and no change in insertion loss was observed. The immersion tin also did not display any visible appearance change, but the change in insertion performance was observed over the range of frequencies tested. Proper choice of surface finish is important at 77GHz frequencies.

Solder alloy effect on solder joint integrity. The strongest factor found to influence thermal cycle resistance was the solder alloy. For all surface finishes tested, the Innolot alloy exhibited the highest resistance to cracking and thus lowest propensity to change in electrical resistance over continual thermal cycles, outperforming the SAC 305 baseline by over 25% on average. The -40°/160°C range was specifically chosen to effectively evaluate the creep-resistant properties of the solder alloys. Given predictive modeling, lower temperature extremes would result in higher cycles to failure. Additionally, given the failure criteria as defined by IPC-9701A, a change in resistance of greater than 20% does not indicate the resultant device is no longer electrically functioning.

The interaction (**FIGURE 4**) and resulting Weibull plots (**FIGURE 5**) suggest minimal variation among the finishes, with immersion tin exhibiting the highest propensity to change in resistance. Results suggest the amount of free tin affects the failure rate due to continual exposure to higher temperature ranges. Further investigation of these results will be examined

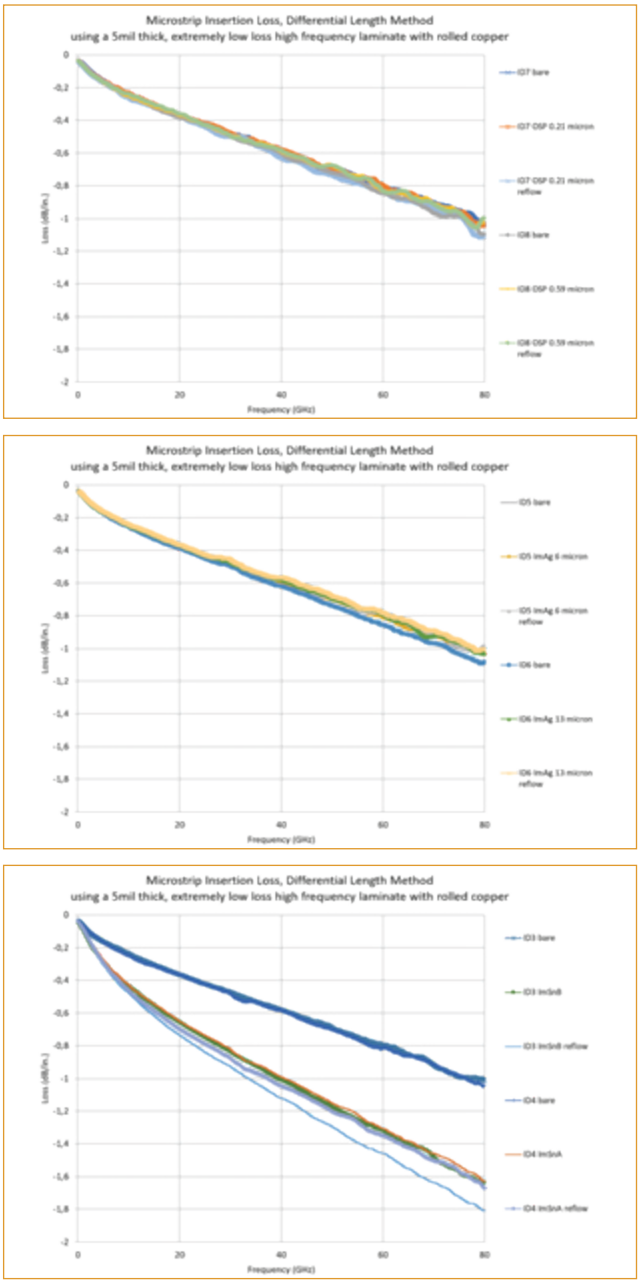


**FIGURE 3.** Insertion loss of OSP, ImAg and ImSn at two thickness levels and with and without reflow.

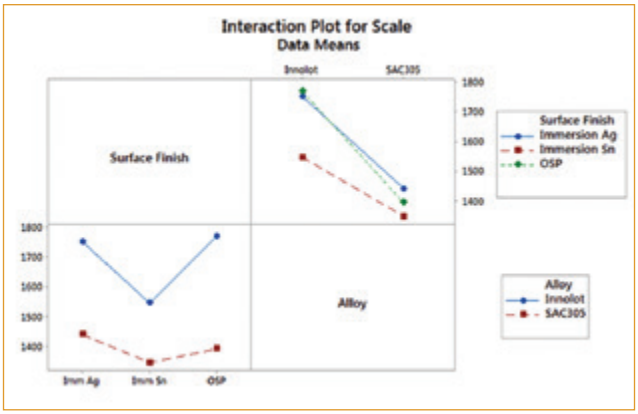


**FIGURE 4.** Interaction plots for thermal cycle testing.

in future work. The immersion silver and Cu OSP surface finish resulted in 63.2% of the parts tested passing resistance readings above 1,750 cycles, as illustrated by the Weibull plots for the Innolot alloy on the challenging thermal cycle profile described above.

The passive component test vehicle results aligned with the results seen on the actively monitored BGA devices. As expected from the sum of squares calculation, shear strength of both alloys was affected most by the number of temperature cycles (**FIGURE 6**). However, the Innolot solder alloy exhibited the lowest rate of shear strength reduction over 2,000 thermal cycles relative to the SAC 305 baseline. The results indicate the design of the Innolot alloy is more resistant to mechanical reduction over the number of temperature cycles. Similar to the active device test vehicle, shear strength was found to be consistent across each of the surface finishes evaluated (**FIGURE 7**). In each of the instances, a tin-rich Cu6Sn5 intermetallic is formed. Ultimately, regardless of alloy or surface finish, the largest rate of reduction in shear strength occurs between 0 and 1,000 thermal cycles, with the Innolot alloy maintaining a significantly higher shear strength over 2,000 cycles relative to SAC 305.

Thermal management of die. Bulk conductivity does not accurately predict the thermal resistance of a package. It does not consider interfacial resistance between the die and adhesive. The previously developed "effective" conductivity test resulted in a dramatic improvement from the high silver and hybrid silver adhesives. Compared to a conventional epoxy die attach, the hybrid silver sinter material showed was almost three times greater, at 14W/m-K compared to 5W/m-K (**FIGURE 9**). As this was demonstrated on a bare silicon die, another advantage is realized compared to leaded solder materials and eutectic gold-tin. It does not require back-side metallization.

A PBGA measuring 7mm x 7mm was used to test MSL resistance at 260°C. Parts were checked by x-ray for delamination after preconditioning to MSL 3 exposure. No evidence of delamination or voiding was observed (**FIGURE 10**). The new adhesive does not pose a threat to the required epoxy mold adhesion.

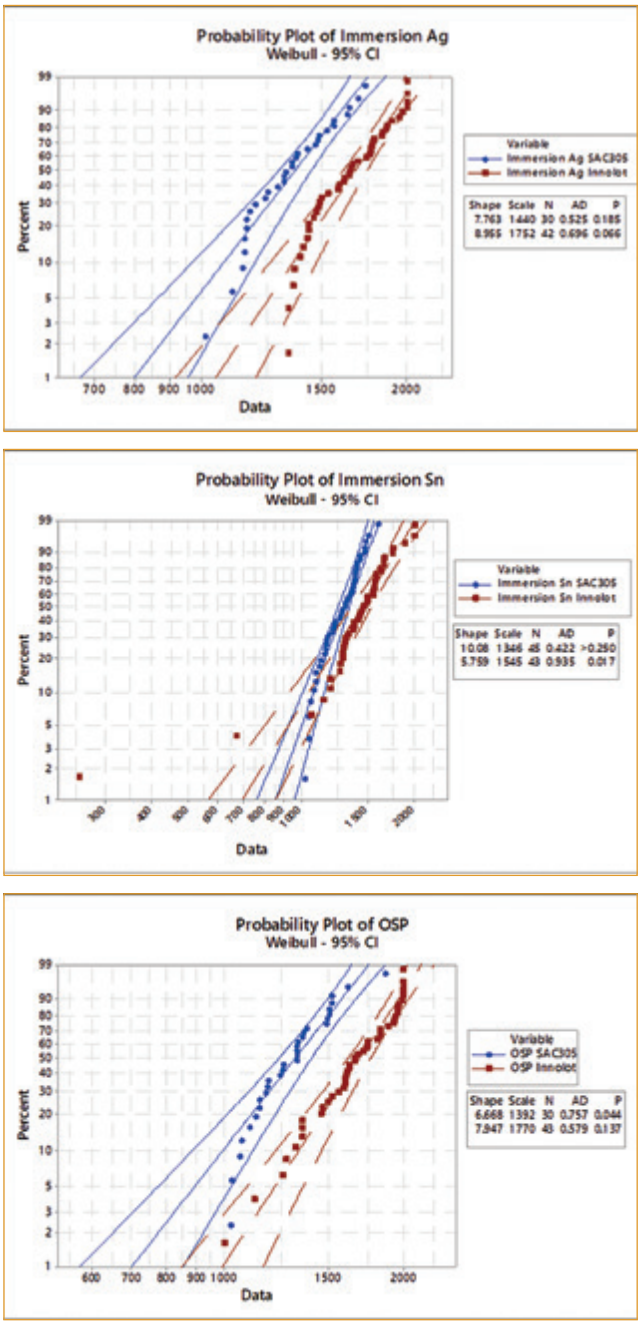


**FIGURE 5.** Weibull plots for thermal cycle testing.

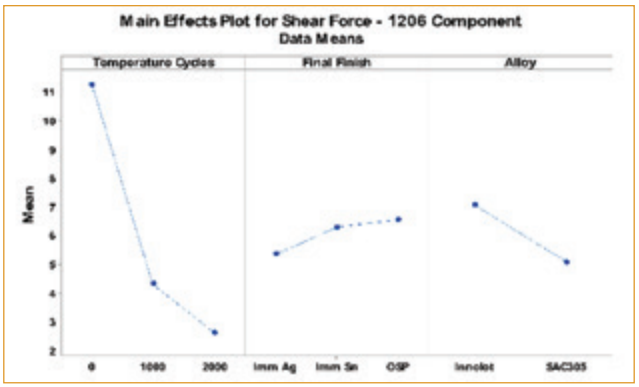


**FIGURE 6.** Main effects plot for shear strength.

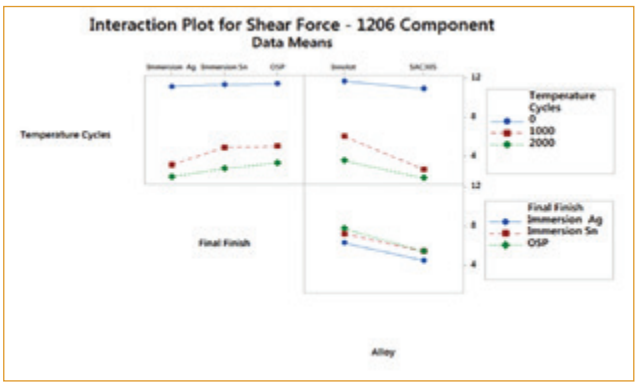


**FIGURE 7.** Interaction plots for shear strength.

## Conclusions

Significant advances are happening in the automotive space to deliver greater safety to passengers and pedestrians around the vehicle. These enhanced safety requirements utilize specialized technologies with enhanced requirements to achieve success. As this research demonstrates, it is imperative the proper surface finish be chosen for high-frequency applications. Enhanced solder alloys such as Innolot are a requirement to withstand the aggressive thermal cycle conditions required for advanced safety. Innolot in this testing shows a dramatic increase in thermal cycle resistance with superior shear strength. Finally, the hybrid silver sintering adhesive will also extend product life by improving the thermal transfer away from the die.

Each of these materials provides improvements over the incumbent but could realize even greater improvement when used together in one design. It is critical to test individual material changes, as well as those combined in the final design build for a complete understanding of end-use life and performance.

## Acknowledgments

This work was a group effort. I'd like to extend appreciation to all those involved, including the MacDermid Alpha circuitry, assembly and semiconductors groups, the Rogers' team and my marketing team for all their help.

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## REFERENCES

1. Synopsys, Dude, Where's My Autonomous Car? The 6 Levels of Vehicle Autonomy, company paper, synopsys.com/automotive/autonomous-driving-levels.html.
2. Avinash Kondepaddy, Why Are Automotive Radar Systems Shifting to 77GHz, Mar. 25, 2019, company paper, pathpartnertech.com/why-are-automotive-radar-systems-shifting-to-77ghz.
3. Wikipedia, retrieved May 11, 2020, wikipedia.org/wiki/dissipation_factor.
4. John Coonrod, "Understanding When to Use FR-4 or High-Frequency Laminates," IPC Apex Expo, April 2011.
5. Harry Bhdeshia and Mike Ashby, "The Creep of Solder," 2004, phase-trans.msm.cam.ac.uk/2004/creep.practical.pdf.
6. Craig Hillman, Ph.D., Reality of New, High Reliability Solders, DfR monthly webinars, Feb 24, 2016.
7. IPC J-STD-020D, "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices," August 2007.
8. Cypress Semiconductor application note, Understanding Temperature Specifications: An Introduction, cypress.com/file/38656/download.
9. H. H. Jin, S. Kanagavel and W.F. Chin, "Novel Conductive Paste Using Hybrid Silver Sintering Technology for High Reliability Power Semiconductor Packaging," ECTC, June 2014.
10. John Coonrod, "The Impact of Final Plated Finishes on Insertion Loss for High Frequency PCBs," SMTA International, September 2017.

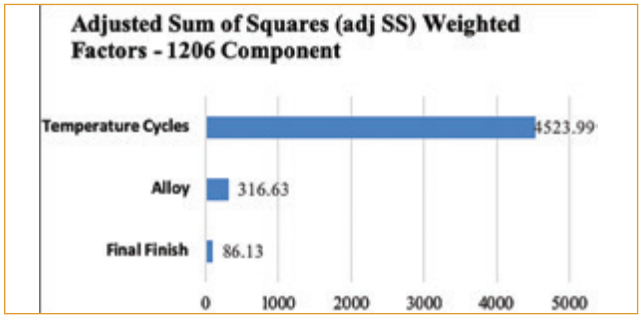


**FIGURE 8.** Sum of squares for shear strength.

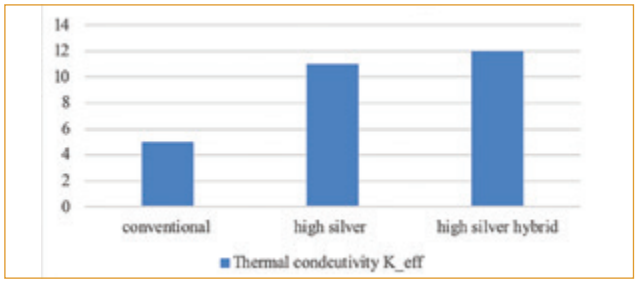


**FIGURE 9.** Effective conductivity comparison, in W/mK.

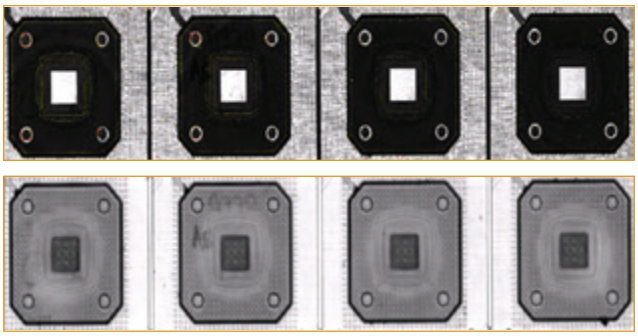

**FIGURE 10.** X-ray images to determine adhesion loss.

*continued from pg. 29*

standards could be extended beyond 50Gb/s per channel. Electrical connectors for printed circuit board and cable communication delivering low insertion loss, flat impedance profiles and minimal crosstalk will maximize the reach of the copper interconnect at an acceptable bit error rate. How quickly higher speeds will be adopted depends on the ability to equalize the channels in the existing power envelope while the channel cost-performance as measured in $/Gb/s is reduced over time. The cost-performance is strongly impacted by bandwidth density. Bandwidth density can be channels x Gb/s/channel per unit area for a package on a PCB or channels x Gb/s/channel per unit length for edge-card interconnection. The required ground pins that shield signals and provide a continuous return path will increase the effective number of pins per channel. So, even in cases where the channels per unit area or channels per unit length are constant, the number of pins may increase to effectively shield the signals.

Reduced dielectric loss materials are increasingly used for high-speed electrical channels, and the demand for those materials will increase as speeds above 50Gb/s per channel are adopted. However, low-loss/ultra-low-loss electrical channels also require attention to processing and design of all the elements of packages and PCBs. Copper roughness, via stubs, antipad size and shape, and internal via and PTH design are all as important as the loss characteristics of the dielectric material. Coreless packages and thin laminates for improved via and PTH design will reduce discontinuities significantly for high-speed channels. The footprint at the electrical connector will require special design rules to avoid becoming a bandwidth limiter in package-to-board, -backplane or -cable interconnections. This footprint design includes via or PTH diameter, length and stub, antipad size and shape and routing escapes from the vias, or PTH and land sizes.

Reference plane gaps, holes and interconnection to PTHs that create return path discontinuities are part of the channel design.

To efficiently address these technology challenges, power efficiency must also continue to improve. The channel shielding requirements demand more layers and vias for the high-speed channel. Improving power efficiency demands lower impedance power distribution for less loss through $I^2R$ loss and less inductance for faster regulation. This creates a trend toward more metal and placing regulation closer to the loads competing with the short reach signaling and increased signal shielding. These trends also leverage the advanced packaging concepts of TSV, SiP and PoP and help drive the economics to adopt this technology. In addition, increasing processor power, increased memory channels, and higher-end PCIe end-point cards like FPGAs/discrete GPUs all lead to much higher power needs at the node and rack levels. 48V to the node is being investigated to enable higher efficiency for higher power racks, and higher frequency VRs are being investigated to deliver the power distribution network to the higher-powered compute elements. DDR5 memory has power management integrated circuits (PMICs)/VRs integrated on the DIMMs.

## High-End Systems Webinar

Join iNEMI on Jun. 17 to review highlights of the High-End Systems roadmap. This webinar, part of a series of roadmap webinars iNEMI is hosting, will share key trends and technology challenges identified in the chapter. For additional details and to register: https://community.inemi.org/ev_calendar_day.asp?date=6/17/2020&eventid=334 ❑

**KARTIK ANANTH**, senior principal engineer, Data Platforms Group, Intel, and **DALE BECKER**, chief engineer, System Electrical Design for IBM, are chair and co-chair, respectively, of the iNEMI High-End Systems Product Emulator Group (PEG).

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*Compensation, continued from pg. 28*

designs each year (55%), up from the prior survey (44%) (**FIGURE 7**). Fifteen percent produce 11 to 15 designs per year, and another 15% produce 16 to 20. Some 16% said they produce more than 20 designs each year, up from 13% in the prior results.

Designers primarily design for these end-markets:

- Government/military/aerospace/avionics/marine/space: 23%
- Industrial controls/equipment/robotics: 17%
- Automotive/other ground vehicles: 9%
- Consumer electronics: 9%
- Medical/optoelectronics and equipment: 9%
- Electronic instruments/ATE design and test: 9%
- Communications/related systems equipment: 8%
- Computers/peripherals: 4%
- Semiconductors and related packaging or test equipment: 4%
- Other: 8%

Challenges. The biggest challenge designers face in 2020 hasn't changed from early last year: workload (59%). However, keeping up with technology changes (43%) and finding/keeping one's job (24%) received more responses than in the late 2018 survey, while outsourcing fell (15%).

The salary curve is likely tied to the larger numbers of younger design engineers responding to this year's survey. It's also a fair prediction 2021 data will reflect representation of even more young, inexperienced designers, as the departing generation continues to leave the field for some much-needed R&R. With a growing population of educated electrical engineers becoming aware of career options in PCB design, there's a solid chance the industry will see an influx of creative, eager minds–maybe gaining momentum after the world overcomes the Covid-19 pandemic. What the industry and overall economy will look like post-vaccine remains to be seen, but we have reason to be hopeful.

For additional figures and tables, see the online version. For a look at past surveys, click here. [https://www.pcdandf.com/pcdesign/index.php/menu-research/menu-market-data/8452-pcb-designer-salary-surveys]. ❑

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# Belts Be Gone and Other New Approaches to Print Stability

Do thinner boards require a different transport mode?

JUST WHEN WE think we have reached the limit on shrinking substrate thicknesses, tighter pad spaces and higher component densities, the industry says, "Not so fast!" Today's mobile phone boards average a remarkable 0.6mm thickness, with as many as 1,000 components packed into a 20mm x 80mm space. Over the past five years, advanced equipment sets have accelerated transport, tooling, vision systems, inspection capabilities and platform controls, all of which have certainly made producing high-quality products with ultra-small dimensions possible. However, in the stencil printing world, even more may be required to ensure maximum board stability during the print operation.

Traditionally, the mode of transport – bringing the PCB or pallet into the machine – has been achieved on some form of rubberized belt. This will no doubt continue as the solution for the assembly line. Inside the printer, however, not only is the board brought into the machine on the belt, but the substrate is clamped to the belt to hold it stationary, present it to the stencil and print. This has worked very well for years and is fine for multiple product builds. For mobile phones and other handheld products, however, current and future dimensions dictate a new paradigm. What are 600µm-thick phone PCBs today likely will continue to get thinner and, even at their current architectures, are susceptible to any type of undulation or extra pressure. Clamping thin, small boards or pallets to a rubber belt can result in movement, twisting or bowing at the substrate edges and potential print accuracy issues. There are flat belt options, which have been the interim solution for thin board printing, but the belts are still constructed from rubber and not completely rigid. Finally, belts are subject to wear; they eventually lose elasticity and require replacement. Without proper maintenance, even greater instability can occur.

To keep pushing the miniaturization envelope and remain high-accuracy print-capable, a novel approach to board stability during the print – i.e., the squeegee application of solder paste – has been developed. This off-belt printing solution has a radical new design. With this system, board transportation into the print platform is naturally managed with a belt system. However, when the substrate is raised to print height, instead of clamping to the belt, as in the conventional approach, the board is positioned on two flat metal surfaces engineered to extremely high degrees of flatness and coplanarity. The belt is removed from the material application operation, resulting in substrate rigidity and stability throughout the print cycle. This is designed to improve alignment and offer a highly stable presentation of the coplaned substrate to the stencil.

> "PCBs will get thinner and are susceptible to any type of undulation or extra pressure."

While clamping modification is one important element of ensuring substrate stability, the foundation for all system components – from cameras to understencil cleaning systems to the print head – must be robust to manage the multiple moving parts. The platform's rail system and frame structure require engineering that balances the speed and complexity of the process with ruggedness and capability to mitigate vibration for optimized printing. Almost counterintuitively, a tough, vibration-resistant frame does not always mean using the heaviest materials available. Controlling movement and providing a solid, motionless foundation necessitates sophisticated designs that marry durable materials with advanced joining mechanisms to deliver maximum stability. Frame systems for extreme high-accuracy semiconductor wire bonding platforms, as well as those that effectively support the high-speed movement and sudden stops inherent with placement systems, are increasingly being leveraged for new stencil printer designs to ensure stability for miniaturized assemblies.

Printing capability has come a long way in the past five years. Still, chasing that extra 5 or 10µm needed for current and future designs – something that once seemed aspirational – is now necessary. ▫

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# PCB Warping Causes and Prevention Strategies

Are your components in balance?

WARPING OF FLAT or planar printed circuit boards is a significant yet common problem when manufacturing and assembling PCBs.

Warpage can prevent pick-and-place machines from accurately placing components. Warpage can cause the lead-free wave solder machine to pick up solder and flood the board with solder. Even worse, a warped printed circuit may not fit in the case or cause problems with automated handling equipment (buffers, etc.).

A few items cause warpage, all known and preventable. The primary reason why a PCB will warp is uneven or imbalanced copper percentages in different layers. When a design is presented to a PCB manufacturer, the fabricator will run a check of the percentage of copper on each layer. This is to ensure the design is balanced; i.e., the copper plane percentages are even about the center. Consider, for instance, a typical 8-layer PCB. A copper power plane would be on layers 4 and 5 and signal layers on the remaining layers. The inner-layer 4-5 has an almost full copper percentage on both sides. The remaining layers are low-copper-percentage signal layers. The stresses locked in by lamination will even out or equilibrate.

When raw laminate is manufactured, the resin, glass fibers and copper are all compressed, heated, and cooled at the same time. Sheets of laminate are very flat when purchased, but they also have "locked-in" stress. The top and bottom copper foil has a lot of strength to control the movement of glass fibers and resin; this is called modulus. When the sheet is laminated at high temperatures, the glass fibers and resin move around somewhat and in different amounts based on their coefficient of thermal expansion (CTE). Also, the woven glass fibers are not necessarily of the same density in the x and y directions, often called *warp* in the x direction, and *weft* or *fill* in the y. Glass prepregs such as 2113 and 2116 have almost even numbers of fibers in both directions, whereas prepreg such as 1080 and 7628 have a larger, different number of fibers in the two different weaves. This means they move more in one direction than the other, creating the potential for warpage (**TABLE 1**).

For the lowest warpage, select 2113 or 2116 as the prepreg. When the glass fibers and resin are laminated with the copper sheets, each part of the package will have a wildly different CTE and modulus! Examples are shown in **TABLE 2**.

The copper exerts the stronger force of the three; the glass fibers are half as strong but only expand 1/3 the amount of the copper, so they are a controlling factor in the x-y axes only. The resin is the weakest as far as strength is concerned but expands three to 10 times as much. Copper is strong enough (modulus) to keep the glass fibers and epoxy in check. However, once etching removes a significant part of the copper, the locked stresses in the resin are released, which expands the PCB unevenly. The percentage of copper etched off will affect the amount each layer will expand, and thus cause warping of the PCB.

Processing a warped board is one of the biggest challenges in PCB assembly. A flat board that begins to warp will warp further as the heat of soldering releases pent-up stress inside the PCB. The single most significant reason for warpage is unequal thickness of copper layers not balanced relative to the center layer of the PCB. In multilayer boards, distributing copper area and weight equally around the theoretical centerline (middle) minimizes warpage.

The typical multilayer PCB is made of epoxy-glass laminate. The epoxy resin is subject to expansion and movement at temperatures above the glass transition temperature (Tg). This is acute during soldering operations, where the substrate is exposed to temperatures of 219° to 260°C. Various struggles are being fought inside the PCB as temperatures rise. The epoxy, which expands the most but with the least modulus (strength), will try to expand in all directions. The glass fibers and copper layers will use their lower CTE and higher modulus to restrict the epoxy expansion in the x-y directions. Therefore, the z-axis is relatively free to expand, which can result in some degree of warpage, sagging or bowing between corners.

**TABLE 1.** Warpage Tendency for Common Prepregs

| Prepreg Style | Warp Fill | Percentage Difference |
|---|---|---|
| 1080 | 23.6 x 18.5 | 1.27 |
| 2113 | 23.6 x 22 | 1.07 |
| 2116 | 23.6 x 22.8 | 1.03 |
| 7628 | 17.3 x 12.2 | 1.41 |

**TABLE 2.** CTE and Modulus Variations

| Material | CTE | Modulus (in GigaPascals) |
|---|---|---|
| Glass fibers | 3-6 ppm/°C | 60-80 |
| Resin | 58 to 200 (t/g) ppm/ °C | 0.7 to 4 |
| Copper | 17 ppm/°C | 115 |

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The copper percentage ratio of an imbalanced PCB design after etching for each layer is shown in TABLE 3. The second row of percentages shows the improvement after copper pouring.

In the typical example noted above, the original PCB design as supplied would have experienced more than 3% warpage. After the designer repaired the files using copper pour equalization, the distribution of copper among all dielectric layers becomes even about the center. The PCB will have 0.25% warpage, well within the 0.75% parameter in industry specifications.

The primary solution for minimizing PCB warpage is to use the correct copper weight and copper-etched percentage balance between dielectric layers and copper layers around the center in the PCB. For proper warpage control during the soldering and assembly process, use appropriate (and sufficient) clamp-down fixturing to hold the PCB flat during soldering. At the design stage, keep in mind component "balance" with regard to heat-producing components, i.e., how they are evenly distributed across the PCB assembly. □

**TABLE 3.** Copper Percentage Ratio of an Imbalanced Design Post-Etching

| PCB Design as Supplied | | | | PCB Design After Pouring to Equalize | |
|---|---|---|---|---|---|
| Layer 2 | 24% | Signal plane | Sum of layers 1-4 = 118 | 70% | Sum of 1-4 = 229 |
| Layer 3 | 15% | Minor signal place | | 70% | |
| Layer 4 | 23% | Signal plane | | 33% | |
| Layer 5 | 22% | Signal plane | | 26% | |
| Layer 6 | 76% | Ground plane | Sum of layers 5-8 = 226 | 76% | Sum of 5-8 = 230 |
| Layer 7 | 74% | Power plane | | 74% | |
| Layer 8 | 54% | BGA plane with ground areas | | 54% | |
| | Warpage: 3% | | | Warpage: 0.25% | |



# Incomplete PTH Reflow

## Is poor stencil design the culprit?

THIS MONTH WE illustrate solder balling and incomplete reflow when reflowing through-hole components with pin-in-paste.

Solder balling pin-in-hole reflow (PIHR) close to the body of the connector suggests poor design of the stencil for this application (FIGURE 1). There is no standoff on the corner of this part, which may have permitted the paste to be displaced when the component was attached. There should always be free space around the paste deposit to permit placement and reflow, without contacting the paste.

In any PIHR process, the board and assembly with the connector must be correctly profiled to ensure all the solder paste reflows into the plated through-holes. The center of the connector on the board will be the coldest part during reflow. The closer the pin is to the body of the component, the cooler it will be, as shown in FIGURE 2. At the right of the image, there is successful reflow and hole fill. Moving from center to the left, the paste has not reflowed completely and has not reflowed adjacent to the connector body. Makes a nice x-ray image!

We have presented live process defect clinics at exhibitions all over the world. Many of our Defect of the Month videos are available online at youtube.com/user/mrbobwillis. □

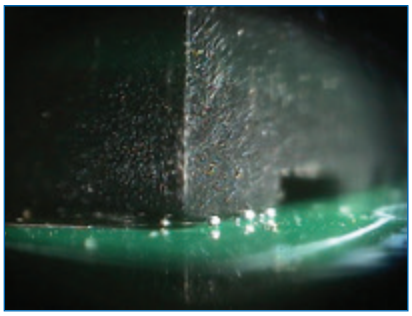

FIGURE 1. The presence of solder balls could mean poor stencil design.

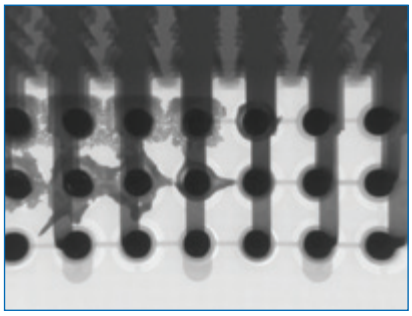

FIGURE 2. X-ray image showing paste reflowed at right but not at left.

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# Do X-Ray Inspection and Radiation Dose Damage Components?

Down the radiation rabbit hole!

INCREASED USE OF x-ray inspection throughout the component and PCBA supply chain to check the quality of optically hidden joints and features can elevate a component's level of radiation dose during assembly. A simple and sensible question, therefore, is can this cause any issues? For example, could this increase the risk of component failure, either a complete, temporary or intermittent failure, that happens during manufacture or potentially at some later time in the field? A sensible and simple question perhaps, but, unfortunately in my experience, one that generates many further questions and uncertain answers.

In general, the industry consensus, together with the reality that x-ray inspection has been widely used for years, is that for *most* components there is probably not an issue with the radiation doses likely during x-ray inspection. But here we enter our rabbit hole of additional questions: What constitutes the "not most" components?

This question may be clear for those end-users who specifically consider the performance of their boards when operating within an enhanced ionizing radiation background, such as in the military and aerospace arenas. Their in-house expertise will have already considered and mitigated the possible effects radiation dose may have on higher-risk components, and they can advise on appropriate protocols to follow throughout manufacture and test. In such applications, the radiation dose likely experienced during x-ray inspection will almost certainly be a tiny fraction of what the end-product will see during operation. For other applications, EMS companies and end-users are unlikely to be as well-versed in such knowledge. They might be reliant on component manufacturer datasheets for information on known issues from exposure to ionizing radiation, and, perhaps most important, to provide a maximum dose limit (for inspection and test). In my experience, such information does not readily appear.

Our question, then, becomes what components might potentially be at more risk and therefore experience a radiation dose during x-ray inspection that could affect behavior relative to normal operation? For our purposes, and for the vast majority of boards, I suggest the most probable class of devices to be considered includes those that store a charge, particularly silicon nodes. (My understanding is GaAs-based devices are much more radiation-hard and of less concern when exposed to the radiation doses likely during x-ray inspection.) This new question leads to yet more questions: What are the potential effects of this radiation on such devices, and what are the possible doses to which they will be exposed during inspection?

The literature suggests that if something were to happen from x-ray inspection radiation, it would be to potentially modify the stored charge at an individual silicon node (bit-flip). The issue we have when considering this is this failure process is statistical, specifically stochastic in nature, rather than deterministic. My understanding of this means that if it were deterministic, then doubling the dose would double the failure rate. However, as it is a stochastic process, doubling the dose increases the probability of a bit-flip failure, but that this increased probability is for all of the nodes in the batch of similar components, not just the component you have. In other words, you are increasing the chance for a (single?) bit-flip to occur on a specific device, but it might not be yours! From a practical point of view, if a bit-flip were to happen, is that a permanent failure? For example, could you reprogram a device after inspection, or avoid the potential effect by programming the device only after x-ray inspection? Or are any, or all, such issues unacceptable and therefore require the imposition of additional mitigation techniques in advance of any x-ray inspection (see later)? There may be other radiation-induced effects on these or other devices. The literature shows an increase in certain devices' background noise following x-ray inspection. However, comparing such investigations on individual devices to how they would actually be treated when assembled as part of wider board inspection is not clear and entirely application-specific.

If a bit-flip at a silicon node is what we should consider as a primary potential issue following x-ray inspection, then at what dose level to the component does this become statistically meaningful? Here our radiation rabbit hole adds further complexity: How do you measure the type and dose rate of the radiation falling on sensitive features during inspection? The units of radiation dose are also confusing in that there are two types.

First is the radiation-absorbed dose coming from a radiation source such as an x-ray tube. This is measured in Gy (Gray) or R (Roentgen); the latter, although not an SI unit, is still popular in many jurisdictions. Second is the effective dose, measured in Sv (Sieverts) or rad/rem (for the non-SI preferring jurisdictions). The effective dose accounts for the quality and type of the radiation that the receiving object/material is exposed to, as different materials can be more susceptible to the same level of incoming radiation (Gy/R). For example, if the human body is

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exposed to the same level of x-ray radiation dose (xGy), the effective dose to the lens of the eye (ySv) will be greater than the effective dose to the skin (zSv), as the lens of the eye is more radiation-sensitive. Similarly, for silicon, low-energy x-rays are more "effective" (i.e., silicon is more susceptible to them) than high-energy x-rays, and this effect is nonlinear across the x-ray spectrum. In a typical x-ray inspection system, the x-ray source (tube) produces "white" x-ray light, giving x-rays of all wavelengths up to the maximum kV setting. When you view the typical x-ray tube spectra used in inspection systems, it shows more low-energy x-rays are produced compared to high-energy ones. While this must be considered in dose calculations if the silicon in the at-risk device were open to the radiation directly, the reality is any device packaging, second-side components and board layers in the line of sight between the x-ray tube and the sensitive component will modify the "effective" x-ray spectrum to which the silicon is actually exposed. Most low-energy x-rays will be unable to penetrate any intervening material. Other points to consider when measuring the radiation dose/dose rate to sensitive components include the material of the measuring detector, the type of radiation used, and if the dose to a material is incremental or is "reset" for each inspection. If, for example, the radiation measurement detector used was an ionization chamber, air is the detecting medium, and the measured values it provides must be converted from dose (in air) to dose (in desired medium, for example silicon). This requires the use of appropriate, and potentially complicated and nonlinear with kV, conversion factors. The radiation type used for x-ray inspection is low-energy x-rays and not more energetic photons. Dose to silicon is cumulative so multiple inspection sequences will increase the chance for potential issues to occur as the "clock" is not reset at each inspection.

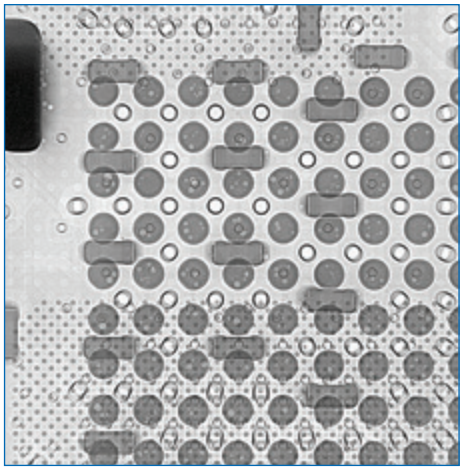


**FIGURE 1.** Lower magnification and therefore lower dose rate x-ray image.

With the complexity of the potential effects of radiation on components, the challenges of measuring the "effective" dose rate and the lack of knowledge of the actual radiation spectrum that our susceptible devices could be exposed to, we should also ask what level of dose is acceptable for the component to be exposed to during x-ray inspection? Outside of the necessary expertise for military and aerospace applications, where dose limits for certain components have been shared in published papers, such information is in my experience rare to see. Further, while such guidelines, where available, should certainly be considered as a "safe (?)" acceptable dose to be used during x-ray inspection, does that necessarily mean that for other non-military/non-aerospace applications a higher dose level is acceptable?

During x-ray inspection of a board, the dose rate/total dose (= dose rate x time of exposure) experienced by a specific component will also be affected by the x-ray system's configuration. In particular, this will involve how the image magnification is provided, the x-ray tube kV and power settings selected, and distance from the sample to the x-ray tube. The closer the device is to the point of origin of the x-rays (the focal spot), the greater the dose rate it will see. As x-rays are photons, if the device is moved away from the focal spot, the dose rate for the same x-ray tube kV/power settings will decrease by the inverse square law. Remember, the focal spot lies within the tube housing and not on the exterior tube surface. Therefore, the sample always has in-built separation from the focal spot.

For open and sealed-transmissive tube types, this minimum distance of the sample to the focal spot is ~0.5mm or less. For sealed tube types it is ~4mm or greater. Consider this variation when extrapolating any independently taken in-system dose rate measurements and using them for calculating a total dose estimation of a specific inspection sequence. For example, if an open tube has a 0.5mm minimum focal spot distance, the dose rate for a device (silicon?) placed 1.0mm away from the tube surface will be 1/9 (11.1%) the value compared to if the device were located at the tube surface. (That is, the inspection location is now 1.5mm from the focal spot, versus 0.5mm at the tube surface). If the sample was 2.0mm away from the tube surface, or 5x the distance from the focal spot compared to that at the surface, the dose rate at this point falls to 1/25 (4%) of the tube surface dose rate. This shows that deliberately moving the sample away from the x-ray tube during inspection will substantially reduce the dose rate/dose to which it is exposed. Put another way, the region of interest can be investigated longer before reaching the same possible critical dose limit. It also allows us to consider that while the entire sample is contained within the x-ray system for the entire duration of the x-ray inspection sequence, the contribution to the total dose a radiation-sensitive component will receive when other parts of the board are being inspected will be a very small fraction of the dose likely when it is being specifically examined, as it will always be much farther from the x-ray source. Of course, this will depend on the inspection sequence and yet may still need to be considered as a contribution to the total dose.

Moving the sample away from the tube will affect the achievable geometric magnification (GM), as the GM is the ratio of the distances (focal spot to sample) divided by the focal spot to detector. Therefore, to substantially reduce the dose rates during inspection, one approach is to sacrifice image magnification. However, if this means potential flaws can no longer be seen in the image, especially the smallest features, then use of x-ray inspection in the first place needs to be reviewed. Different x-ray systems have different sample

manipulation configurations for how the tube, detector and sample are moved, which may further exacerbate the reduction in available image magnification when deliberately moving the sample away from the x-ray tube. As an example, the x-ray images in **FIGURE 1** and **2** are of the same component at different magnifications but the same x-ray tube settings. The lower magnification (Figure 1) means the sample is exposed to a substantially lower dose rate when creating and holding the image for operator analysis. However, does it provide sufficient detail to see potential flaws in the smallest features compared to the more magnified, and therefore much higher, dose-rate-inducing pass (Figure 2)? As a mitigating technique, some x-ray systems may permit the x-ray tube to be blanked, or turned off, after the image has been captured, leaving the image onscreen for however long the operator requires for analysis but without adding to the dose experienced.

The effect of tube kV on radiation dose rates is more difficult to quantify, owing to the difficulty in understanding the spread of x-ray frequencies that actually reach a silicon die within a particular package. This is sample-dependent and changes because of absorption of the initial x-ray beam as it passes through a different thickness of intervening packaging and board material, as well as potentially through other components in the line of sight. Although lower kV radiation has a greater effective dose to silicon, I suggest examinations for all but the very thinnest of inspection objects are undertaken at 80-160kV and, as such, I would suggest to a first approximation changing the kV used for inspection has little or no bearing on dose rates experienced during inspection.

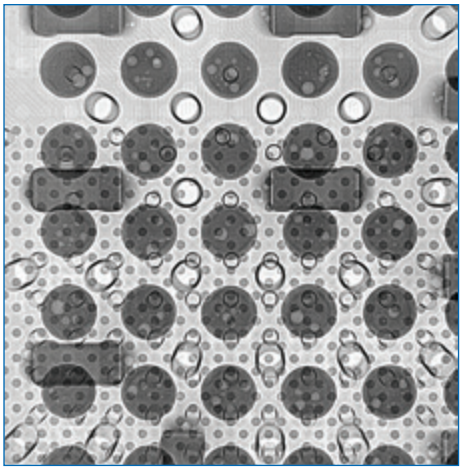


**FIGURE 2.** Higher magnification and therefore higher dose rate x-ray image.

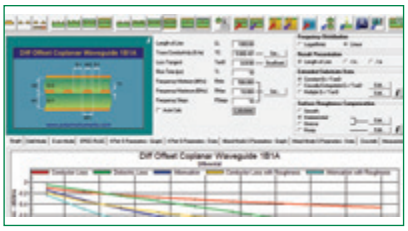
The effect of the x-ray tube power used during the inspection may be meaningful as, from my own experiments, dose rates scale linearly with power. Therefore, doubling the tube power used will double the dose rate experienced at the same sample position. Most x-ray systems now use flat-panel detectors (FPDs) rather than image intensifiers (IIs) to produce the image. FPDs typically require more tube power than IIs to produce a similarly contrasted image (without enhancements applied). Therefore, the increase in tube power used for this type of detector may be pertinent to the total dose a component could receive. To mitigate this issue, an x-ray system's image enhancement software functions could be used to modify fewer contrasted images created by the FPD at lower tube powers, yet still provide images that are "adequate for analysis" and may be worth considering as part of the inspection sequence.

Are you still with me down this rabbit hole? In terms of considering the impact radiation dose has during x-ray inspection, forewarned is forearmed. If you have component(s) that may be at risk, understand the potential failure modes that may occur; the issues that contribute to dose; and apply solutions for these, as well as other mitigating factors in your inspection regime. Here is my checklist of some of the questions to the question is there an issue with x-ray inspection and radiation dose? Please add your own!

- Do I have a radiation-sensitive component?
- Do I need to x-ray inspect it?
- What is the maximum dose this component can be exposed to?
- What are the dose rates at different distances away from the x-ray source in my inspection system, and how can I measure or calculate/estimate them for specific inspection sequences for potentially at-risk locations?
- Can I modify the inspection regime, such as by reducing the image magnification and/or the x-ray tube settings used and/or turning off the x-ray radiation when examining the images, yet still successfully analyze what needs to be seen?
- How can I minimize the total inspection time on the sample, yet achieve acceptable test coverage?
- Do I need to inspect more than once, or reinspect after rework, as the dose to silicon is cumulative?
- Could I apply additional filtration into the x-ray beam before it passes into the sample, thereby potentially modifying/reducing the lower energy x-ray spectrum from exposing sensitive locations?
- Should I consider using (lead) shielding on the board to protect the most sensitive components and/or collimating the x-ray source to prevent any additional dose to sensitive components when other parts of the sample are being investigated?

As you can see, the good, simple question of whether there are issues from the radiation dose of x-ray inspection leads to many other questions I believe must be considered. This topic may not be your wonderland today, but you might have to consider it in the future. If this becomes necessary, then ask the questions, consider the answers and use mitigation techniques, if appropriate, to reduce the dose rates and total dose to your products during x-ray inspection. ▫

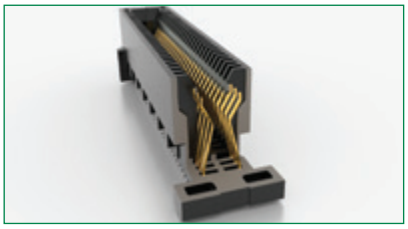
*Au.:* Images courtesy Peter Koch, Yxlon International.



## INSERTION LOSS CALCULATOR

Si9000e v. 20.03 contains extended substrate data library that allows user to enter tables of frequency vs. Dk and loss tangent. These tables can be associated with each substrate region for a given structure and are used during frequency-dependent insertion loss calculations. Larger capacity library; imports/exports individual material tables and complete library.

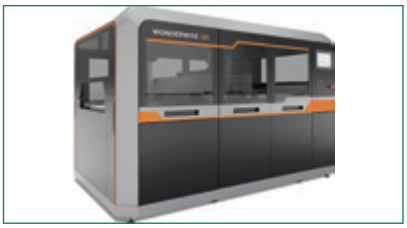
**Polar Instruments**
**polarinstruments.com**



## MICRO PITCH EDGE CARD SOCKET

Samtec HSEC8 incorporates higher-cycle edge rate contact. Edge rate contact system is high-speed; contact geometry is designed, simulated, and optimized for 50Ω and 100Ω systems. Is designed for more lead-in for mating PCB. Tips of contacts are hidden behind chamfered entry in plastic insulator, helpful when mating PCB has blunt edge. Comes in 40 to 200 positions; is PCI Express Gen 4 compatible; accepts 1.6mm-thick PCBs; comes with optional weld tabs. Is RoHS- compliant, lead-free solderable, and UL recognized.

**Samtec**
**samtec.com**



## COPPER SURFACE PREP MACHINE

Wonderwise 220 for horizontal inner-layer copper surface preparation can prepare copper surfaces on single side or both sides automatically. Plasma process achieves activation on copper for adhesion of light-sensitive films. Enables good wettability and adhesion. Footprint is 3 sq. m. Integrates into production lines, as copper sheets can be processed directly after preparation process.

**Wise**
**wisecompany.it**

## OTHERS OF NOTE

### ECAD-MCAD COLLABORATION

Altium 365 cloud-based design software allows collaboration among PCB designers, mechanical designers, part suppliers, and manufacturers. Works with Altium Designer 20. Allows sharing, visualizing, and markups of PCB designs at any time, on any device. Built-in co-designer capability between ECAD and MCAD domains (PTC Creo, Dassault Systèmes SolidWorks and Autodesk Inventor).

**Altium**
**altium.com**

### DRY-FILM PHOTORESIST

Riston DI3000 multi-wavelength, dry-film photoresist for pattern plating features high adhesion and chemical resistance. Eliminates lifting and breakdown defects in Cu, Sn or Au. Riston DI5100 film for mSAP processes is made for smooth copper high adhesion on isolated resist lines. Riston DI9200 HDI film for print-and-etch has high resolution and adhesion, and lamination conformation. Fast photospeed at multiple LDI wavelengths.

**DuPont Interconnect Solutions**
**dupont.com/electronic-materials.html**

### THERMAL INTERFACE CAPS

Sarcon caps are box-shaped and come in standard sizes to fit many transistors or can be custom-ordered to exact specifications. Installation takes seconds by sliding over heat-generating component. Dissipates unwanted heat to surrounding environment or nearby heatsinks.

**Fujipoly**
**fujipoly.com**

### POWER AL ELECTROLYTIC CAPS

BCcomponents 257 PRM-SI series reportedly offer up to 20% higher ripple current than previous-generation capacitors in case sizes up to 20% smaller, while providing useful life to 5,000 hr. at 85°C. Ripple currents up to 5.05A. Feature cylindrical aluminum cases, insulated with blue sleeves, and rated voltages to 500V in 25 case sizes ranging from 22mm x 25mm to 35mm x 60mm. RoHS-compliant.

**Vishay**
**vishay.com**

### BOUNDARY SCAN SOFTWARE

ScanExpress v. 9.6.0 includes test plan analytic data that may be saved to local database, exported to a file, or viewed using an included chart builder interface. Features integrated test plan data collection, including individual test execution time, test plan information, and individual test step results and diagnostics; data filtering and export for integration with other data systems; chart generation, display, and export.

**Corelis**
**corelis.com**

### VIRTUAL PROTOTYPE TESTING

PathWave Advanced Design System (ADS) now enables designers to perform pre-compliance testing on virtual prototypes of switched-mode power supply designs. Power Electronics Professional (PEPro) software now has radiated EMI capability as an add-on. Includes automatic setup and pre-built test benches, frequency-domain far-field analyses that mimic real-world tests, and comparison with government-mandated masks.

**Keysight Technologies**
**keysight.com**

## AUTOMATIC CRIMPER

CrimpCenter 64 SP has dual quick-change system. Can prepare new job while production is running, change applicators and terminals in 30 sec. and reportedly save more than 1 min. per terminal changeover compared to conventional methods. Offers application-specific default values for process parameters, automatic control of pneumatic pressure of feeding belts and gripper systems, straightening unit and roller design for thin cables.

**Schleuniger**
**schleuniger.com**


## REFLOW PROCESS MONITOR

OvenSentinel offers continuous reflow oven process monitoring down to the in-process zone, board and profile specification level. Measures in-transit boards in real time. Isolates issues and analysis of any potential yield infringement event to maximize known "OK" PCB output. Scalable.

**ECD**
**ecd.com**

## 'NO LIQUIDS' FLUXER

PlasmaFluxer uses cold-active plasma to melt micrometer-sized powder of adipic acid and deposit it on PCB. Liquid carrier material is reportedly not needed. Nitrogen is used to create plasma flame. Aerosol formed from meltable flux particles and nitrogen is led into plasma flame and directed to PCB surface. Once aerosols touch surface, particles solidify and form long-term coating. Substitutes wet-chemical flux activation with dry process. Soldering results are reportedly comparable to standard liquid fluxes.

**Seho**
**seho.de**

## OTHERS OF NOTE

### LED ICT/FCT

TR5001 SII LED series is an in-circuit and functional tester dedicated to LED lighting. Offers multicore parallel testing with up to four independent cores, plus quick disconnection interface with built-in auto-calibration and self-diagnostics. LED analyzer offers simultaneous LED testing for color and brightness for up to 1080 LED channels. Reportedly reduces operators' reinspection.

**Test Research Inc.**
**tri.com.tw**

### HERMETIC PACKAGE PROTECTANT

Staydry Z20 is a silicone film moisture getter for hermetic packages. Has backing adhesive that meets outgassing and adhesion testing for aerospace, telecom and medical applications; meets MIL-STD-883K, Method 5011.6. Employs silicone polymer for transmission of water into active desiccant matrix dispersed within polymer. Active desiccant allows high percentage of water to be absorbed and trapped inside silicone matrix. Adheres to most substrates, including metals, plastic and glass. Is available in easy peel form.

**MacDermid Alpha**
**MacDermidAlpha.com**

### INSPECTION BACKLIGHT

Universal LED Backlight HD-127 has intensity adjustment control. Slim light panel with homogeneous white light is intended for bright-field illumination of inspection objects. Features 6200K color temp.; contains LED light sources mounted across diffuser with protecting glass for uniform and soft illumination. Is designed into aluminum housing with 4 x 5mm mounting slots.

**Inspectis**
**inspect-is.com**

### LOW-VISCOSITY BLACK EPOXY

EP42-2LV Black is a two-part epoxy with low viscosity and good flow, for bonding, sealing, coating and casting. Viscosity of mixed system is 1,000-2,000cps. Working life of 60 to 90 min. per 100g batch. Cures optically opaque at room temp. in 2 to 3 days or at elevated temp. of 200°F in 2 to 3 hr.

**Master Bond**
**masterbond.com**

### LARGE CABINET X-RAY

GenX-90P and GenX-130P accommodate PCB sizes up to 21" (533mm) x 17.5" (445mm) with oblique angle viewing up to 70°. Accommodate 90kV or 130kV x-ray sources. Are upgradable from 90kV to 130kV. Detector is field-upgradable. Configurable with many sizes of FPDs or versatile image intensifier.

**PDR Americas**
**pdr-rework.com**

### THERMALLY CONDUCTIVE GEL

Bergquist Liqui-Form TLF 6000HG is a thermally conductive, dispensable gel that offers stable viscosity in storage and use. Accommodates gaps up to 3mm. Pre-cured formulation requires no mixing or refrigeration. Exhibits no material cracking or degradation in thermal conductivity after 1,000 hr. of thermal cycle testing.

**Henkel**
**Henkel-northamerica.com**

# In Case You Missed It

This column provides abstracts from recent industry conferences and company white papers. Our goal is to provide an added opportunity for readers to keep abreast of technology and business trends.

## 3-D Printed Electronics

"Charge-Programmed Three-Dimensional Printing for Multi-Material Electronic Devices"

*Authors:* Ryan Hensleigh, *et al.*

*Abstract:* 3-D printing can create complex geometries that could be of use in the development of electronics. However, the approach is mainly limited to nonfunctional structural materials, and the 3-D printing of electronic devices typically requires multiple process stages of embedding, spraying and writing. Here, the authors report a 3-D printing approach that can volumetrically deposit multiple functional materials within arbitrary 3-D layouts to create electronic devices in a single step. The approach prints 3-D structures with a programmable mosaic of distinct surface charge regions, creating a platform to deposit functional materials into complex architectures based on localized electrostatic attraction. The technique permits selective volumetric depositions of single metals and diverse active material combinations, including ceramic, semiconducting, magnetic and colloidal materials, into site-specific 3-D topologies. To illustrate the capabilities of the approach, the authors used it to fabricate devices with 3-D electronic interfaces that can be used for tactile sensing, internal wave mapping and shape self-sensing. (*Nature Electronics,* Apr. 6, 2020; nature.com/articles/s41928-020-0391-2)

## Memory Transistors

"Bioinspired Bio-Voltage Memristors"

*Authors:* Tianda Fu, *et al.*

*Abstract:* Memristive devices are promising candidates to emulate biological computing. However, the typical switching voltages (0.2-2V) in previously described devices are much higher than the amplitude in biological counterparts. The authors demonstrate a type of diffusive memristor, fabricated from the protein nanowires harvested from the bacterium *Geobacter sulfurreducens,* that functions at the biological voltages of 40-100mV. Memristive function at biological voltages is possible because the protein nanowires catalyze metallization. Artificial neurons built from these memristors not only function at biological action potentials (e.g., 100mV, 1ms) but also exhibit temporal integration close to that in biological neurons. The potential of using the memristor to directly process biosensing signals is also demonstrated. (*Nature Communications,* Apr. 20, 2020; doi.org/10.1038/s41467-020-15759-y)

## Noise Control

"Electromagnetic Interference (EMI): Measurement and Reduction Techniques"

*Authors:* Phalguni Mathur and Sujith Raman.

*Abstract:* This review presents both EMI measurement techniques and EMI reduction techniques in detail. EMI measurement techniques are presented under two sections that deal with emission testing and immunity testing, respectively. EMI reduction techniques are presented under four sections, with electromagnetic shielding given special attention under which various methods used by the scientific community to measure the shielding effectiveness of a material or microwave absorber and its application in EMI reduction are illustrated. This is followed by EMI filters, circuit topology modification and spread spectrum. (*Journal of Electronic Materials,* February 2020; doi.org/10.1007/s11664-020-07979-1)

## Wearable Sensors

"A Tailored, Electronic Textile Conformable Suit for Large-Scale Spatiotemporal Physiological Sensing *in vivo*"

*Authors:* Irmandy Wicaksono, *et al.*

*Abstract:* The rapid advancement of electronic devices and fabrication technologies has further promoted the field of wearables and smart textiles. However, most of the current efforts in textile electronics focus on a single modality and cover a small area. The authors have developed a tailored, electronic textile conformable suit (E-TeCS) to perform large-scale, multimodal physiological (temperature, heart rate, and respiration) sensing *in vivo*. This platform can be customized for various forms, sizes and functions using standard, accessible and high-throughput textile manufacturing and garment patterning techniques. Similar to a compression shirt, the soft and stretchable nature of the tailored E-TeCS allows intimate contact between electronics and the skin, with a pressure value of around ~25mmHg, allowing physical comfort and improved precision of sensor readings on skin. The E-TeCS can detect skin temperature with an accuracy of 0.1°C and a precision of 0.01°C, as well as heart rate and respiration with a precision of 0.0012m/s$^2$ through mechano-acoustic inertial sensing. Knit textile electronics can be stretched up to 30% under 1,000 cycles of stretching without significant degradation in mechanical and electrical performance. Experimental and theoretical investigations are conducted for each sensor modality, along with performing the robustness of sensor-interconnects, washability, and breathability of the suit. Collective results suggest E-TeCS can simultaneously and wirelessly monitor 30 skin temperature nodes across the human body over an area of 1500 cm$^2$, during seismocardiac events and respiration, as well as physical activity through inertial dynamics. (*npj Flexible Electronics;* Apr. 23, 2020, nature.com/articles/s41528-020-0068-y)

# THINK SMALL

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