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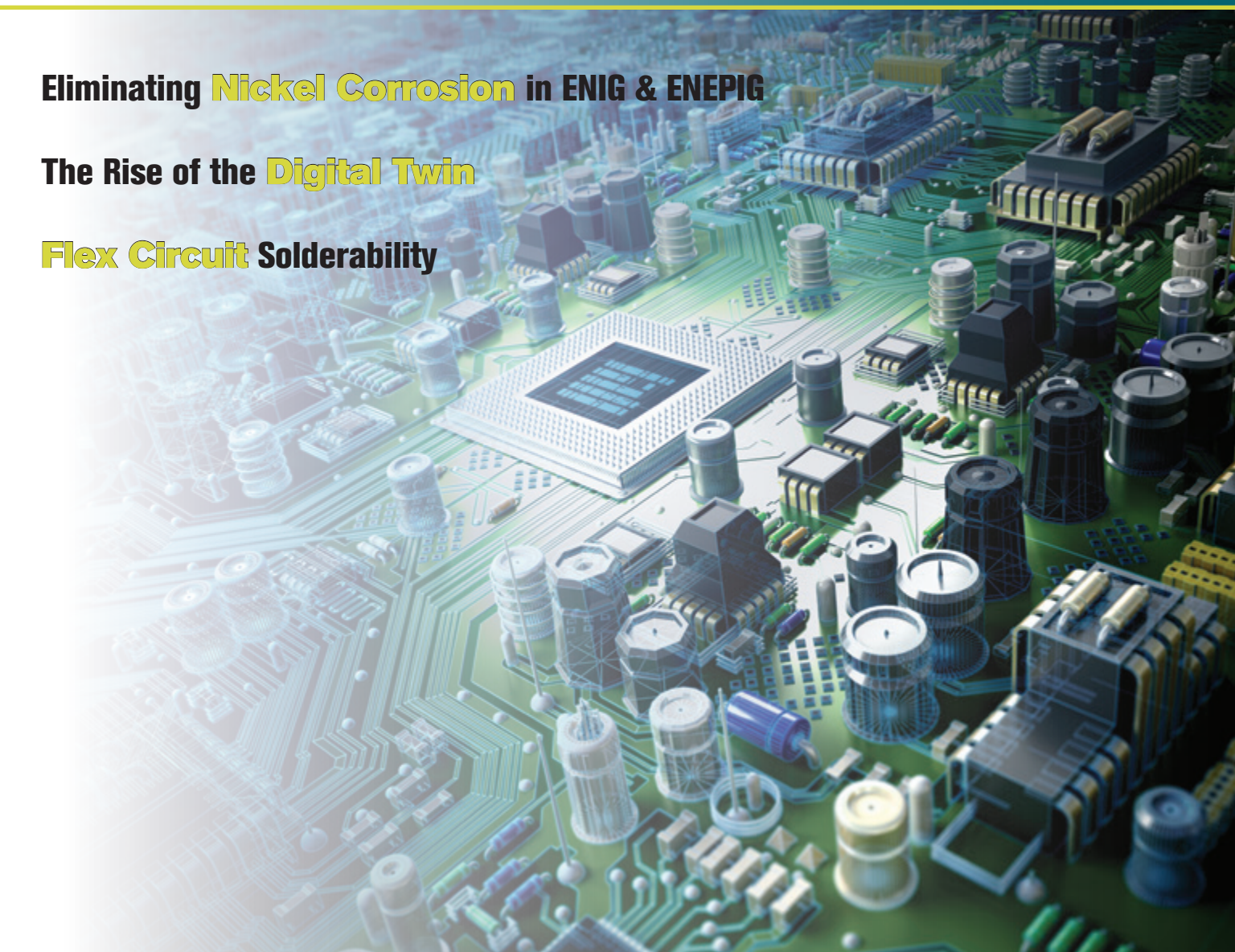
December 2019

Routing Automation & Design Reuse

Eliminating Nickel Corrosion in ENIG & ENEPIG

The Rise of the Digital Twin

Flex Circuit Solderability



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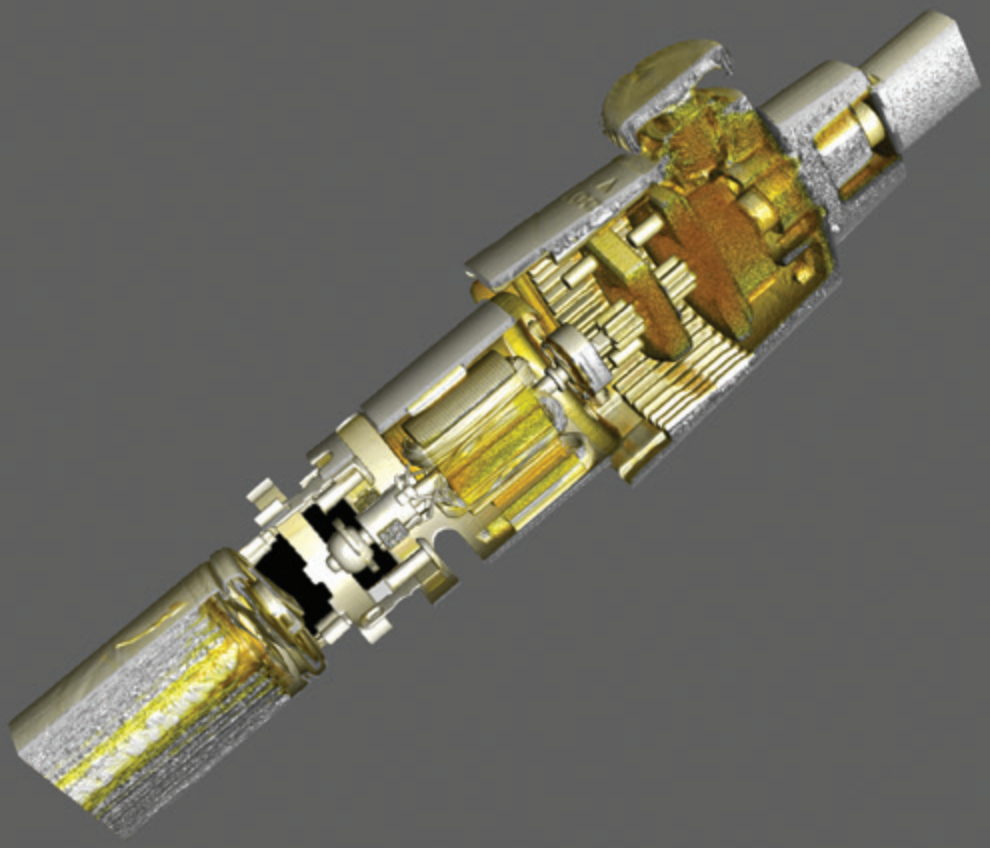

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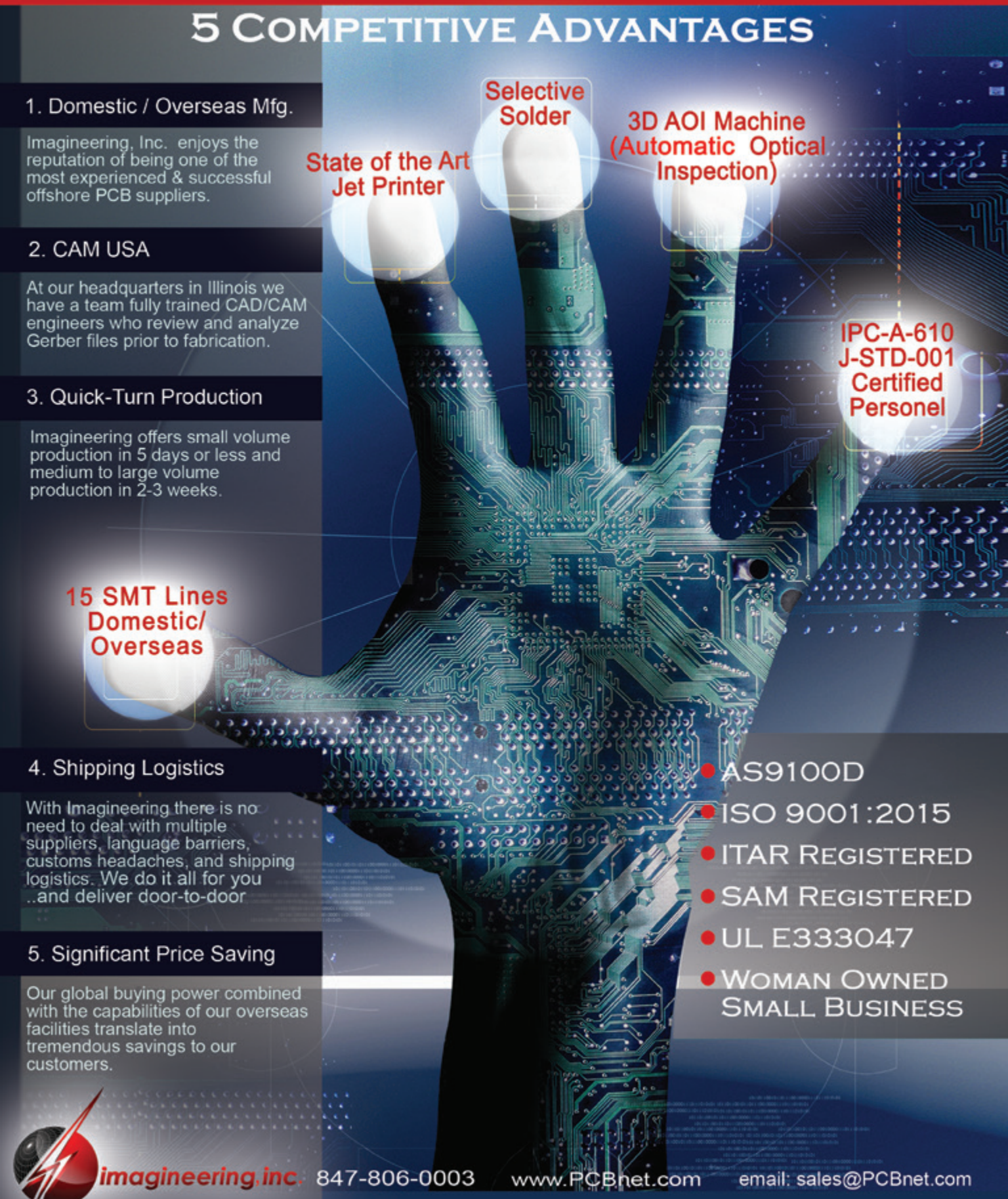

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MIKE BUETOW
EDITOR-IN-CHIEF

CCGAs Expose Brittle Supply Chain

FPGAS are a multibillion-dollar business, characterized by suppliers like Xilinx, MicroChip, Texas Instruments and Cypress Semiconductor. So why are they reliant on a single source for copper-wrapped solder column attachment?

And not just any source. Six Sigma is a small, founder-run Silicon Valley-based company. For more than 30 years, it has performed a variety of third-party services, including solder dipping, BGA reballing, and solderability testing. It also happens to be the sole supplier of copper-wrapped solder column attachment services to the major FPGA vendors. And according to industry watchers, that leaves the supply chain in something of a pickle.

The risk with any sole source is something happens that affects their ability to make deliveries. Such an outcome would spell disaster for the high-rel companies that use column grid arrays (CGAs). And loss of access to the unique copper-wrapped columns used in key programs, including military and space, would put those applications at severe risk.

One alternative is organic packages. An investigation published by Reza Ghaffarian at Jet Propulsion Laboratory in 2006 found solder joint reliability of plastic BGA packages on polymeric boards to be generally superior to that of the ceramic versions due to the CTE mismatch between the ceramic balls and the substrate. In 2015, new work performed by Martin Hart of TopLine found solder columns on ceramic packages to be more compliant than solder balls, and able to absorb CTE mismatch of up to 10ppm/^{o}C when soldered on a PCB.

In his paper, Hart also asserted that a copper-wrapped version is more reliable than the conventional tin-lead version. Raychem in 1983 found it could wrap copper ribbon around high-temperature PbSn20 solder wire, then apply a eutectic SnPb coating to secure the copper to the column. These ceramic CGA (or CCGA) packages were found to outlast conventional PbSn10 columns under temperature cycling tests, Hart wrote. In 2010, Kyocera-run finite element modeling tests found the effective thermal conductivity of Six Sigma's copper-reinforced interconnect was approximately 75% higher than the equivalent IBM high-lead CGA. In a subsequent study published in 2012, JPL tested CCGA packages for 596 thermal cycles ranging from -185° to +125°C – conditions meant to replicate those that would be experienced on Mars and Jupiter's moons – and found no catastrophic failures, although there was evidence of solder fatigue.

The research came at the same time the industry was undergoing a major supply chain shakeup. IBM, the inventor of the column grid array, sold its CGA equipment, IP, and licenses to Silicon Turnkey Systems, which in turn was acquired by Micross Components. (IBM was a main supplier to Xilinx.) A few years earlier, BAE, another supplier, switched to providing internal services only. That left Actel, which was acquired by MicroSemi in late 2010, without a supplier of solder columns. MicroSemi then outsourced its attachment services to Six Sigma. Previously, Raychem apparently didn't see the hoped-for revenue materialize, and subsequently licensed its patents to the last remaining supplier … Six Sigma.

There's little question additional suppliers would impact lead-times and pricing models in a positive way for customers. But the cost of capital equipment, coupled with the lengthy qualification time, seem to be roadblocks for the few companies that considered jumping in the mix.

Hart notes the frailty of the situation. "The defense industry should be concerned about its dependency on a single source vendor to attach copper-wrapped solder columns to FPGA devices as recorded in QML-38535," he said in a press statement. "Military-grade FPGA devices used for defense applications cannot function without solder columns."

Help may be on the way. Reports have it that as many as four companies might be inching toward qualification. Funding remains a critical issue, however.

Knowing the potential for losing a key sole source supplier, should the US government be more vested in the outcome? Perhaps, but it seems FPGAs simply don't rank high enough on the priority list for near-term action.

Beyond the not-so-simple matter of what the FPGA market might look like in a few years, this situation raises a host of knotty questions. In no specific order, how many other critical technologies are facing unplanned extinction? How do we speed the process so these "lower priority" items get resolved? When problems like this come about, is a consortium of the major vendors in order? And should government set up a team to instruct competitors on how to develop consortia for intensive short-term programs to resolve common industry problems like this?

mbuetow@upmediagroup.com
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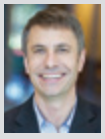
PCDF People

FAPCT named **Bill Schwerter** director of strategic sourcing.

Bürkle North America appointed **Kurt Palmer** president and CEO. Palmer has over 30 years of experience in consumable and equipment distribution throughout North America. He previously served as vice president of sales for Bürkle North America, director of operations for TCT Circuit Supply, and co-owner of Tapco Circuit Supply.

Isola named interim CEO **Travis Kelly** president and chief executive. He comes to the laminate supplier from an affiliate of Cerberus Capital Management, the private equity firm that owns Isola.



National Instruments promoted current president and COO **Eric Starkloff** (pictured) to president and CEO, effective Feb. 1. He replaces **Alex Davern**, who was CEO for three years.

Shennan Circuits USA named **Luis Rivera** regional FAE manager.

Summit Interconnect named **Marc Strickland** flex operations manager.

PCDF Briefs

Advanced Circuits completed its previously announced move to a new 50,000 sq. ft. location in suburban Phoenix and invested $4 million in new equipment at the site.

Apple reportedly is testing a smartphone with a wraparound display, one that makes use of the sides and rear of the handset.

Chemnitz University of Technology and **Fraunhofer** researchers have developed a combination of inkjet and screen printing, called multi-material 3-D printing tools, and are using it to develop electronic 3-D printed objects.

KAUST researchers found that a submicrometer-thin mesh of silver nanowires – that is transparent to light, highly electrically conductive, flexible and stretchable, and simple to make – could find use in flexible electronic displays, sensors or solar cells.

Future smartphones may not need traditional metal-based circuits if a startup led by **Apple's** ex-5G chief, Ruben Caballero, gets its way. **Keyssa's** solution is to ditch the pins.

Hofstetter PCB installed a **Schmid** PlasmaLine.

Ucamco to Add Assembly to Gerber X3 Format

GENT, BELGIUM – Ucamco in November announced plans to extend its Gerber data transfer format to include components. The company is seeking comments on the proposed new specification, which adds component layers to the top and bottom of the Gerber file structure.

The new layers show component location, shape, fiducial locations and footprints, all data that fit with the Gerber format's image files. These data are supported by a new set of attributes specific to the component layers and that provide non-geometric information about the component such as manufacturer part numbers.

The new layers are described using Gerber's existing syntax and methodology, added the company in a statement.

The development would bring Gerber closer in line with competitive formats such as IPC-2581 and ODB++, which for years have incorporated assembly attributes.

In a press release, Ucamco managing director Karel Tavernier said, "While designs for bare boards are transferred using Gerber files, the associated component data are typically contained in separate, non-standardized drawings and pick-and-place and BoM files. The Gerber format lends itself perfectly to the transfer of component data, as well as bare board data, and so it is a natural step for the format to be used to describe the board in its entirety."

Gerber X3 remains fully compatible with existing workflows, installed base and legacy software, he added. "The new component data are in dedicated files, separate from the bare board files, so if this data are not needed, these files can simply be ignored, and the manufacturer proceeds as before."

By combining bare board and component data, the Gerber files could offer an integrated overview of the entire board. In turn, operators could visualize component placement to check for errors and set up assembly, generate manufacturing tools such as paste stencils, program pick-and-place machines, and assist in component procurement.

Ucamco said the draft was developed in concert with industry experts, including Jean-Pierre Charras, who developed a prototype X3 input/output for KiCad, and Wim De Greve, head of software tools development at Eurocircuits. The new draft specification is available at ucamco.com/en/news/towards-gerber-x3. – *MB*

PCB West 2020 Show Floor Selling Out

ATLANTA – The exhibition floor space for PCB West 2020 is more than 80% sold as of Nov. 5, UP Media Group said. Booth sales began the first week of October, and the show floor is expected to sell out for the ninth year in a row, show organizers added.

"We sold 70% of the booths in the first 48 hours show renewals were available, and we fully expect to sell out the show floor again for 2020," said Frances Stewart, vice president of sales and marketing, UP Media Group. "While the early bird discount deadline has passed, we continue to get renewals and interest from new vendors because of the strong attendance and value for the money."

PCB West will be held Sept. 8 - 11, 2020, in Santa Clara, CA. The event includes a four-day technical conference and one-day exhibition to be held at the Santa Clara (CA) Convention Center.

PCB West provides a conference and exhibition focused on the design and manufacture of PCBs, HDI, electronics assembly and circuit board test. The September 2019 event attracted more than 2,400 registrants.

Currently 88 booths for the September 2020 trade show have been sold, or 80% of the show floor, leaving 22 booths remaining.

For information about exhibiting at PCB West, visit pcbwest.com or contact Frances Stewart at 678-817-1286; fstewart@upmediagroup.com.

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Conference & Exhibition

Conference: September 8 - 11

Exhibition: Wednesday, September 9

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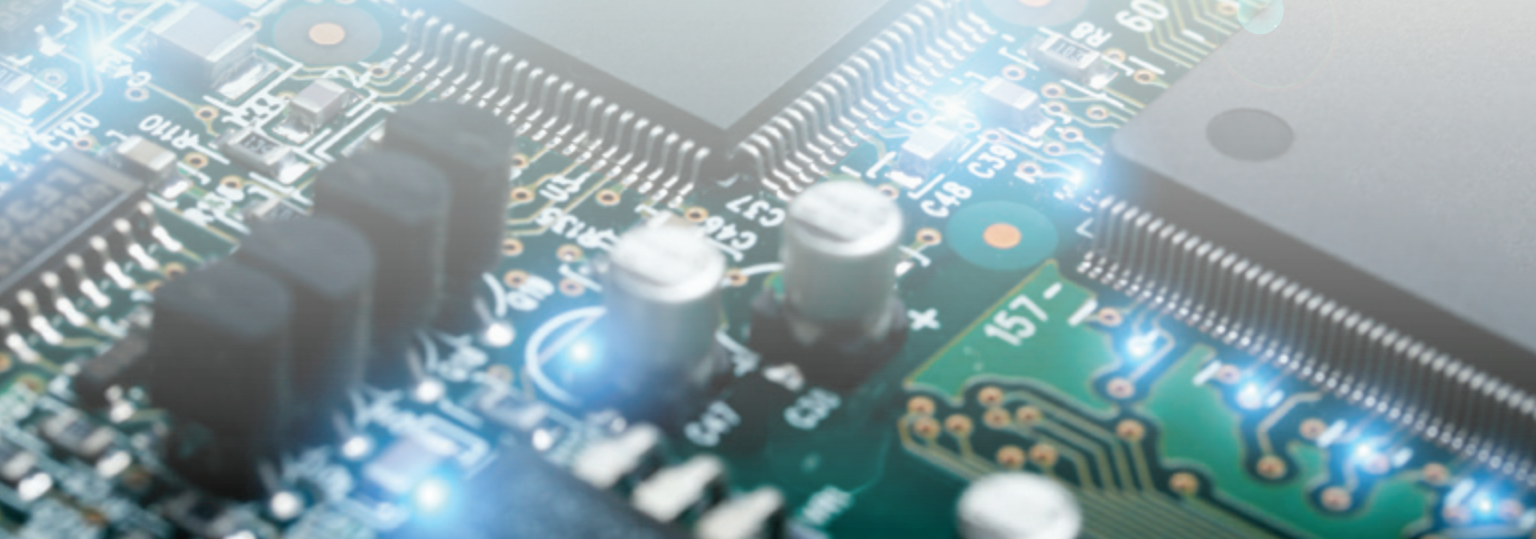
SANTA CLARA CONVENTION CENTER, CA



Linkoping University researchers discovered a conducting polymer that can both increase and reduce its volume when exposed to a weak electrical pulse. In a sponge, or filter, the researchers can control the size of particles that pass through.

Newark launched a new collection of affordable components, tools and test equipment under its new brand, Multicomp Pro.

PNC purchased a **Limata** X1000 laser direct imager.

Printed Circuits purchased a **Notion Systems** n.jet direct solder mask and legend ink printer.

Schweizer Electronic named **Neutronics Solutions** sales representative for the US and Canada.

The Swedish Chemicals Agency (Kemi) launched an investigation into the effects of the country's tax on certain chemicals in electronics.

Taiwan Union Technology has reportedly encountered quality issues with its copper-clad laminate that may lead to loss of some major orders from **Google**, according to reports.

Würth Elektronik CBT became the first fabricator to use **Taiyo America** IJSR-4000 JM03G inkjet solder mask in production.

CA People

Cogiscan promoted **Greg Benoit** to director of business development.

Mycronic promoted **Jeff Leal** to head of product management.

Neways appointed **Eric Stodel** CEO. In his 30-year career, he has held various leadership roles and senior management positions at Flextronics, Solectron, Driessen, B/E Aerospace, and Marinoffs.

Sanmina named **Kurt Adzema** EVP and CFO. He most recently served as CFO at Finisar.

Screaming Circuits promoted **Duane Benson** to director of marketing.

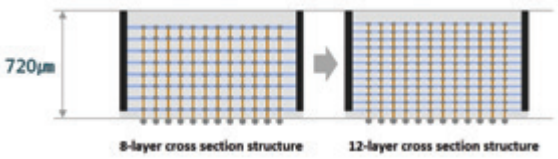
Valtronic announced **Sunita Kembhavi** as purchasing manager and Brett Crane as production manager.

VJ Technologies named **Lian Li** general manager in China. She has a bachelor's degree in mechanical technology and equipment, and was an engineer at ScienScope and vice general manager at Unicomp.

Samsung Develops First 12-Layer 3D-TSV Chip Packaging Technology

SEOUL – Samsung Electronics in October announced it has developed the industry's first 12-layer 3D-TSV (through-silicon via) technology. The innovation, which is used for mass production of high-performance chips, requires pinpoint accuracy to vertically interconnect 12 DRAM chips through a three-dimensional configuration of more than 60,000 TSV holes, each of which is one-twentieth the thickness of a single strand of human hair.

The thickness of the package (720µm) remains the same as current 8-layer high bandwidth memory-2 (HBM2) products, which is a substantial advancement in component design. This will help customers release next-generation, high-capacity products with higher performance capacity, without having to change their system configuration designs.



NICE PACKAGE Cross-section of the 8- and 12-layer TSV package.

The 3-D packaging technology also features a shorter data transmission time between chips than existing wire-bonding technology, resulting in faster speed and lower power consumption, Samsung says.

"Packaging technology that secures all of the intricacies of ultra-performance memory is becoming tremendously important, with the wide variety of new-age applications, such as artificial intelligence and high-power computing," said Hong-Joo Baek, executive vice president of TSP (Test & System Package) at Samsung Electronics.

"As Moore's law scaling reaches its limit, the role of 3D-TSV technology is expected to become even more critical. We want to be at the forefront of this state-of-the-art chip packaging technology."

Relying on its 12-layer 3D-TSV technology, Samsung will offer the highest DRAM performance for applications that are data-intensive and extremely high-speed.

Also, by increasing the number of stacked layers from eight to 12, Samsung will soon be able to mass produce 24-Gb high bandwidth memory, which provides three times the capacity of 8Gb high bandwidth memory on the market today. – *MB*

Researchers Report a New Way to Produce Curvy Electronics

HOUSTON – Contact lenses that can monitor your health, as well as correct your eyesight, aren't science fiction, but an efficient manufacturing method – finding a way to produce the curved lenses with embedded electronics – has remained elusive.

Until now. A team of researchers from the University of Houston and the University of Colorado Boulder reported developing a new manufacturing method, known as conformal additive stamp printing, or CAS printing, to produce the lenses, solar cells and other three-dimensional curvy electronics. The work, reported in the journal *Nature Electronics*, demonstrates the use of the manufacturing technique to produce many curvy devices not suited to current production methods. The work is also highlighted by the journal *Nature*.

"We tested a number of existing techniques to see if they were appropriate for manufacturing curvy electronics," said Cunjiang Yu, Bill D. Cook Associate Professor of Mechanical Engineering at the University of Houston and corresponding author on the paper. "The answer is no. They all had limitations and problems."

Instead, Yu, who is also a principal investigator with the Texas Center for Super-

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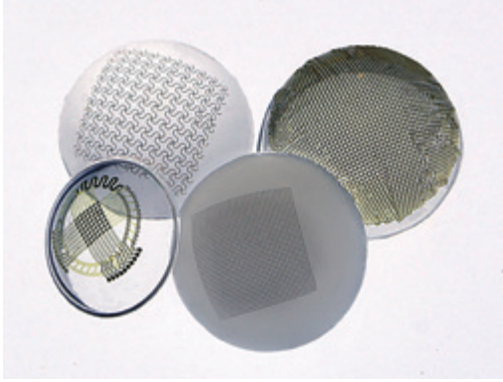

BEND IT A team of researchers is using CAS printing to make curvy 3-D electronics.

conductivity at UH, and his team devised a new method, which they report opens the door to the efficient production of a range of curvy electronic devices, from wearables to optoelectronics, telecommunications and biomedical applications.

"Electronic devices are typically manufactured in planar layouts, but many emerging applications, from optoelectronics to wearables, require three-dimensional curvy structures," the researchers wrote. "However, the fabrication of such structures has proved challenging due, in particular, to the lack of an effective manufacturing technology."

Existing manufacturing technologies, including microfabrication, don't work for curved, three-dimensional electronics because they are inherently designed to produce two-dimensional, flat electronic devices, Yu said. But increasingly, there is a need for electronic devices that require curvy, 3-D shapes, including smart contact lenses, curved imagers, electronic antennas and hemispherical solar cells, among other devices.

These devices are small – ranging in size from millimeters to centimeters – with accuracy within a few microns.

Recognizing that, Yu and the other researchers proposed the new fabrication method: conformal additive stamp printing, or CAS printing.

CAS printing works like this: An elastomeric, or stretchy, balloon is inflated and coated with a sticky substance. It is then used as a stamping medium, pushing down on prefabricated electronic devices to pick up the electronics and then print them onto various curvy surfaces. In the paper, the researchers describe using the method to create a variety of curvy devices, including silicon pellets, photodetector arrays, small antennas, hemispherical solar cells and smart contact lenses.

The work was performed using a manual version of the CAS printer, although the researchers also designed an automated version. Yu said that will make it easy to scale up production.

In addition to Yu, coauthors include Kyoseung Sim, Song Chen, Zhoulyu Rao, Jingshen Liu, Yuntao Lu, Seonmin Jang, Faheem Ershad and Ji Chen, all with UH, and Zhengwei Li and Jianliang Xiao, both with the University of Colorado Boulder.

This work was supported by National Science Foundation. – *University of Houston/Jeannie Kever*

CA Briefs

BESTProto installed a **Mycronic** MY-600 solder paste printer.

Cal-Comp Technology (Philippines) has decided for the second time to withdraw its planned $210 million IPO on the local exchange.

Celestica is cutting ties with **Cisco**, its largest customer at $750 million annually, after failing to meet profitability targets.

Cornell Capital announced an investment in **Lorom Holding**, a provider of cable and printed circuit assembly.

Critical Manufacturing has partnered with **Cogiscan** to deliver advanced smart factory solutions for electronics manufacturers.

Fabrinet has signed a lease for a building in Israel, where the EMS firm plans to establish an NPI assembly facility.

Flex is planning to invest up to $500 million to expand its manufacturing base in India, according to reports. The firm plans to set up export-oriented facilities, aiming for revenue of $1 billion in the next year.

Foxconn's plans to build five innovation centers in Wisconsin have stalled, Wisconsin Public Radio reported. Foxconn disputes the report.

India expects **Apple**, **Foxconn** and **Flextronics** to boost production on its soil due to new favorable taxation laws aimed at drawing in manufacturers.

International Controls Services purchased a **Kurtz Ersa** HR 600/2 hybrid rework system.

Inventec will invest $157 million to expand production facilities in Taiwan, the Ministry of Economic Affairs said.

Gateway Technical College officially opened a renovated and expanded advanced manufacturing center, adding nearly 36,000 sq. ft. to the **Foxconn** and state-supported project.

Inspur Electronic Information purchased a **Universal Instruments** FuzionOF placement platform.

IPC issued a call for posters for IPC Apex Expo 2020 in San Diego.

Kitron installed a pair of **Universal Instruments** Fuzion SMT lines for its new facility in Grudziadz, Poland.

Kongsberg Defence & Aerospace placed an order with **Kitron** worth about $10 million.

Lightspeed Manufacturing has moved to a larger EMS facility in Haverhill, MA, to accommodate growth.

Neo Tech expanded its partnership with electronic thermostat OEM **Pro1**.

Optomec has delivered its 500th industrial 3-D printer, this one to a division of **General Electric**.

Out of the Box Manufacturing purchased a **Kurtz Ersa** HR 600/2 Hybrid rework system.

Pegatron will not rule out setting up new factory sites in Vietnam and India to satisfy customer demand, according to company president and CEO SJ Liao.

Philippine electronics exports are at significant risk of being harmed if China – the country's top market – gets its consumer electronics slapped with tariffs next month in the ongoing US-China trade war.

Plasmatreat opened a 15,000 sq. ft. technology and research center at the company's headquarters in Steinhagen, Germany.

Precision Graphics installed two **Juki** ISM towers and an Incoming Material Station.

Transition Automation appointed **AdoptSMT** as distributor in Germany, Switzerland, Austria, and Eastern Europe regions.

Universal Instruments installed a **MIRTEC** OMNI 3-D AOI at its Advanced Process Lab.

Universal Instruments will celebrate its 100th anniversary with a companywide party at its Conklin, NY, corporate headquarters on Nov. 15.

The **US PTO** has issued a patent protecting Dynamic Dual Head dispensing technology for the Camalot Prodigy dispenser.

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EMPTY STORAGE

Trends in the US electronics equipment market (shipments only).

	% CHANGE			
	July	Aug.	Sept.	YTD%
Computers and electronics products	-0.3	-0.3	-0.4	4.2
Computers	-1.2	-2.0	-6.9	-22.4
Storage devices	2.7	-0.3	-11.3	18.7
Other peripheral equipment	-5.5	4.6	3.4	6.1
Nondefense communications equipment	0.6	0.0	0.7	11.7
Defense communications equipment	-14.9	-3.0	0.8	-0.2
A/V equipment	0.6	-8.0	-4.8	33.1
Components[1]	-1.0	2.2	-2.2	4.2
Nondefense search & navigation equipment	0.4	-0.1	-5.5	2.9
Defense search & navigation equipment	1.1	-0.7	0.3	3.0
Medical, measurement and control	0.5	-1.0	0.0	0.6

[r]Revised. *Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: U.S. Department of Commerce Census Bureau, Nov. 4, 2019

IPC: 90% of US Electronics Manufacturers 'Troubled' by Higher Tariffs

BANNOCKBURN, IL — Almost 90% of US electronics manufacturers are troubled by the higher tariffs imposed by the US and China on each other's imports, and some are investing less in the US and hiring fewer workers as a result, according to new IPC survey results.

On average, companies report tariff increases on 31% of the total dollar value of the products they import. Twenty-five percent of companies report over half of the dollar value of the products they import are facing higher tariffs.

IPC queried its US members between Sept. 25 and Oct. 2.

Some 69% of companies report lower profit margins as a result of increased tariffs, with a ripple effect of negative consequences: 21% report they are reducing investment in the US, and 13% say they are cutting back on hiring and/or reducing headcount.

More than a third of companies report they cannot increase their prices to cover the cost of higher import tariffs because of various factors.

Fifty-one percent of responding companies report they are now sourcing from countries other than China as a result of increased tariffs on Chinese imports.

Hot Takes

- Taiwan's manufacturing production index fell 0.65% year-over-year and 3.53% sequentially to 111.1 in September. (Taiwan Ministry of Economic Affairs)
- Household refrigeration and laundry appliances are on track to ship 326 million units worldwide in 2019 and 330 million in 2020, with smart appliances on track to double to 33 million units in 2020. (Futuresource Consulting)
- Notebook shipments in 2019 are estimated to increase 1.6%, then slip significantly due to the 15% US tariff on Chinese-made notebooks. (DigiTimes)
- Video conferencing hardware shipments increased 50% last year, reaching 1.4 million units, with a projected CAGR of 27% through 2022. (Futuresource Consulting)
- The power device market grew 13.9% in 2018 and is expected to grow this year as well. (Yole Développement)
- Japan PCB shipments were down 1% year-over-year in value and 3.1% in volumes in August. (JPCA)

METALS INDEX

US MANUFACTURING INDICES

	JUNE	JULY	AUG.	SEPT.	OCT.
PMI	51.7	51.2	49.1	47.8	48.3
New orders	50.0	50.8	47.2	47.3	49.1
Production	54.1	50.8	49.5	47.3	46.2
Inventories	49.1	49.5	49.9	46.9	48.9
Customer inventories	44.6	45.7	44.9	45.5	47.8
Backlogs	47.2	43.1	46.3	45.1	44.1

Sources: Institute for Supply Management, Nov. 1, 2019

KEY COMPONENTS

	MAY	JUNE	JULY	AUG.	SEPT.
Semiconductor equipment billings[1]	-23.6%	-18.4%	-14.6%	-10.5%[r]	-6.0%[p]
Semiconductors[2]	-14.8%	-16.5%	-15.5%[r]	-15.4%[r]	-14.6%[p]
PCBs[3] (North America)	0.99	1.00	1.00	1.02	1.04
Computers/electronic products[4]	5.39	5.46	5.46	5.48[r]	5.52[p]

Sources: [1]SEMI, [2]SIA (3-month moving average growth), [3]IPC, [4]Census Bureau, [p]preliminary, [r]revised

Speed Freeze

As veteran engineers know, sometimes less is more, and a lot faster.

OUR INDUSTRY IS noted for spectacular new technology that eclipses everything around it at breathtaking speed. As exciting and noteworthy as those technologies may seem, however, success more often moves in ways and at speeds akin to the proverbial turtle. Patience pays.

The virtue of patience struck me while attending a regional industry event. The afternoon included technical presentations and a tour of an advanced manufacturing facility. The tour was conducted by energetic, sharp, intelligent young engineers who were excited and proud to show off the fruits of their labors. The facility did not have the latest equipment, but these innovative young bucks set up the equipment to take full advantage of the latest in holistic ergonomic advances, lean material logistics, and had a connected digital ecosystem that would make any Industry 4.0 proponent proud.

The tour was topped off by a strategic *Star Wars*-inspired planning room where stakeholders from all over the company connect via a real-time, 360° media area to look at problems, products, opportunities, and perform the necessary planning to ensure the highest level of quality in the quickest turn time. This collaborative media war room was designed to maximize communication to expedite decision-making. Someone asked how much time this protocol saved. Perhaps the vague reply should have been a warning: "Our productivity has increased significantly by having all stakeholders actively involved … ."

The tour was engaging, the technology deployments state-of-the-art, and the manufacturing challenges and goals awe-inspiring. We visitors were truly wowed. Well, up until one of the more seasoned spectators asked one of the beaming tour-guides this: "What is your single biggest obstacle to success?" The answer came back: "It takes too long to get things done. We need to get more done faster to meet our demand," which led to the following: "So, what are you doing about it?"

The response was what you might expect from an eager engineer.

We heard about how they get everyone together – globally – on a regular basis to review any given problem or opportunity. Then, tasks are assigned, and staffers report back at the next global meeting, sometimes with PowerPoint presentations or perhaps video showing the situation, so the group can look, talk, and determine the best course of action. And let there be no mistake, the key word was ACTION! These young engineers spent as much of their time planning, scheduling and reporting about meetings to increase speed, throughput and "productivity" as they did on the shop floor dealing with speed, throughput and "productivity."

The tours wound down, and the afternoon was topped off by technical presentations. Each presentation was made by a seasoned industry veteran and focused on finding new solutions to problems the young engineers had encountered. This company was blessed to have a cadre of senior-level talent available to tackle the exciting new challenges brought forth by the engaging young engineers.

Each presentation began the same way: identifying a problem in the manufacturing process that was gumming up the works, then citing the protocol followed and the ultimate solution. One problem was chronic poor quality when running a particular material that reduced throughput. Another was assembly equipment stopping mid-cycle because of some sort of failure, which reduced speed and negatively impacted "productivity." How the veterans' responses differ from those of the young engineers made an interesting contrast.

The process followed by each presenter was similar. Look at samples and/or equipment, collect suspect materials, talk to shop-floor operators, then retreat into the lab to develop and conduct a battery of experiments. The presentations outlined the findings, recommended a solution, and course of action to implement the solution, and reported the improvement achieved to date.

Someone asked if the veterans used the futuristic planning room during their analysis. The answer was consistently "no." Their tone indicated the problems were isolated, and adding people to the conversation can lead a team off track, swelling a project into something that takes forever to complete. As one of the presenters noted, "Sometimes less is more, and a lot faster."

Which gets back to patience. Technological advances stretch everyone. In a strong economy, the stretch may be how to crank up production when hiring competent workers is so difficult. When the economy is down, the stretch may be how to develop something with minimal investment dollars available. Meeting those and myriad other challenges, often seems to set everyone sprinting off toward a quick solution. Patience! It takes patience to stay focused on the challenge, rather than allowing the response to escalate out of reasonable control. It takes patience to follow a methodical approach, rather than involving many unnecessary colleagues who may inadvertently put the brakes on a fast-track need.

There's a place for youthful enthusiasm. Just be sure they stay on the right track. ❑

PETER BIGELOW
is president and CEO of IMI Inc. (imipcb.com); pbigelow@imipcb.com. His column appears monthly.

Preparing for the Workplace of Tomorrow

Workers need to understand the "why" of manufacturing and how to manage processes.

THE PACE OF technological change continues to increase. Products are getting smaller and more challenging to build. The increased levels of automation needed to build those products are driving a need to rethink the role of the personnel associated with those machines. The worker who fills those new jobs needs to understand the "why" of manufacturing and have the critical thinking skills to manage processes rather than just run machines.

One example of this role rethinking is happening at Burton Industries, an electronics manufacturing services (EMS) provider whose primary manufacturing facility is in Michigan's Upper Peninsula.

"We believe it is our responsibility to stay in front of the technology needs and expectations of our customers," said Gary Burnett, president and CEO, Burton Industries. "While we've made the investment in the equipment needed to support advanced manufacturing challenges, we also see the need to create an internal culture where every employee recognizes the very important role they play in helping our customers succeed. To that end, we have moved away from the traditional model of machine operators and inspectors supported by engineering and quality assurance managers in our surface mount device (SMD) area. Our model now requires all SMD area team members to obtain and possess skill level and training equal to process engineers. Each team member now has a training plan designed to accomplish that. To incentivize that extra effort, we've made these positions some of the highest-paid in our facility."

The company focused on launching this effort predominantly in the SMD area for two reasons. First, on average, 90% of the components placed are surface mount. Second, production is predominately focused on high-mix, low-to-medium-volume manufacturing for customers with variable demand. In order to support customer requirements, the SMD area needs a team that can flexibly move around the area as daily demand changes.

This transition is still a work in progress. To start, the company defined five position expertise classifications for its SMD area:

- Entry level
- Intermediate level
- Advanced level
- Expert level
- Advanced expert.

Entry-level associates complete approximately 22 hr. of job-specific training, including basic operating procedures on every piece of equipment in the SMD area. They complete another 9 hr. of training related to OSHA and general workplace safety training. At the intermediate level, training expands to include documentation packages, equipment maintenance, inspection procedures, quality concepts and processes, and customer satisfaction. Those in the intermediate classification also pursue IPC-A-610 certification. At the advanced level, training moves to machine programming and rework procedures. At the expert level, associates receive manufacturer-provided training on all equipment in the work cell, plus start to train in the procedures related to support of the area, such as software validation and incoming material inspection procedures. They also pursue IPC certification in repair/rework. At the advanced expert level, associates become a mentor/trainer to the team and pursue SMTA Process Certification. They are responsible for SMD area process decisions, maintaining zero defects, managing continuous improvement efforts and equipment validation. As currently envisioned, the total process requires nearly two years to complete required training and associated testing.

"There wasn't a template out there for us to use. We had to create this," said Rosemary Kazik, human resource director.

In establishing this factory within a factory focus, the company opened all the positions within the SMD and allowed all employees to apply for these Learn 2 Earn positions. The expectation is that everyone applying would be put on a training path designed to reach expert level or higher. Workers disinclined to apply had options too.

"There were people who chose not to apply for this reengineered job," said Kazik. "Nobody lost a job. We moved them to other areas to see where they would fit best. We will eventually reengineer all production areas in the company, so those who have moved will be on a path to higher competency levels and compensation. In most cases, people who preferred to be transferred were new to SMD and were less confident of their skill. This gives them more time to learn jobs in the areas they've transferred to and build that confidence. At the same time, we had people outside of the SMD area who wanted the challenge."

As with all new initiatives, there have been challenges. Developing new, explanatory documentation was one.

"The team will be doing everything from stencil design to build when fully trained. We could find training material on the 'how,' but we've had to create our own material to explain the 'why.' For the team to make the right decisions to effectively manage their SMD factory, they need to have a clear understanding of the 'why' behind the decisions," said Darren Pieczynski, solutions engineer.

SUSAN MUCHA is president of Powell-Mucha Consulting Inc. (powell-muchaconsulting.com), a consulting firm providing strategic planning, training and market positioning support to EMS companies, and author of *Find It. Book It. Grow It. A Robust Process for Account Acquisition in Electronics Manufacturing Services*; smucha@powell-muchaconsulting.com.

Another challenge was keeping manufacturing running smoothly while training was underway. At program inception, 14 employees were classified to the five skill levels based on their experience and skills base. They are required to complete all training and tests to officially qualify for those positions within the next 12 to 18 months. As a result, work schedules need to include time for training.

Director of manufacturing Monica Benson called the amount of planning "exciting": "The success we've enjoyed so far, and the success we will have, is due to the planning. The goal is that everyone will be cross-trained in the cell. The training plan and schedule really maps everything out to get an amazing amount of training for a good number of people in a short period of time. Yet, we have to be cognizant that in a schedule this tightly packed, something like a bad flu season could slow us down."

How do employees feel about the new program?

"I think including the 'why' of what we do helps folks who think out of the box," said Ayricka Bailey, machine operator intermediate. "If we know the 'why,' it helps us fix problems without disrupting things. If I change something, does this create a problem? The 'why' tells me that. I think this helps the team efforts."

"When everyone works as a team, it is more interesting," adds Greg Vallone, senior operator, advanced expert. "We don't have to struggle because we are approaching this with a pit crew mentality. When people are struggling with a job they have difficulty performing, they don't want to come to work. But in a pit crew, no one person has a mountain to climb. Everyone knows how they fit in."

"There are clear guidelines to move to the next level. The structure and organization work well," said Jacob Cadeau, SMD machine operator, intermediate.

"I like the fast-paced environment. It keeps your brain moving. Every day there are new continuous improvement challenges. We want to be flexible for our customers, and translating that ability into an efficient line changeover strategy takes work. We are measuring downtime with stop clocks and utilizing other visual factory tools to ensure the team can proactively work on continuous improvement," said Zach Wangelin, SMD work cell leader, who is currently qualifying as an advanced expert.

There have also been benefits from a recruiting standpoint. As Kazik says, Burton wants employees to see the opportunities and career paths. "That's a great recruiting tool because most employers in our area are not offering this type of pathway to success. We don't let people fail. We'll find another path for those unable to achieve at least the expert level in SMD."

While still a work in progress, Burton Industries' approach appears to be paying dividends for all concerned: a more flexible, self-directed work team, lower turnover and a path to success for employees willing to Learn 2 Earn. ❑

Should PCB Buyers Pay Tooling and Testing Charges?

Automation and faster amortization should mean lower costs.

PCB MANUFACTURERS OFTEN include nonrecurring engineering (NRE) and electrical test (ET) charges in quotes, in addition to the piece price. During my training sessions for board buyers, I am frequently asked how to avoid those charges.

It's a good question.

When I started in this industry some – ahem – 30 years ago, NRE charges were approximately $100 per conductive layer, meaning a 4-layer PCB was $400; a 6-layer PCB was $600, and so on. Back then, it took a lot of labor hours to create manufacturing files from a piece of original artwork, as nothing was as digital as it is today.

With advances in technology, releasing an order to the manufacturing floor requires a fraction of the time it once did. Sure, some board manufacturers still do some things manually, but most have adapted their front-end engineering to incorporate technological advances.

Laser direct imaging (LDI) has eliminated use of expensive and time-consuming films with strict storage requirements. In addition, liquid photoimageable (LPI) solder mask and legend applied with inkjet technology has automated much of the PCB production process.

On top of that, many of today's fabricators outsource front-end engineering capabilities overseas at a fraction of the cost to maintain a domestic staff, especially to India. They pay a fixed cost for a service, whether they receive one new job per day or per month. This significantly reduces tooling costs and the time required to create those tools for the board supplier. Shouldn't the PCB buyer benefit from that?

Like NRE, the process for electrical test has seen improvements in cost drivers. In the past, dedicated electrical test fixtures were the industry standard. With dedicated fixtures, electrical testing charges are based on the hole count or test points required. The charge also includes material and time required to drill holes for the fixture plates that house the spring-loaded test pins. The dedicated fixtures are manually assembled.

Dedicated fixtures, while great for high-volume production orders, require plenty of storage space. Or they must be disassembled after use, only to then be manually put together for a reorder, which requires more time.

Most PCBs shipped to the US today are comprised of high-mix, prototype-through-medium-volume production, where the time, labor and storage space required for dedicated fixtures may not make much sense.

The better solution is for manufacturers to use fixtureless testing, also called flying probe testing.

Flying probe testers are fixtureless, meaning the Gerbers received from the customer generate a test program.

Depending on the type of machine used, the printed circuit board, whether an individual piece or multiple pieces on a manufacturing panel, is secured vertically or horizontally, and the flying probes do their work. The time required depends on the machine speed and number of points needing testing. Setup time between orders is minimal, and retesting can be done quickly.

Flying probe testers once were too expensive for most fabricators. In fact, fabricators had to send their orders to outside service companies called test houses.

But that meant PCB delivery schedules and ET charges had to account for shipping time and freight to the test houses, as well as time to get orders back to the fabricator for final inspection before shipment to the customer.

Today, as test equipment costs have decreased, most PCB manufacturers have at least one flying probe on site, meaning their testing costs per part number have dropped significantly. So, testing charges passed on to buyers should also be much lower. You may be able to get ET charges waived altogether. But just like with NRE charges, your ability to do so will depend on the size, dollar value, and longevity of your orders with a particular manufacturer.

You now have far more power as a buyer to get tooling charges waived or reduced, but you must be able to ask. Here's what you need to know:

Are you dealing with a broker? Brokers make anywhere from 20 to 40% on the purchase order total. If brokers play a major role in your PCB supplier base, always ask for the NRE to be waived.

Order size matters. Is it for five pieces or five thousand? The bigger the order, the easier it is to get the NRE waived. Any order totaling more than $10,000 in value that is an IPC-A-600 Class 2 commercial build with standard delivery time should have tooling waived. It's a different story for military or medical builds that require special paperwork. For lesser value orders, you might be able to get the manufacturer to discount the tooling cost.

Ongoing orders rule. Most fabricators want continuous runners: orders that have multiple scheduled deliveries with very few revision changes. Those orders are sought after and are easily welcomed with tooling charges waived.

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GREG PAPANDREW has more than 25 years' experience selling PCBs directly for various fabricators and as founder of a leading distributor. He is cofounder of Better Board Buying, a purchasing training consulting firm; greg@boardbuying.com.

What Surrounds a Typical Trace?

At higher speeds, the micro-environment around traces can alter simulation results.

IN THE PAST few weeks, e-mails from multiple sources crossed my inbox asking about the relationship between epoxy resin and signal behavior. With a couple of SI guys on one side and a career PCB manufacturing guy on the other side hitting me the same week with different versions of the same question, I thought it would make for an interesting column topic.

FIGURE 1 shows the initial image I was provided, along with the question what surrounds a typical trace? At face value, this may sound trivial, but it's a reasonable issue for a signal-integrity practitioner to be concerned about.

The answer depends on what's above the signal layer, what's below it, and where it appears in the stackup. Figure 1 is a reasonable representation of an inner stripline layer, if the cross-hatched dielectric representation is a prepreg with a fully cured core above it. In this case, the copper features on the signal layer are encompassed by a layer of resin that comes from the adjacent prepreg, as a result of heat and pressure applied during the lamination process.

After making the above observation, I learned that the trace whose surroundings were in question was on an outer microstrip layer, with air on top. In this case, the cross-hatched area would typically be prepreg as before, but Figure 1 no longer accurately represents the "micro-environment" around the trace. The reason outerlayer copper features aren't surrounded by resin is that the entire printed circuit board sandwich goes through the lamination press with a solid piece of copper on top. None of the resin flows around the trace, because the resin is fully cured before features in the outerlayer copper are etched. From there, drilling and plating take place, and solder mask is typically applied. As a result, a more accurate model of the micro-environment around the trace would either be air or solder mask, as shown in **FIGURE 2**. This is significantly different from Figure 1, of course, and we should expect different results in both simulated and manufactured circuit boards.

So what? At this point, you may be asking, "Who cares?" And if you're signaling at 1MHz, you probably don't care. But if you're pushing multi-gigabit speeds, knowing the "micro-environment" around the signals you are modeling with that expensive SI software might be a good idea, right? A more accurate picture of Figure 1, if it represents a stripline, is shown in **FIGURE 3**.

The figure shows innerlayer (stripline) signal layers are surrounded by resin on both sides. This is important because the resin has fundamentally different electrical properties than the adjacent prepreg or core materials.

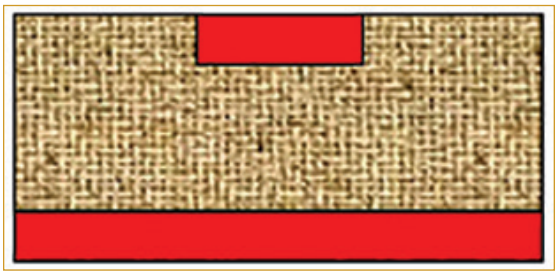

FIGURE 1. This started as a microstrip representation, but it's more representative of a stripline.

It's important to realize that core and prepreg spec sheets report composite dielectric constant (Dk) and dissipation factor (Df) numbers for the glass and resin combined. No surprise there, but these composite Dk and Df values represent highly dissimilar components. Electrical-grade glass fiber ("E" glass), for example, has a Dk of roughly 6.8. While it depends on the resin system – there are at least 100 to choose from – typi-

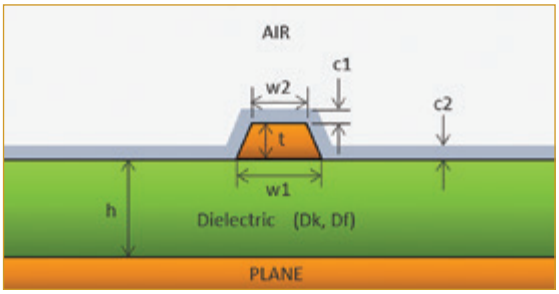

FIGURE 2. A more accurate representation of the microstrip trace in Figure 1, including conformal coating (solder mask).

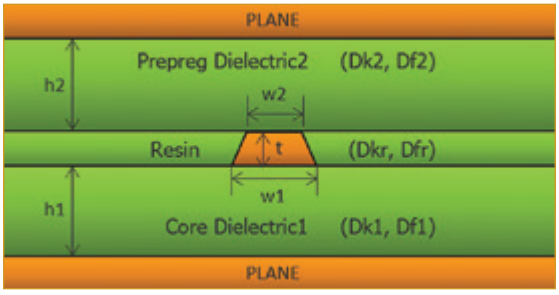

FIGURE 3. A more accurate representation of the cross-section in Figure 1, if it represents a stripline.

BILL HARGIN
has more than 20 years' experience in PCB design software and materials. He is director of everything at Z-zero (z-zero.com); billh@z-zero.com.

cal epoxy resins are in the ~3.0 Dk range. Lower Dks mean higher signal-propagation velocities and higher impedances. It's reasonable to ask how significant this effect is, so that's what we'll investigate next.

Electrical impacts from stackup parameters. Some SI practitioners assume the dielectric adjacent to and on the same plane as the signal are represented by the electrical parameters of the vertically adjacent laminate (core) or prepreg, so we'll start with this notion as a baseline, while looking at impedance, propagation speed, and predicted insertion loss as dependent variables for comparison.

We'll use 0.5oz. copper, a 6-mil wide stripline trace, 5-mil thick core and prepreg, a Dk of 3.85, with Df equal to 0.010. Using the dielectric-property assumptions noted in the previous paragraph, the resin adjacent to the signal layer will be modeled with the aforementioned parameters.

Temporarily ignoring copper roughness and etch effects – topics for another day, perhaps – the stripline in Figure 2 results in a 43.8Ω impedance, a propagation velocity of 6.02in/ns, and a simulated insertion loss of 0.81dB/in at 10GHz.

Next, let's look at the same cross-section, while including adjustments for the fact that resin will surround the signal traces. An algorithm built into industry modeling software estimates "neat" (pure) resin properties from the adjacent prepreg as Dk=3.08 and Df=0.015, resulting in a 44.1Ω impedance, a propagation velocity of 6.06in/ns, and a simulated insertion loss of 0.83dB/in at 10GHz. So, less-accurate modeling of the resin layer leads to underestimation of impedance, propagation velocity and insertion loss. Whether these differences are enough to cause downstream SI problems depends on what is being designed, over what transmission-line lengths, and at what frequencies. **FIGURE 4** shows these simulated results in Z-zero Z-solver software.

Microstrip modeling. Given an ounce of copper plating, the incorrectly drawn microstrip in Figure 1 results in a 54.6Ω impedance, a propagation velocity of 7.2in/ns, and a simulated insertion loss of 0.51dB/in at 10GHz. But it's an imaginary construction … a GIGO exercise!

Modeling Figure 1 and including solder mask results in a somewhat similar 53.7Ω impedance, a propagation velocity of 6.87in/ns, and a simulated insertion loss of 0.62dB/in at 10GHz. Can you survive overestimating propagation velocity by 0.33in/ns and underestimating insertion loss by 0.11dB/in? Perhaps. The problem multiplies when you consider whether these differences are happening across 5" to 15" traces or 30" to 40" backplanes and at progressively increasing speeds.

Conclusion. Differential-signaling characteristics and crosstalk will also be affected by these adjustments to the micro-environment on signal-trace layers. And, as Lee Ritchey often points out, differential signals are comprised of two single-ended transmission lines that may or may not be closely coupled to each other. I decided to focus on single-ended signals to avoid blurring the main point, which is that if you're signaling at multi-gigabit speeds, details like the micro-environment around traces matter. You can simulate your face off, but absent the correct underlying stackup details, that expensive SI simulator may be providing less-than-accurate results. □

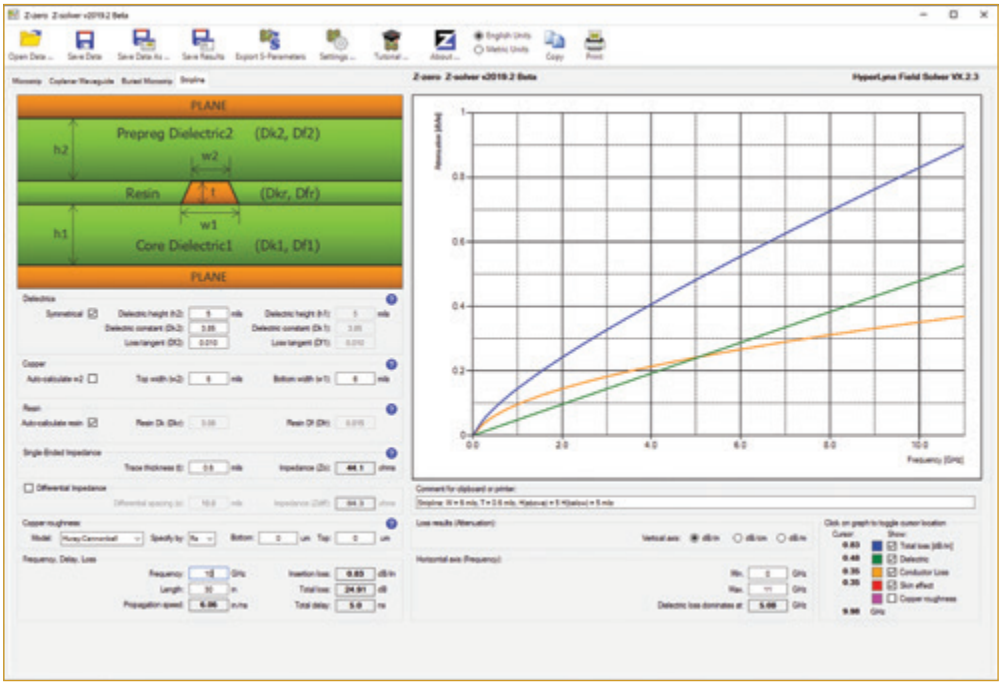

FIGURE 4. A single-ended stripline, including modeling of "neat" resin using Z-zero Z-planner software and Mentor's HyperLynx field solver.

Why 'Born on Dating' is Not a Reliable Means for PCB Shelf Life

Flex circuit solderability and life expectancy are influenced by handling and finishes.

WHAT IS THE shelf life of a flex circuit if it stays in its original sealed packaging? And what is the life expectancy of a flexible circuit?

I assume the first question refers to long-term solderability and the second to the overall functionality of the flex circuit once installed in the final application.

As far as long-term functionality goes, flexible circuits in a *static* application really don't have a post-installation "best if used by" date. There are flexible circuits over 25 years old still functioning without issue in military and avionics systems. Flexible circuits have also been used for decades in satellite applications due to their very low mass and high connection density. Considering the cost of a service call to a satellite, only the most reliable interconnects are used in these applications. That flexible circuits are still in use after all these years is a testament to their long-term reliability. The only exceptions to overall life expectancy are flexible circuits operating in very harsh environments, such as continuous temperatures above 275°F, strong acid or caustic exposure, abrasion, etc.

In short, flexible circuits installed in a protected, moderate environment will typically outlive the device in which they are installed. Note again that everything so far refers to a static application. If the application is dynamic, all bets are off. So many variables can affect the dynamic performance of a flex circuit, it impossible to cover them all, at least not in a one-page column. My advice is to refer to the general guidelines in IPC-2223, *Sectional Design Standard for Flexible Printed Boards*, and then discuss the application with the flexible circuit supplier. They should be able to evaluate the application and offer a good estimate of longevity. This will be stated as a function of the number of flex cycles, rather than time.

Regarding life expectancy, many things affect flex circuit solderability after an extended time on the shelf. The first issue is moisture content and absorption. Do *not* assume the supplier did a complete preconditioning bake to remove moisture before the parts were bagged and sealed. While a sealed bag should keep parts from absorbing additional moisture, it will not remove existing moisture. The sealed bag will also trap any moisture carried by the circuit when it was packed. It is best to assume parts were not baked immediately prior to shipment and contain some amount of moisture. If a flex with even a moderate amount of moisture content is processed through a reflow oven, the results will not be pretty. When moisture-laden flex is rapidly heated in a reflow oven, the moisture will rapidly expand and can cause severe blistering and delamination. It is always best to do a preconditioning bake at the assembly facility immediately prior to SMT. Even if the parts are already reasonably dry, another baking step will not hurt anything.

Another step to potentially increase solderable shelf life is to require your supplier to include a desiccant pack and a humidity indicator card (HIC) inside the sealed bag (**FIGURES 1** and **2**). This will help ensure parts stay dry until the bag is opened. If you do this, also make sure your receiving department does not

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FIGURE 1. Including a desiccant pack and humidity indicator card (HIC) inside the sealed bag will help keep flexible circuits dry when they are on the shelf.

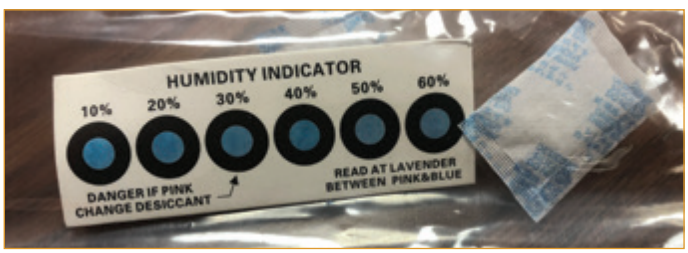


FIGURE 2. Close-up of the HIC.

MARK FINSTAD is senior application engineer at Flexible Circuit Technologies (flexiblecircuit.com); mark.finstad@flexiblecircuit.com. He and co-"Flexpert" **NICK KOOP** (nick.koop@ttmtech.com) welcome your suggestions. The authors will speak on flex design and manufacture at PCB West in September (pcbwest.com).

Materials Supply Chain Security

Between counterfeits and improper handling, the potential for consequences is rampant.

I'M A HUGE fan of the connected world. I've commented previously on the many potential benefits for communities everywhere. Like many good things, however, it poses its own set of challenges. One of these is the "democratization" of cyber-crime. The spread of the IoT means we are all vulnerable in our connected homes, our connected cars, or when enjoying the efficiencies of connected infrastructures and smart services. The potential consequences of cyber-attacks are no longer an issue only for banks, governments or large corporations. The consequences of a hacked car or medical device can be personal, real-time, and in some instances life-threatening.

IoT software protocols and hardware-device security down to the silicon level are being developed to counter a host of potential attacks that can range from stealing stored passwords or intellectual property to taking over devices and systems using malicious firmware. This will be an ongoing battle of "arms versus armor." Other potential security threats such as counterfeiting are more mature, less fast-paced, but costly and potentially dangerous. Counterfeit electronic components are reckoned to cost the industry billions of dollars every year, although the Semiconductor Industry Association points out that the safety implications and potential threat to life posed by rogue components often worth only a few cents each make this a far more serious issue than financially larger black markets such as those for counterfeit high-value luxury goods.

Threats from substandard materials. When it comes to printed circuit boards and materials, counterfeiting can be a problem, but there are other issues to look out for too. The variety of different grades of substrate materials has proliferated enormously in recent years, as many subtly different formulas have been developed to help designers optimize and fine-tune more and more parameters to push performance to the limit. There is often no visible difference between materials of various grades, although properties can vary enormously between special high-end formulas such as low-loss substrates and those for more general-purpose applications. Sometimes the system requirements are so substrate-dependent that even one grade lower can be enough to impair system performance.

Malice or mistake? Not only must materials used be genuine, but fabricators should select the correct grade during manufacture. Incorrect materials could be used through simple errors or poor stock-handling practices, if not an outright desire to cut costs and boost profits.

Products built on low-loss substrates are likely to fail production tests if materials of the wrong grade are used. However, incorrectly specified IMS materials could be less easy to spot immediately. Recently, the number of different IMS grades offered by leading manufacturers has grown enormously due to trends such as LED lighting and e-mobility. Ventec, for example, has 12 different grades of IMS materials to meet a variety of thermal management challenges. The issue here is that system reliability is closely linked to operating temperatures, so if, for example, the emitter for an automotive LED headlamp is built with a lower grade IMS than the manufacturer specified – say a 1.0W/m.K product in place of 3.0 or 3.6W/m.K chosen by the system designers – the error may not be discovered until long into the life of the vehicle. Automotive lighting is no longer designed for easy replacement because LED reliability is presumed to be extremely high. If large numbers of units fail before the warranty period expires, the resulting extra costs could seriously damage the lighting supplier's reputation.

On the other hand, poor handling of materials could result in using over-specified materials, hence unnecessarily higher costs. In either case, the LED emitters will not operate at the design temperature, which could result in unpredictable chromaticity. An operating point just 10% higher could cause a noticeable difference, creating a highly visible quality issue. Other systems deployed in high-temperature environments, such as under-the-hood electronics, including engine management or mechatronic modules, can also be at risk of compromised reliability due to incorrect IMS products.

So, it's important to keep supply chains secure. It's also important for board shops to ensure correct management of their materials and maintain adequate traceability. Materials suppliers can help to some extent by providing services such as indelible marking to help verify both the authenticity and performance grade of the materials supplied.

It's worth mentioning that some engineering problems may indicate the wrong materials are in use, when in fact the underlying reason is somewhat different. We recently helped a customer troubleshoot an RF product that had run into problems. The board design was marginal to get the necessary range and sensitivity for the desired signal strength and power consumption. We traced the problem to circuits built on panels fabricated at right angles to the master sheet used in the original design. The difference in fibers per inch between one orientation and the other was enough to cause signal loss, resulting in a failure to meet the loss budget. It's just one more illustration showing the value of keeping proper control over processes and materials. □

ALUN MORGAN
is technology ambassador at Ventec International Group (ventec-group.com); alun.morgan@ventec-europe.com.

Closing Out 2019 on a Positive Note

Local chapter events, plus a great keynote in North Carolina.

WOW! I CAN'T believe it's December already. The IPC Designers Council chapters had another active year filled with great industry content from various industry events and chapter activities. From chapters that remain very strong to an old legacy chapter being resurrected and a new chapter formed, local entities continue to be active in their respective regions. We finish our 2019 chapter update series by highlighting the Silicon Valley Chapter and the Research Triangle Park (RTP) Chapter, plus some comments on the Designer Certification program.

Silicon Valley Chapter

Chapter leader: Bob McCreight

The Silicon Valley Chapter held its final 2019 meeting Oct. 24 in Milpitas, CA. Thanks to Sierra Circuits for recording the meeting and their complementary slides. Much appreciation goes out to Footprintku and Zuken for their roles in hosting and sponsoring the meeting. The combined team did a great job, and we look forward to working with them again for next year's fourth quarter meeting. We had 35 attendees. The venue was excellent, and the lunch was enjoyable. The topic, presented by Scott Nance, was informative and contained a lot of great PCB design material. I would also like to give a shout-out to Optimum Design Associates for its involvement. The next chapter meeting will be Feb. 13. More details will come in early 2020.

Research Triangle Park (RTP) Chapter (North Carolina)

Chapter leader: Tony Cosentino

The RTP Chapter hosted PCB Carolina 2019 on Nov. 13 at the North Carolina State University McKimmon Conference and Training Center (**FIGURE 1**). The event was a great success. As current president of the chapter, I commend our officers and volunteers for their tremendous efforts to bring such a large event to this region.

The event included an awesome keynote address about IoT by Tom Snyder of RIoT Labs and Gaëlle Fages of Bayer Crop Science, along with breakfast (**FIGURE 2**). Afterward, the show floor opened with 78 vendors of PCB design software, fabrication, assembly, components, materials, and more. The first part of the event included eight technical sessions, followed by a large buffet lunch. The second part of the event included eight more technical sessions. Technical session details are located on the PCB Carolina website, and the actual presentations will be posted soon. The third part of the event included an evening reception with more food and drinks (**FIGURE 3**).

The RTP Chapter arranged two half-day soldering workshops through Circuit Technology Inc. (CTI), which occurred during PCB Carolina. CTI's IPC Master Instructor Angel Deluna taught hands-on soldering workshops in accordance with IPC J-STD-001,

FIGURE 1. PCB Carolina included a STEM program for local students.

STEPHEN CHAVEZ MIT, CID+, is a member of the IPC Designers Council Executive Board and chairman of the communications subcommittee..

IPC-610, and IPC-7711. And in conjunction with PCB Carolina, IPC offered a course the day before the event on design for excellence by Dale Lee of Plexus. Further, EPTAC held IPC Designer Certification Programs for CID and CID+. CID certification was taught by CID Instructor Kelly Dack, and CID+ certification was taught by CID+ (Advanced) Instructor Dave Seymour (**FIGURE 4**).

The RTP IPC Designers Council offers this event to bring designs and engineers together to keep the local community connected and offer opportunities for continued education. We aspire to attract younger talent to this industry by engaging local universities and community colleges because they are our future. This year, we worked with IPC to bring 50 local high school students from five schools who are involved in the STEM program to PCB Carolina. STEM is a curriculum based on the idea of educating students in four specific disciplines: science, technology, engineering, and math. The students were in a structured environment called the Owl Project. During lunch, a panel of industry engineers talked with the students, who then were chaperoned through the exhibits.

This year's event was up in registration from last year's event by 15% (not including the STEM students). I hope to see new faces at PCB Carolina 2020, so start making your plans now to attend.

For 2020, the chapter will hold elections at our January chapter meeting. I have been the RTP Chapter president for the past 10 years, and I plan to step down. I will remain active in an ancillary position to support the chapter as required. I publicly announced my plan to step down as president of the chapter during the keynote at PCB Carolina. I have publicly endorsed current VP Randy Faucette as the next president, and we are working to bring a new face to the VP position.

IPC CID/CID+ Certification Success

We continue to have successful IPC CID and CID+ certification courses as we close out 2019. Our most recent class successes were held in many diverse locations throughout the US and abroad. Classes to mention over the past few months ranged in locations from Santa Clara, CA (PCB West), to Schaumburg, IL; Anaheim, CA; Dallas, TX; Raleigh, NC (PCB Carolina); and Scottsdale, AZ. The last class of the year was held in Manchester, NH. Congratulations again to all those who have successfully achieved IPC CID or CID+ certification. These certification courses are an excellent source of professional development.

And if you are not yet CID/CID+ certified, I highly recommend these certification courses as a path for continued education in PCB design. For 2020 CID and CID+ certification schedules and locations, contact EPTAC Corp. to check current dates and availability. Note: Dates and locations are subject to change, and a minimum enrollment of seven students is required for a class to be held. □

FIGURE 2. Keynoter Tom Snyder of RIoT Labs talks IoT.

FIGURE 3. Thirsty attendees line up for the evening reception.

FIGURE 4. Dave Seymour leads the CID+ certification class.

LAYOUT AUTOMATION Using Advanced PCB Design Techniques

Good PCB design doesn't have to be time-consuming.

by BRENT KLINGFORTH

After 25-plus years of PCB design, I could not imagine going back to designing a PCB as I did in the late '90s or even early 2000s. New technology is constantly added to tools to simplify our job. The key is staying abreast of these technologies. If you are not using advanced techniques like high-speed routing and tuning, placement planning groups, design reuse, plane generation automation and others, your design completion time could be delayed up to 70% or more.

Most designers start a PCB design by grouping parts using cross-probing from the schematic. However, using a spreadsheet-based view (**FIGURE 1**) allows us to quickly see information about components and groups created for each circuit. These groups can be created either in the schematic or PCB layout.

Today, every design contains some sort of I/O interconnect, visual indicators and mounting features that need to interact with a mechanical enclosure. In most cases, the mechanical engineer will define the locations of these objects and even place 3-D models to support their design efforts.

This design example is started by using collaboration data created from Siemens NX. Our ME created the board outline, mounting holes, and connectors based on their mechanical design. In less than a minute we've done the work that would normally take 60 min. or

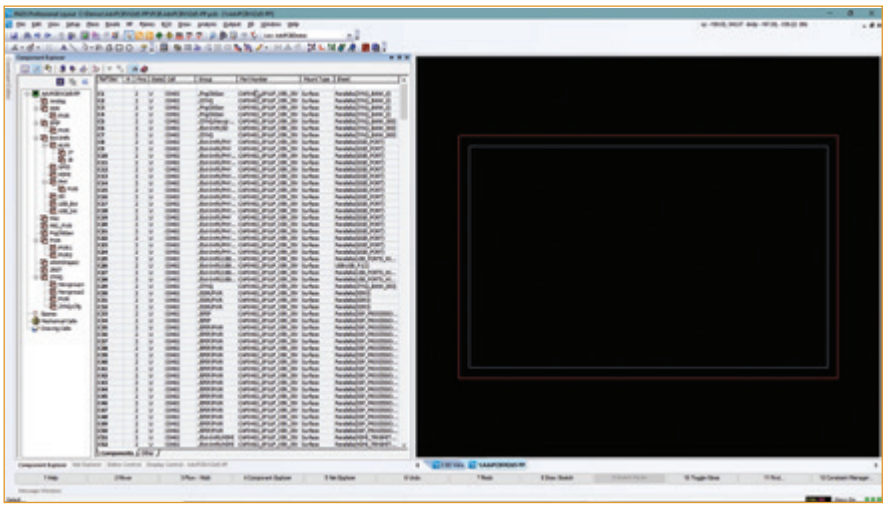


FIGURE 1. Spreadsheets show component and group data for each circuit at a glance.

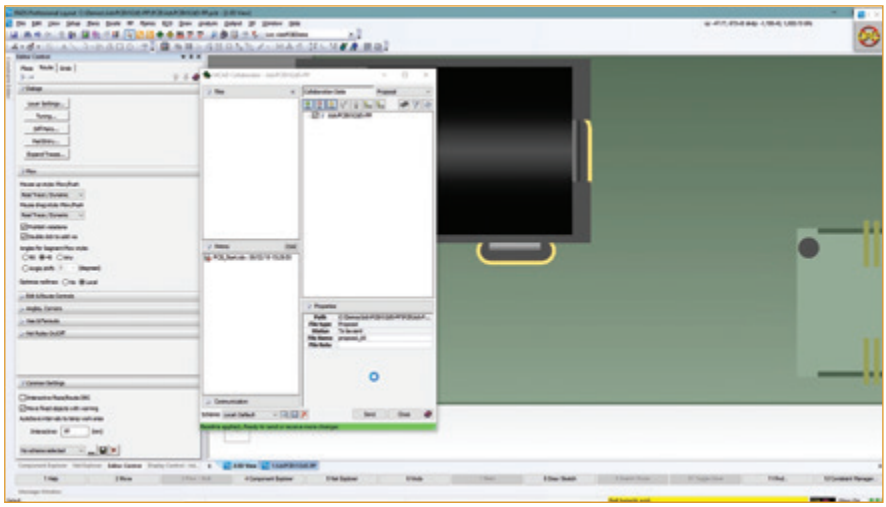


FIGURE 2. ECAD/MCAD collaboration tools allow the ME and EE to exchange data using visualization and electronic data.

more (FIGURE 2). In addition, using drawings means a higher chance of making an error.

Creating a rough placement while seeing interconnect using groups allows us to plan our placement without placing a single part (FIGURE 3). While placing groups, net lines are visible, which vary in thickness based on the connection count. The circle size for a group is defined by the component size and count. More important, we can see net topology between groups, which helps determine routing paths and potential for congestion. In addition, we can create hierarchical groups, one large group for the entire circuit and subgroups for items such as termination resistor, decoupling, etc. This allows use of additional automation for parts to be placed on the bottom or at a particular rotation, which can be assigned to each group or subgroup.

Most schematics and PCB tools can cross-probe to assist with placement. To simplify this task, however, we can use an embedded schematic viewer with simplified controls (FIGURE 4). Passive components always pose a challenge to place, given the large number in a design. Finding passives via the schematic and using sequential placement simplifies this. While placing termination resistors for this connector, we'll use alignment technology to speed placement. As each part is placed and lines up with the axis of another, the part snaps to the edges of that placed component.

At some point, a group of parts will need to be moved. Creating groups for the majority of parts in a design enables moving a selection of components easily.

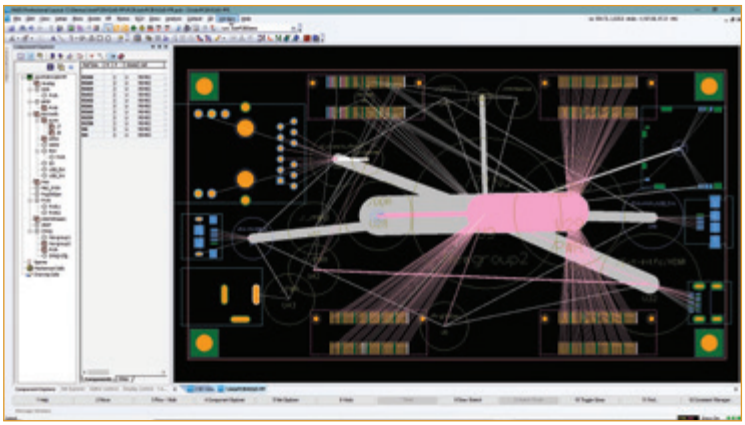


FIGURE 3. Placement groups allow preplacement planning.

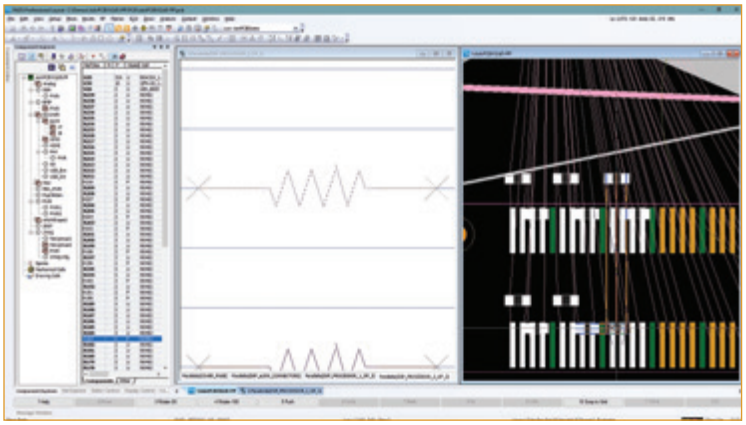


FIGURE 4. An embedded schematic viewer.

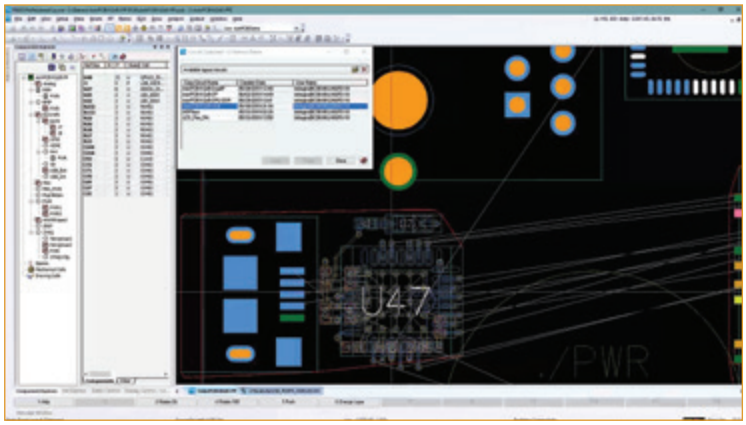


FIGURE 5. Reusing circuits across multiple designers saves time for many functions.

Design Reuse

The ultimate time-saving technique is to reuse circuits from one design in another. Design reuse can be done for the schematic and PCB. Our sample design contains two USB interfaces that use the same circuit but different connectors. The connectors were placed via MCAD collaboration; for the remaining components and routing, we will reuse designs.

Layout reuse includes all items that can be created in a layout, along with those selected upon creation (FIGURE 5). These can include part placement, traces, planes, vias, drawings, keep-outs, stack-up, manufacturing data, and so on. If reference designator values from the saved reuse and the current design are the same, some tools offer the option to automatically choose the correct parts. If there's no reference designator match, you can autoresolve part selection and interactively select the appropriate part for those that do not have a single match. Once placed, the circuit can be customized based on surrounding circuits.

Constraint Management

Many designers try to avoid the constraint management process, except for the basics, as they find it time-consuming and difficult. Constraints are the backbone of good PCB design, however. Without constraints it's difficult to produce a

design that's correct 100% of the time, especially when the design is anything but simple.

Constraint editors define rules that most users feel are overly complex in a simple and structured fashion. Let's start with net classes. Why is the process of creating net classes worthwhile? Classes allow us to organize groups of nets that require the same physical rules. Rules defined on a net-by-net basis will become very unorganized and difficult to manage. Classes provide additional benefits like assisting with viewing, setting colors, design review, using routing automation, etc. The sample design shown in **FIGURE 6** defines 10 net classes. The 100, 90, and 50Ω classes simplify routing by defining trace width impedance rules based on layer. With access to a stack-up editor, designers can also determine single-ended and differential pair trace widths and gaps for impedance-controlled nets (**FIGURE 7**). Find the proper trace width, and the software will calculate the gap. Trace width and gap will automatically adjust depending on the layer its routed on, and you can control which layers will be used for routing. These classes could have been made more granular by doing it based on specific net groups; this decision will be made based on design requirements.

We have not yet defined physical spacing rules between objects. Our net class definition only created a container for a group of nets, the routing layers, trace widths by layer, and differential pair trace width/gap. Every design contains certain technology or requirements that use specific clearance rules, but not every net group needs these special rules. With most tools, you define physical spacing rules with a net class. This makes the process simple, but it does not allow different spacing rules between classes to be defined easily.

Typically, defining class-to-class spacing rules requires more complex and time-consuming processes. If the CAD tools allow you to define specific rules based on technology or requirements, apply rule reuse. Once the general and special clearances have been defined, a simple class-to-class matrix can define where the spacing rules will be used. The benefit here is if a clearance requirement changes, you don't have to remember where those rules were set. Just change the clearance group in question, and it's automatically applied where needed.

What happens when you work on that design with a new processor, DSP, or FPGA where the package is only available in 0.8mm or smaller pitch package? Or what if you're introducing RF circuitry like 5G or designing products with high voltage? With most design tools, you need to be cognizant of where traces traverse boundaries, requiring different trace width and spacing.

To simplify the design process, we could use rules that are specific to an area of the board. When this capability is needed, it by far outweighs almost anything else that would reduce routing time.

Now that we've created the core rules required to design a PCB, what if we have nets sensitive to signal quality, like SerDes differential pairs, DDR, common interfaces like USB, Phy, HDMI, etc.? These all require special electrical rules: length matching, special vias, topology control, trace length control by layer, maximum via count, and differential pair creation. In some rare instances, the need to create rules that rely on length information from other nets or pin pairs may be required to simplify routing.

CAD tools handle this through formulas. These types of rules are classified in some CAD tools as constraint classes. Why a "class?" Because each grouping created will include net assignments, similar to net classes. One might ask, "I've already created net classes. Why do I need to do it again for length rules?" Reason: Net classes define spacing and trace width requirements for nets to be combined, even though they may not have the same electrical rule requirements. For clarification, let's say differential pairs need to be 100Ω, and layer restrictions are not a concern. These nets could include SerDes, DDR Clock and Strobe, HDMI, etc. When it comes to electrical rules, all these would require their own classes, but we can simplify trace-and-space rules by putting them in the same net class.

Differential pairs merit more detail, as these are probably the most common special rule feature used in a design. Whether you're in the schematic tool or layout, ideally you can access the same constraint classes with all the same rules, including creating pin pair definitions and differential pairs. Automation will help create the diff pair associations, so each net pair is done one at a time. Assuming the schematic is correct and diff pair nets are named with a proper suffix (i.e., _P and _N, or something to that effect), it takes seconds to find and group all nets in the design with these suffix values.

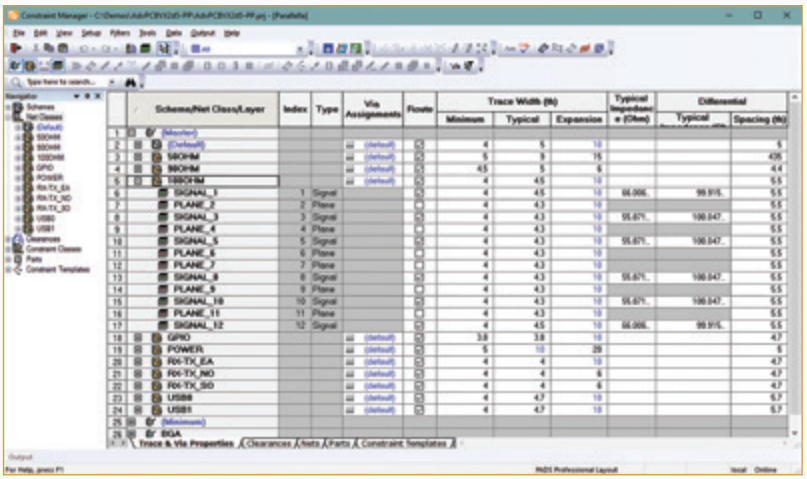


FIGURE 6. Net classes define trace width impedance rules based on the layer.

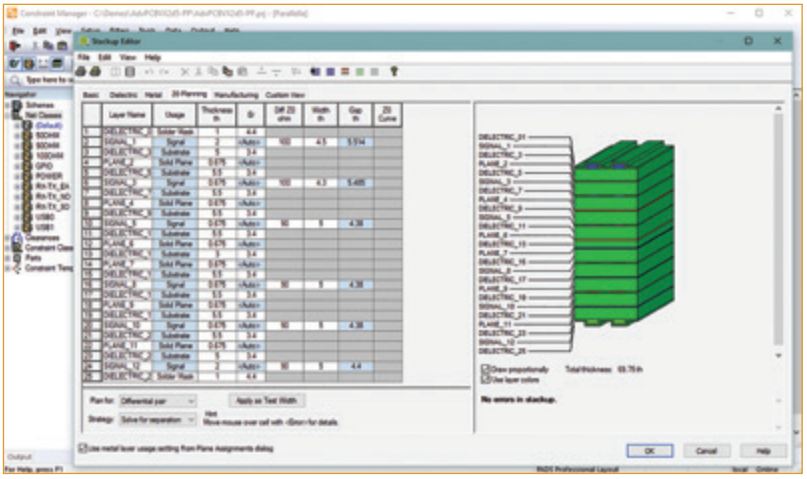


FIGURE 7. A stack-up editor determines single-ended and differential pair trace widths and gaps.

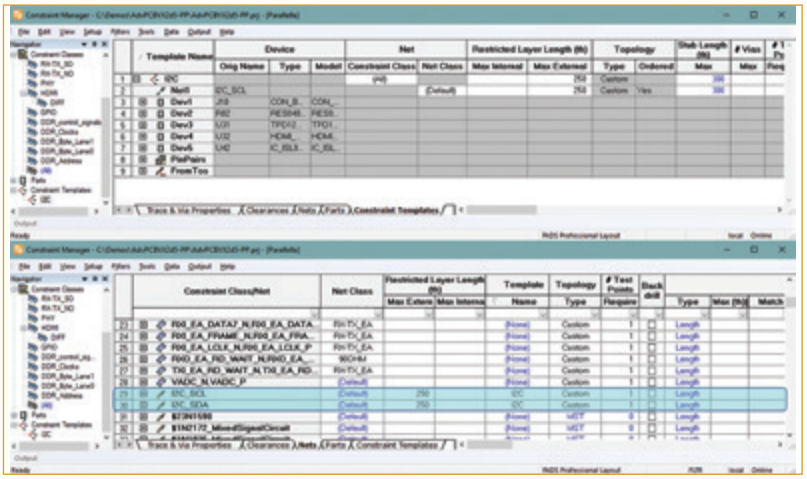


FIGURE 8. Constraint templates.

Another rule reuse option on the electrical rule side is constraint templates. These allow us to take a constraint definition for a net or diff pair with any of the following rules defined:

net class association, topology definition, including virtual pins, stub length, max. vias, length, test point count, restricted layer length, formulas, and special differential pair rules. These can be saved to a constraint template that can be assigned to objects requiring the same electrical rules (FIGURE 8). When we adjust one or several of the parameters, all nets or diff pairs assigned that template name will take on those changes. So, instead of managing the process of modifying all these individually, it can be done in one location. Finally, constraint templates allow the sharing of design rules from one design to another via export and import.

Routing Automation and Length Matching

The simplest form of routing automation is fanning out pins from SMDs. This is the process of using the autorouter to connect short traces to a via, so a net has access to internal layers. To take full advantage of automated fan-out design, rules are required: items such as fan-out direction from SMDs/pins, trace width to be used by net or class (e.g., "power and grounds nets usually require large traces"), via type to be used by net or net class, allowed length of trace, and clearances.

Let's start with BGAs. These devices are, for the most part, the simplest. Choose one of three options and go (FIGURE 9). For non-BGA parts, you have more choices. Take, for example, a high-pin-count connector. Ideally, the power and ground pins are routed to the outside, and all the diff pair pins are routed on the inside to minimize length discrepancies (FIGURE 10). To achieve this, set the fan-out direction for outside, select the power/ground (PG) pins and perform the fan-out. Next, adjust the fan-out direction to inside, select the component, and fan-out the remainder. For tight designs or BGAs with fine-pitch ball spacing, placing vias in the pins of passives or even BGA pads is required. Adjustable on-the-fly settings and finite control make the process that much easier. In our case, we need to place decoupling caps directly under the BGAs, which requires vias to be placed in the pins. After defining a via-in-pad rule in the CAD tool, we can place capacitors at the appropriate locations with no issues.

Now that we've created the appropriate rules and placed our fan-outs, it's time to start routing. This phase of the design usually takes the most time, especially when hand-routing, which involves point-and-clicking each point, with no push-and-shove. It's surprising how many designers today still prefer this method, even when the tool contains interactive routing technology. We recommend investigating the push-and-shove routing capability of the CAD tool. Two automated options are available: interactive push-and-shove for single or multiple nets and sketch routing. Automated methods can cut design routing time by five to 10 times.

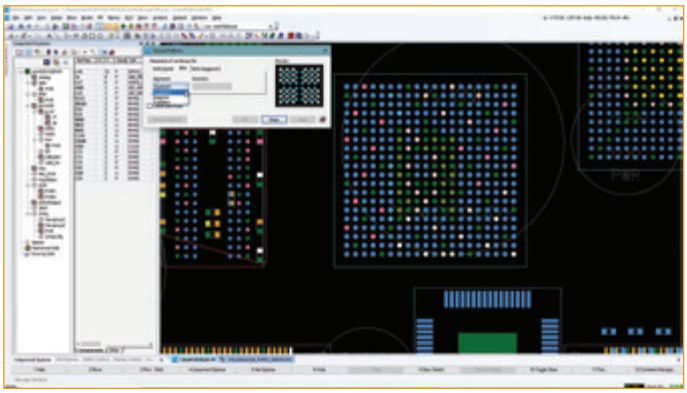


FIGURE 9. BGA fanout options.

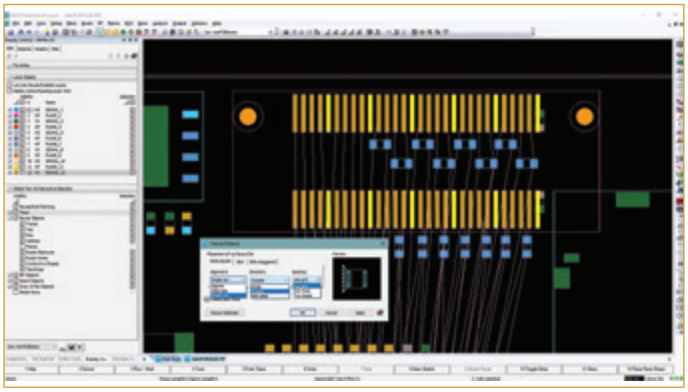


FIGURE 10. Sample connector for fanout.

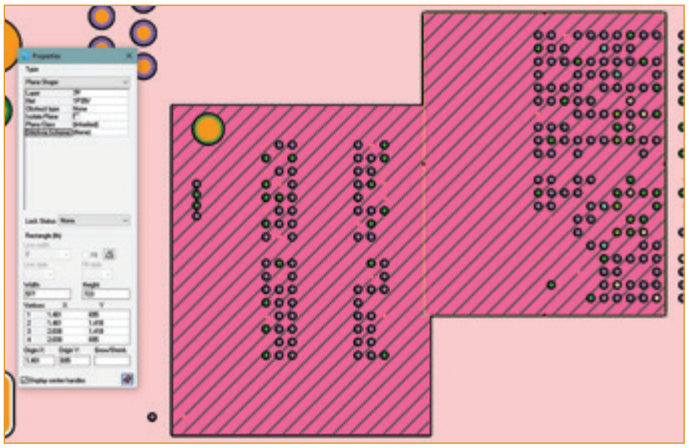


FIGURE 11. Simplified plane shape creation.

Finishing the Design

Aside from documentation, typically one of the last major tasks to complete a board design is creating plane areas. Many of today's designs include 10, 20, even 30-plus plane areas, or very complex board outlines, all of which can consume a good portion of the design time. One type of circuit design that requires special attention is power supplies. For power supplies, we need to keep inductance down and create copper areas that can handle high current. Doing this with traces is not the best option. Using planes and solid connections to pins is the sim-

plest method. Drawing simple rectangles and circles, and using merge-and-cut commands, full shape corner manipulation, and setting per shape plane thermals, allows us to create complex plane areas in seconds to minutes, not minutes to hours.

In addition, when dealing with through-hole pins in power sections, it's far less time-consuming to modify pin thermal settings based on layer and use rather than at the library level, for unlimited flexibility.

I mentioned complex board outlines. We can now create full board area planes in seconds by taking advantage of this shape and not replicating it. Having one central location to control the nets assigned to a layer, which net is allowed to use the route border as its plane shape, and setting the state of the shape facilitates proper design management.

Whether working with a four or 40-layer board, at some point we need to create embedded planes. As showed earlier, using simple rectangles and circles instead of drawing complex polygons dramatically reduces the time it takes to create embedded planes (**FIGURE 11**). Consider these two examples. First, we'll create an embedded plane using rectangles and merging of shapes. What's the advantage of taking the time to merge shapes? It allows us to easily move the shape at any point and change properties. Next, we'll create the same shape using rectangles and merging/subtracting shapes. Having this option gives flexibility, as each design possesses different challenges. To finish our plane area, we'll round all the corners.

All experienced designers must at some point fill a plane area with vias or place guard vias around a trace. Placing these one by one takes forever. In our sample design, we must create a ground plane directly under the RJ-45 connector and fill with vias. Using stitch shape, we can play with several scenarios and choose the most appropriate, as it only takes a few seconds to process. We'll save this configuration in case we create more plane areas requiring via fill. When later creating a shape, we can then assign this configuration (**FIGURE 12**).

Now that we have saved a configuration, if we undo the via stitching, we can assign the new via stitching configuration. To perform the stitching process requires just two mouse clicks and a few seconds to complete the job.

Automation can speed the design process in other areas. Take teardrops. They are not always needed, but when they are, they should not be cumbersome. Controlling the length and width is mandatory; otherwise, some designs may require adjusting far too many traces to add teardrops without creating DRC errors. The CAD tool should allow you to window-select traces requiring teardrops and choose that option with a single click. If the entire design needs teardrops, simply set an option for all pads (**FIGURE 13**).

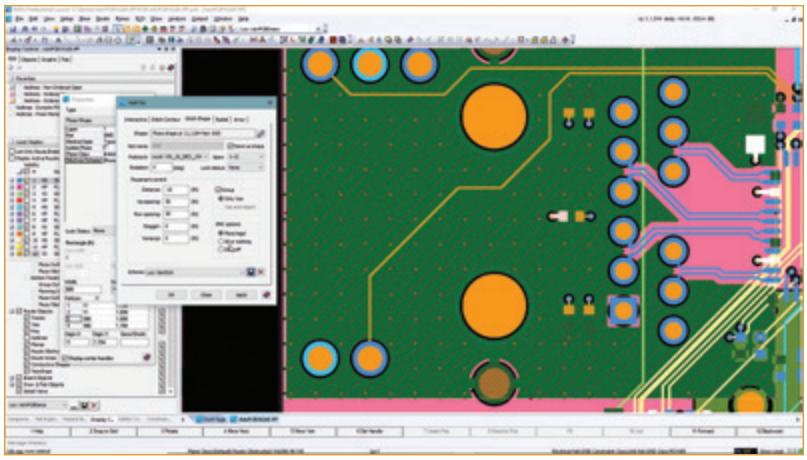


FIGURE 12. Via stitching setup.

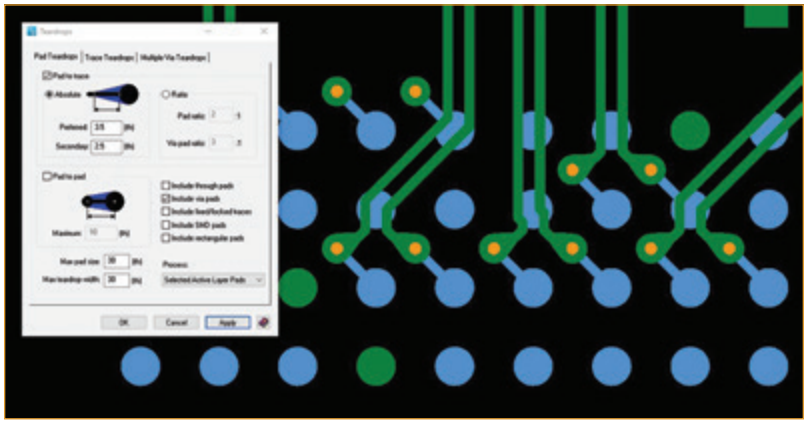


FIGURE 13. Teardrop configuration.

As a specialized function we can fine-tune teardrops by setting curved settings for areas where space is at a premium. Notice how the added copper is not uniform between each side but fills in as needed to make a conformal curve.

For quick adjustments to an electrical constraint – for instance, if we forgot to define a differential pair – use of an add-in window in both the schematic and layout tools can quickly adjust electrical constraints and define a differential pair.

Likewise, say our engineering lead asked for a change to the 100Ω differential pairs and space requirements. We could rip up the traces and reroute. What's faster, however, is to change the trace width and let the tool do the rest.

Good PCB design can be complicated and painstaking. But it doesn't always have to be time-consuming too. □

BRENT KLINGFORTH is technical marketing engineer at Mentor, a Siemens Business (mentor.com). Before joining Mentor, he spent 25 years designing PCBs; brent_klingforth@mentor.com.

ELIMINATION OF NI CORROSION in ENIG and ENEPIG by Using Reduction Assisted Immersion Gold

Could a switch from standard immersion gold reduce plating defects?

by GEORGE MILAD, JON BENGSTON AND ALBIN GRUENWALD

Ed.: This article is adapted from a paper from the SMTA International Proceedings and is published with permission of the authors.

Nickel corrosion in electroless nickel immersion gold (ENIG) and electroless nickel electroless palladium immersion gold (ENEPIG) is occasionally reported, when encountered at assembly, manifested as soldering failures in ENIG and wire-bond lifting in ENEPIG. Although this is not common, when encountered it is very disruptive. Its presence can cause delays, missed delivery schedules, supply-chain disruption, failure analysis investigations, and manufacturer liability.

To highlight and mitigate nickel corrosion defects, the IPC Plating Processes Subcommittee revised the 2002 standard IPC-4552, *Performance Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Boards*. That revision, IPC-4552A, was released in 2017. Work on revision B took place in 2019, and that document awaits a final IPC member vote. Upon release of IPC-4552B, corrosion inspection will become mandatory.

One objective of IPC-4552B is to eliminate nickel corrosion by focusing attention on the defect. Suppliers will have to offer more robust processes, and manufacturers must have tighter process control. One method to eliminate nickel corrosion is reduction assisted immersion gold (RAI). This article addresses the role of RAI gold in eliminating corrosion in ENIG and ENEPIG.

Chemical non-electrolytic gold deposition/plating is the result of a reduction of the gold ion in the solution to the gold metal. Reduction occurs through the supply of electrons. Electrons may be supplied by different methods:

$$Au^{++} + 2e \longrightarrow Au$$

- Immersion gold (IG). Displacement reaction where the substrate supplies the electrons needed to reduce the ionic gold to metal. Immersion reaction is limited in deposit thickness capability as the substrate becomes less available. Under non-ideal, IG will corrode the underlying nickel (Ni).
- Autocatalytic gold (AG) deposition. The electrons needed to reduce the gold ions to metal are supplied by a reducing agent component in the bath. This requires an underlayer of IG to initiate. Nonaggressive; will not produce substrate corrosion. Unlimited thickness.
- Reduction assisted immersion gold (RAI) deposition. RAI gold is a mixed reaction bath. Both immersion and autocatalytic reactions start simultaneously (**FIGURE 1**). As the substrate becomes less accessible, the immersion reaction will diminish, and the autocatalytic reaction will dominate. Non-aggressive; will not produce substrate corrosion. Capable of depositing 4 to 6µin of gold in a single step.

Advantages of RAI IG include:

1. RAI gold is noncorrosive; eliminates Ni corrosion in ENIG and ENEPIG finishes.
2. Economic, one gold bath.
3. Capable of depositing higher thickness of gold (up to 7µin), if desired.

This is in contrast with fully autocatalytic (electroless) gold, which requires two gold baths, one for the deposition of an initial immersion gold layer prior to the autocatalytic deposition.

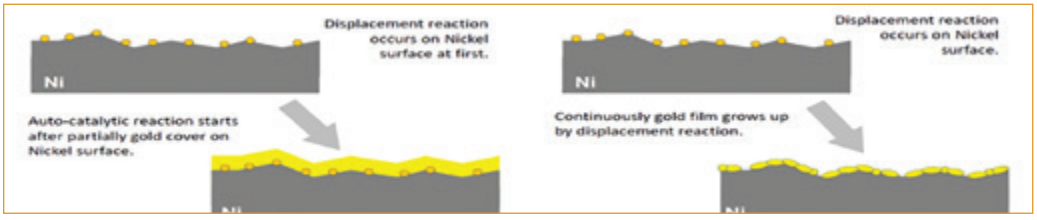


FIGURE 1. Graphic presentation of immersion gold vs. RAI gold.

ENIG and RAI Gold

Ni corrosion occurs during IG deposition. It occurs when the Ni deposit is compromised (uneven with deep crevices) in combination with an extended dwell time in an aggressive IG bath (low in Au content, high in acidity). Process control and reduced dwell time in the immersion gold bath are the primary mitigating methods used to date.

FIGURE 2 shows a 5000X SEM micrograph of a corroded Ni surface after gold stripping. An irregular topography with distinct crevices between the domains is where corrosion initiates and may cause black pad.

FIGURE 3 shows a 5000X SEM micrograph of a non-corroded nickel surface after Au stripping. The Ni deposit exhibits an even topography. This Ni deposit will never produce a black pad.

A new approach to the elimination of corrosion is the use of RAI IG. The RAI gold mode of action does not rely on the displacement/corrosion step as standard IG does; its autocatalytic deposition mode does not create corrosion. In addition, RAI gold can deposit higher thicknesses of gold (3 to 5µin). Some product designs prefer a thickness exceeding the recommended thickness of 1.6 to 2.8µin. Since Ni corrosion occurs during Au deposition, does the Au bath have a role in causing the defect? Ideally, for every single atom of Ni metal oxidized to Ni ion, two Au atoms are reduced to Au metal. What follows is an investigation of RAI gold as a means to eliminate corrosion in ENIG.

Experimental Design

To demonstrate the capability of the RAI gold bath, sample coupons were prepared and run on two production lines (**TABLE 1**). The first line utilized a standard immersion gold bath. This sample was used as a reference/control. The control sample was plated in standard gold for 9 min. to a thickness of 2.8µin. All plating was performed using commercially available plating chemicals.

The second line used an RAI gold bath. The coupons in the RAI bath had two distinct dwell times: a dwell time of 11 min. and a dwell time of 25 min. Traditionally, extended dwell time in the Au bath produced corrosion. The extended dwell time addressed two questions: Will corrosion occur, and what thickness of Au can be deposited with RAI gold?

TABLE 1. Process Sequence and Dwell Time (minutes)

	CONTROL	SAMPLE 1	SAMPLE 2
Cleaner	5	5	5
Micro-etch	2	2	2
Catalyst	1	1	1
Electroless Ni	24	22	22
Immersion Gold IG	9		
RAI Gold		11	25

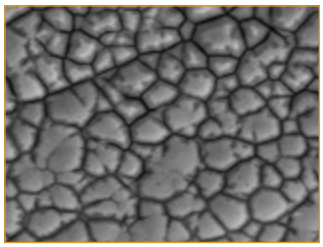


FIGURE 2. SEM of Ni corrosion.

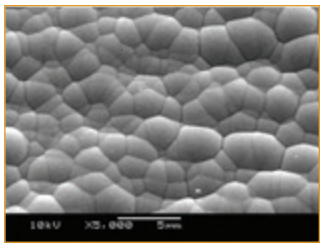


FIGURE 3. SEM of Ni surface.

Results and Discussion

Control. The cross-section of the deposit at 1000X, as specified in IPC-4552A and IPC-4552B, shows a low level of corrosion spikes (**FIGURE 4**). Based on the classification, the spikes are a level 1 or level 2 corrosion, with a product rating of "level 1," per the proposed IPC-4552B. Although this is not cause for rejection, it is a process indicator that implies higher levels of corrosion are possible.

Sample 1. This coupon was plated for 9 min. in the RAI gold to a thickness of 3.2µin. **FIGURE 5** shows the cross-sections at 1000X. The cross-section examination showed a product rating level "0" or an ideal deposit with no signs of corrosion that measured 5.48µin. Here the product rating was also at level "0." **TABLE 2** contains values for thickness XRF measurement for Ni and Au.

Sample 2. It was decided to test an increased well time in the Au bath. This is the traditional method to produce corrosion. In Sample 2, the dwell time in the RAI gold bath was increased to 25 min. The result was a gold layer with a mean thickness of 5.48µin, with level "0" corrosion (**FIGURE 6**).

FIGURE 4. Control sample in standard immersion gold with low level corrosion.

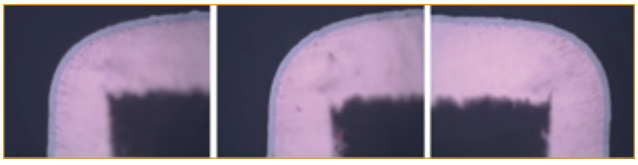


FIGURE 5. Sample 1 RAI gold at 1000X, showing level "0" corrosion/product rating.

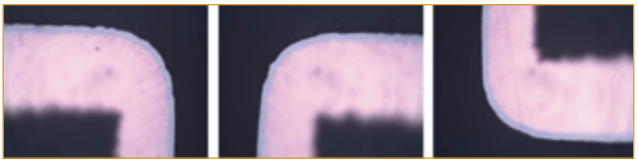


FIGURE 6. Sample 2 RAI gold at 1000X, showing level "0" corrosion/product ratio.

ENEPIG and RAI Gold

The expectation is that Ni corrosion would not occur in ENEPIG, as the Au ions have no direct access to the Ni. This would be true if the Pd layer is impervious to the Au ions. If the Pd layer is thinner (1 to 4µin/0.025 to 0.1µm), it is not totally impervious, and the Au ions may have access to the underlying Ni, offering an easier path to IG deposition. No corrosion would occur.

The effect of the following attributes in creating nickel corrosion were investigated:

- Thickness of the electroless palladium layer
- Type of immersion gold (standard immersion vs reduction assisted immersion gold).

The test vehicle (**FIGURE 7**) in this study consisted of a copper-clad laminate substrate Cu-plated to a thickness of 20µm using an acid Cu electroplating process. ENEPIG was deposited on the test vehicle using two different Au baths. The first was a standard IG bath that ran at an acidic pH of ~5.5 at a temperature of 180ºF. The second bath was an RAI gold bath, also known as a "mixed reaction" bath. All plating was performed using commercially available plating chemicals.

The thickness of the Pd deposit was varied by changing the dwell time in the baths. The rate of deposition over time was recorded. The different thickness Pd layers were individually placed in the respective Au baths for an exaggerated dwell time of 30 min. The exaggerated dwell in the Au bath was by design to ensure some level of Ni corrosion would occur, and there would be a way to evaluate the difference the thickness of the Pd layer would play in Ni corrosion and the impact of the type of Au used.

Test #1 involved varying thicknesses of electroless Pd with standard IG. Test #2 involved varying thicknesses of electroless Pd with RAI gold. After each test, cross-sections of the ENEPIG layer at different Pd thicknesses were evaluated for Ni corrosion using SEM.

TABLE 2. Thickness Values for Sample 1

n= 1	Au 1 =	3.16µin	NiP 2=	175.9µin
n= 2	Au 1 =	3.17µin	NiP 2=	176.0µin
n= 3	Au 1 =	3.08µin	NiP 2=	168.4µin
n= 4	Au 1 =	3.15µin	NiP 2=	177.7µin
n= 5	Au 1 =	3.15µin	NiP 2=	180.1µin
n= 6	Au 1 =	3.14µin	NiP 2=	175.7µin
n= 7	Au 1 =	3.17µin	NiP 2=	178.6µin
n= 8	Au 1 =	3.10µin	NiP 2=	171.5µin
n= 9	Au 1 =	3.20µin	NiP 2=	178.5µin
n= 10	Au 1 =	3.06µin	NiP 2=	176.8µin
n= 11	Au 1 =	3.11µin	NiP 2=	172.8µin
n= 12	Au 1 =	3.08µin	NiP 2=	169.4µin
n= 13	Au 1 =	3.12µin	NiP 2=	167.5µin
n= 14	Au 1 =	3.10µin	NiP 2=	171.0µin
n= 15	Au 1 =	3.23µin	NiP 2=	177.7µin
n= 16	Au 1 =	3.10µin	NiP 2=	168.2µin
n= 17	Au 1 =	3.13µin	NiP 2=	176.2µin
n= 18	Au 1 =	3.15µin	NiP 2=	169.5µin
n= 19	Au 1 =	3.07µin	NiP 2=	169.0µin
n= 20	Au 1 =	3.10µin	NiP 2=	174.5µin

	AU 1µIN	NIPµIN
Mean	3.128	173.8
Standard deviation	0.044	4.096
CoV (%)	1.41	2.36
Range	0.163	12.6
Number of readings	20	20
Measuring time	30 sec.	

TABLE 3. XRF Readings for Sample 2

n= 1	Au 1 = 5.35µin	NiP 2= 156.9µin
n= 2	Au 1 = 5.07µin	NiP 2= 159.1µin
n= 3	Au 1 = 5.19µin	NiP 2= 160.4µin
n= 4	Au 1 = 5.26µin	NiP 2= 161.2µin
n= 5	Au 1 = 5.22µin	NiP 2= 159.1µin
n= 6	Au 1 = 5.08µin	NiP 2= 158.7µin
n= 7	Au 1 = 5.22µin	NiP 2= 157.5µin
n= 8	Au 1 = 5.13µin	NiP 2= 160.9µin
n= 9	Au 1 = 5.17µin	NiP 2= 160.6µin
n= 10	Au 1 = 5.22µin	NiP 2= 158.8µin
n= 11	Au 1 = 5.39µin	NiP 2= 166.4µin
n= 12	Au 1 = 5.35µin	NiP 2= 164.7µin
n= 13	Au 1 = 5.32µin	NiP 2= 166.2µin
n= 14	Au 1 = 5.12µin	NiP 2= 160.0µin
n= 15	Au 1 = 5.31µin	NiP 2= 163.4µin
n= 16	Au 1 = 5.36µin	NiP 2= 165.9µin
n= 17	Au 1 = 6.81µin	NiP 2= 158.4µin
n= 18	Au 1 = 6.62µin	NiP 2= 161.5µin
n= 19	Au 1 = 6.41µin	NiP 2= 164.9µin
n= 20	Au 1 = 6.01µin	NiP 2= 164.4µin

	AU 1µIN	NIPµIN
Mean	5.48	161.5
Standard deviation	0.531	3.058
CoV (%)	9.68	1.89
Range	1.74	9.5
Number of readings	20	20
Measuring time	40 sec.	

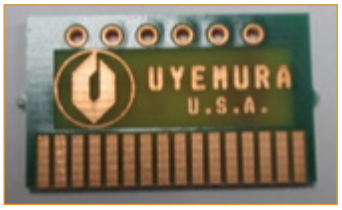


FIGURE 7. Test vehicle.

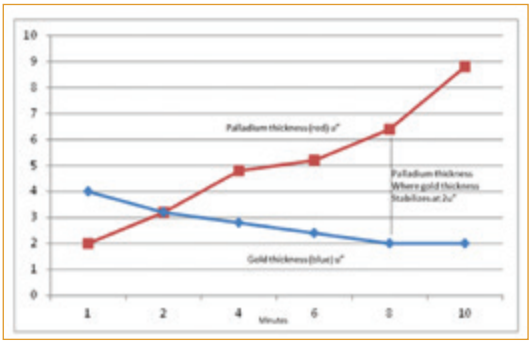


FIGURE 8. A graphic presentation of the data from Table 2.

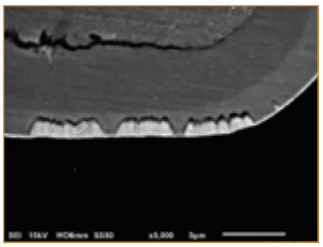


FIGURE 9. Ni corrosion at 2µin (0.05µm) of EP.

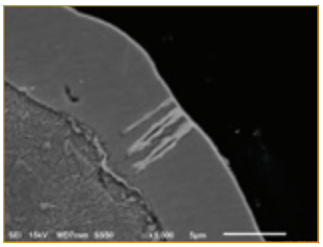


FIGURE 10. Ni corrosion at 4.8 µin (0.12µm) of EP.

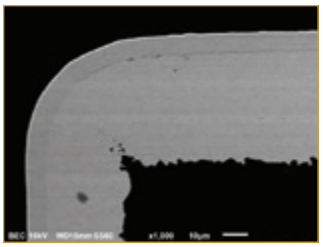


FIGURE 11. No corrosion at 8.8µin (0.22µm) of EP.

TABLE 4. Process Sequence

PROCESS	TEST #1	TEST #2
Cleaner	0	0
Microetch	0	0
Activator	0	0
E'less Ni	0	0
E'less Pd	0	0
IG Standard	0	X
RAI Gold	X	0

Test #1, ENEPIG with standard IG. Six solder test coupons were plated in electroless nickel at a fixed dwell time and Ni thickness (TABLE 4). This was followed by electroless phos-palladium (EP). The coupons' dwell time in the EP bath was 1, 2, 4, 6, 8 and 10 min., giving rise to EP thickness that varied from 2-10µin (0.05-0.25µm) of Pd (FIGURE 8). All six samples were then immersed in the IG bath for 30 min. at 180°F.

Holes from each coupon were then cross-sectioned. Using SEM, 20 corners were evaluated for Ni corrosion at 5000X and 1000X.

The data show Au thickness at the lower EP thickness was as high as 4.0µin (0.1µm) and continued to diminish as the thickness of the EP increased (TABLE 5). Au thickness was limited to 2µin (0.05µm) when the thickness of the EP was 8µin (0.20µm) or greater. The explanation is the Au ions at the lower EP thickness had access to the underlying Ni and proceeded to deposit at an accelerated rate, producing Ni corrosion (FIGURES 9 to 11).

Test # 2, ENEPIG with RAI gold. Test #2 followed the process sequence outlined in Table 4. Six solder test coupons were plated in electroless nickel to fixed dwell time Ni thickness. This was followed by electroless palladium. The coupons' dwell time in the EP bath was 1, 2, 4, 6, 8 and 10 min., giving rise to EP thickness that varied from 2 to 10µin (0.05 to 0.25µm) of palladium (TABLE 6). All six samples were then immersed in RAI gold bath for 30 min.

Holes from each coupon were then cross-sectioned. Using SEM, 20 corners were evaluated for Ni corrosion at 5000X and 1000X. No corrosion was visible with the RAI gold between 2.0µin to 5.4µin (0.05µm to 0.14µm) (FIGURES 12 to 15).

TABLE 5. Thickness at Different Dwell Times and Corresponding Thickness with Standard IG

MINUTES IN EP BATH	EN µIN/µM	EP µIN/µM	IMAU µIN/µM
1	272/6.8	2/0.05	4/1.0
2	272/6.8	3.2/0.08	3.2/0.08
4	272/6.8	4.8/1.2	2.8/0.07
6	272/6.8	5.2/0.13	2.4/0.06
8	272/6.8	6.4/0.16	2/0.05
10	272/6.8	8.8/0.22	2/0.05

TABLE 6. Pd Thickness at Different Dwell Times and Corresponding Thickness with Reduction Assisted IG

MINUTES IN EP BATH	EN µIN/µM	EP µIN/µM	IG µIN/µM
1	255/6.4	1.47/0.04	8.73/0.22
2	255/6.4	2.10/0.05	8.05/0.20
4	255/6.4	3.56/0.09	7.28/0.18
6	255/6.4	4.92/0.12	7.24/0.18
8	255/6.4	6.50/0.17	7.30/0.18
10	255/6.4	7.70/0.19	6.96/0.17

Conclusions

The results show a major advantage to using RAI gold compared with IG. IG showed major corrosion on the Ni layer, particularly at the lower thickness of the electroless Pd layer. The IG accessed the underlying Ni, creating corrosion. One way to minimize corrosion is to increase the thickness of the Pd layer.

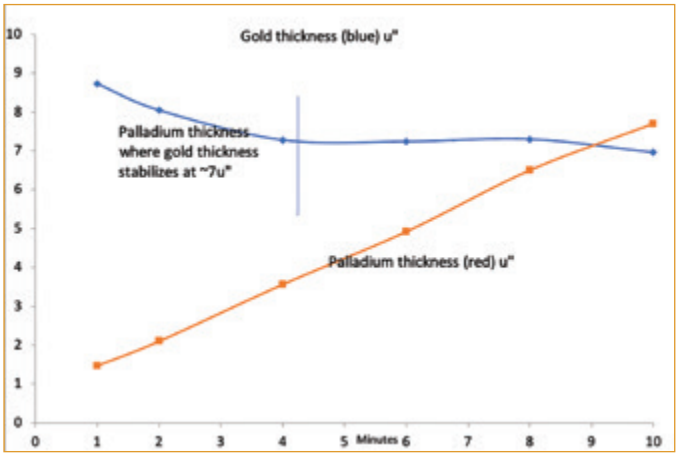


FIGURE 12. Chart of electroless palladium with RAI immersion gold vs. time in the EP bath.

Presently, IPC-4556, *Specification for Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG) Plating for Printed Circuit Boards*, specifies 2 to 12µin (0.05 to 0.3µm) for the EP layer and 1.2 to 2.0µin (0.03 to 0.05µm for IG. The authors of this paper recommend increasing the lower limit of EP thickness to 7µin (0.18µm).

On the other hand, the RAI gold did not corrode the underlying Ni, even at very low electroless Pd thicknesses (1 to 2µin).

The data also show there is a limit to how much Au can be deposited using IG (<2.0µin). In contrast, Au thicknesses of up to 8µin were easily achieved with RAI gold.

The results show substituting RAI gold for IG will not corrode the underlying Ni and permit a thicker Au deposit (up to 8µin) on the Pd substrate. ▫

GEORGE MILAD, JON BENGSTON and ALBIN GRUENWALD are with Uyemura (uyemura.com); gmilad@uyemura.com. Milad is co-chair of the IPC Plating Processes Subcommittee.

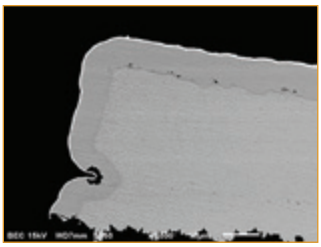


FIGURE 13. No corrosion at 2.0µin (0.04µm) of palladium.

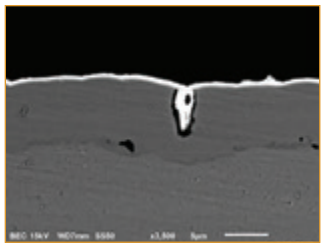


FIGURE 14. No corrosion at 3.4µin (0.04µm) of palladium.

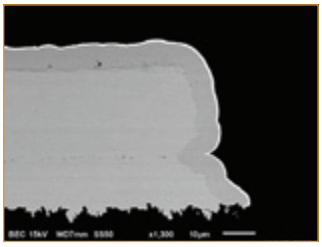


FIGURE 15. No corrosion at 5.4µin (0.04µm) of palladium.

Digital BUILDING BLOCKS

AI and machine learning will shape the coming era of electronics manufacturing. **by DANIEL GAMOTA, PH.D.**

Ed.: This is the third of an occasional series by the authors of the *2019 iNEMI Roadmap.* This information is excerpted from the Smart Manufacturing chapter of the roadmap, available from iNEMI (inemi.org/2019-roadmap-overview).

Smart manufacturing is considered a "journey" that will require hyper-focus to ensure the appropriate technology foundation is established. Several enabling "horizontal" technologies (digital building blocks, data flow, security) are considered the most important to build a strong, agile, and scalable foundation. This article presents digital building blocks, with a focus on artificial intelligence (AI) and machine learning (ML) tools, and digital twins.

Advancements in the development of digital building blocks (interconnected digital technologies) are providing digitization, integration and automation opportunities to realize smart manufacturing benefits. These building blocks will enable electronics manufacturing companies to stay relevant as the era of the digitally connected smart infrastructure is developed and deployed.

Artificial intelligence (AI) and machine learning (ML). AI and ML tools and algorithms can provide improvements in production yields and quality. These tools and algorithms will enable the transformation of traditional processes and manufacturing platforms (processes, equipment, and tools). With respect to PCB assembly (PCBA), AI and ML present several opportunities to aggregate data for the purpose of generating actionable insights into standard processes. These include (but are not limited to):

1. **Preventive maintenance.** Collecting historical data on machine performance to develop a baseline set of characteristics on optimal machine performance, and to identify anomalies as they occur.
2. **Production forecasting.** Leveraging trends over time on production output versus customer demand, to more accurately plan production cycles.
3. **Quality control.** Inspection applications to leverage many variants of ML to fine-tune inspection criteria. Leveraging deep learning, convolutional neural networks and other methods can generate reliable inspection results, with little to no human intervention.

Digital twins. The concept of a digital twin lends itself to on-demand access, monitoring and end-to-end visualization of production and the product lifecycle. By simulating production floors, the PCBA industry will be able to assess attainable projected KPIs (and what changes are required to attain them), forecast production outputs and throughputs through a mix of cyber-physical realities (physical world to virtual world, and back to physical world), and expedite the deployment of personnel and equipment to manufacturing floors worldwide.

Security. As many PCBA industry manufacturers provide services for several customers in a single location, it is critical to closely manage security for internal and external activities. Internally, security is of utmost importance when connecting equipment to networks, managing local data transfer, and leveraging the cloud for data aggregation and computation. A combination of edge/cloud networks, along with protective firewalls and secure gateways, will be essential to fortify a networking architecture. Externally, data will likely have to flow either upstream (from assembler to OSAT), or to suppliers and facilities worldwide, which will encourage a public/private cloud service model.

Deployment. This is theability to deploy the necessary digital building blocks to realize smart manufacturing at different stages of maturity.

AI and ML will streamline the transition of products across the entire supply chain, leveraging data from one segment to improve operational efficiencies in another (e.g., production time, delivery, logistics). There is also a strong sentiment that the factories of the future will employ numerous employees, whose responsibilities will be augmented with AI and ML, as demonstrated with video analytics systems that can monitor production operations, and flag deviations in processes visually.

Advances in digital twin technologies are accelerating as the potential benefits are communicated to end-users. Also, the enabling technologies (hardware and software platforms) are becoming less expensive.

Standardization of data types and formats will be critical to maintain a consistent digital twin across the entire supply chain (SEMI-OSAT-PCBA). Each segment may have its own preferred guidelines or standards, but these standards should be interoperable among the segments.

The model for gradual penetration of the digital twin will follow aligned with ML and AI, with descriptive, predictive and prescriptive analytics shifting decision-making from individuals to broader system-level views that can holistically suggest and make recommendations on a preferred course of action.

R&D and Implementation Needs

Among the key topics that must be addressed to realize smart manufacturing are:

- Definition hierarchy – digital twin, AI, ML, deep learning (DL)
- Education – aspirational versus achievable
- Talent – data and computer scientists, automation, manufacturing engineering
- Data sharing and IP concerns
- Speed of technology deployment versus speed of node introduction mismatch
- Path for adoption – company/industry best practices, consortium-proposed deployment framework, top 10 smart manufacturing metrics
- Open collaboration – technology development and pilot environments (e.g., SEMATECH 2.0). ▫

This excerpt from the *2019 iNEMI Roadmap* is based on the Smart Manufacturing chapter, co-chaired by **DANIEL GAMOTA, PH.D.**, of Jabil.

Bigger is Better at PRODUCTRONICA

The biennial trade show was busy and upbeat, suggesting good times are still ahead. **by MIKE BUETOW**

Four years after making their Productronica debut, there were scores of AVGs and AVIs, but oddly no one at the biennial trade show was talking about them. Benchtop robots were everywhere too, to little fanfare.

What was hot, however, was process machines built for large-format boards, which are increasingly seen due to the 5G rollout and LED ramps, and virtual reality/augmented reality devices designed to enhance worker training and even production. And sensors are in everything.

The trek to Munich revealed a remarkably upbeat mood, especially in light of Brexit, widespread political upheaval, and US trade wars. While traffic seemed lighter than the recent past, Productronica remains the largest trade show by far for the PCB fabrication and assembly equipment markets outside Asia. Show organizers touted 44,000 attendees, a figure that at times seemed almost believable.

The other notable trend was the elevation from a line solution-based approach to total factory management, again led by the major OEMs like Yamaha, Fuji, Panasonic and others, but with a boost from some of the software vendors.

Just about all the major placement companies now offer AGVs, as do several other makers of handling equipment, most notably ASYS. Few spent any time talking about them, however. The sense we got was the devices are too expensive and too limited in function to see mass implementation in the next few years.

AR/VR development appears to have more near-term marketability. ASM and Aegis were among those leading the way. There's no clear standard yet; some OEMs are choosing Microsoft (Hologram) or Facebook (Oculus) systems. Others are going with derivatives of Google Glass. The choice is application-driven. ASM's VR, for instance, uses the classic Oculus-style goggles in concert with sensor-embedded gloves to teach workers how to perform machine maintenance. The gloves provide true tactile sense, adding a welcome element to the practice. The first rollout is for the TX series of placement machines, but ASM has extensive plans to add its other lines to the instruction mix, including DEK printers.

ASSEMBLY HIGHLIGHTS

Smart Factory

Aegis released FactoryLogix 2019.1 MES, containing some 120 enhancements. Its new FactoryOptix platform, which uses an AR similar to Google Glass, is a lightweight tool for assembly operators working in physically demanding spaces where

The biennial trade show takes up six large halls and draws more than 40,000 attendees.

both hands are needed. It has its advantages over bulkier AR/VR devices. Safety glasses can be popped into the frames, as necessary. Workers view their real environment, not a simulation, yet work instructions are easily visible, and full traceability is captured in real-time. "It turns the workers into a data source," said CEO Jason Spera.

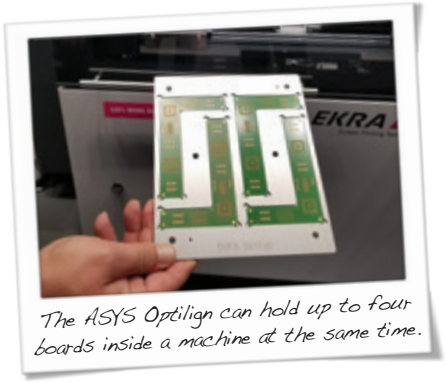
Aegis also rolled out Enterprise Hybrid Cloud, a cloud server that connects to FactoryLogix and rolls up all the line level data into the user's enterprise system, where they can access it with their own IT tools. "Users can't be in a situation where their MES depends on full-time connection to the cloud because, if the Internet goes down, revenue won't get realized," Spera said. "The cloud isn't really about a database; it's about having a central analysis point."

ASM's integrated smart factory software, called Service 4.0, is aimed at solving predictive maintenance problems. It recognizes when calibration is needed, and issues self-repair instructions. ASM sees broad use of IPC CfX to connect machines, while OEMs generate the data and add intelligence, so machines are more predictive. "We want to reach zero downtime and be able to manage all the machines [in a plant] with a single operator," explained Jeff Timms, president of ASM Americas.

The firm is quickly installing the software acquired when it purchased Critical Manufacturing. The tool shows the individual lines or entire factory, including conveyors, feeders, and more. Siplace equipment is automatically configured into the factory software. Moreover, multiple locations can be viewed from a single command center. The auto-populated calendar function shows the machine maintenance schedule and brings to the floor standard instructions for tool repair, including video demonstrations of the activity order.

Handling

As mentioned, ASYS is really shining here. The company is firmly centered on aiding customers looking to a top-down approach to factory management, with new features that help follow material throughout the plant, while automating machine-to-machine processing. A multi-magazine feature on the Speed loader doubles handling throughput. The bare board stack loader has a modified magazine, permitting loading of several boards at a time. A vacuum suction cup on the extractor allows automated extraction of the bare board. All the while, the software is tracking location and inventory. ASYS's incoming material station can relabel a reel with a unique ID and load it inside a dry tower, while an optional embedded x-ray counter tracks the parts. ASYS, of course, makes component cabinets too, since its acquisition of Totech.



The ASYS Optilign can hold up to four boards inside a machine at the same time.

Here, the author sports its FactoryOptix glasses.

Aegis was one of several firms showing AR/VR tools adapted for factory maintenance and training. Its FactoryOptix glasses can be used to access hands-free work instructions.

Printing/Dispensing

Released earlier this year but perhaps overlooked, ASYS's Optilign can sit multiple boards in a carrier, for single-part printing. A fiducial camera checks position and repositions inside the carrier and can print all parts at the same time to increase throughput. Up to 50 parts fit inside the carrier.

Multicarrier can fit up to four carriers inside a machine at the same time, and moves them to the print stage at once, for simultaneous printing. It also performs single-wipe post-print. ASYS sees this as the future of printing: collimating parts for single-stroke print and single-stroke wipe, then re-separating the parts.

ITW EAE's Prodigy dispenser added a large form factor for dual-lane operation. It now handles up to 10" boards on each rail. A passive IR sensor enables closed-loop monitoring of temperatures all through the machine.

The company's Momentum II printer has two noncontact sensors for monitoring paste temperature: one on the paste cartridge and one pointing toward the stencil. They are designed to prevent operators from inserting a new cartridge if the temperature is out of range, and support traceability requirements for various end-markets. The printer pulls the paste specs from the user's MES, and the sensors can stop the printer if the temperature goes out of spec during operation. A paste height monitor allows operators to define the range and alerts users to out-of-spec conditions. The Edison stencil printer line now has a staging function, allowing up to three boards on a single stage conveyor. Built-in buffering capability absorbs upstream delays.

ASM released DEK TQ, a stencil printer with dual-lane capability and optional auto-coplanarity.

ESE's US-8500X handles boards up to 850 x 610mm, with reported accuracy of +/-25µm and a 13 sec. cycle time. The US-2000DXH handles smaller boards (350 x 250mm) at the same accuracy but with a 7 sec. cycle time.

LPKF this year upgraded its MicroCut 6080 stencil cutter to create apertures of 18µm or 10µm, and throughput is now up to 33,000 apertures between 10µm and 125µm.

Kyzen touted its E5361 stencil cleaner, which can be used

on the printer or in a cleaning system.

Fuji's new NXTR PM stencil printer has a dual-lane conveyor, and automatically calculates printing conditions and makes on-the-fly updates. Its auto-solder transfer feature can load paste from the front of the machine on-the-fly.

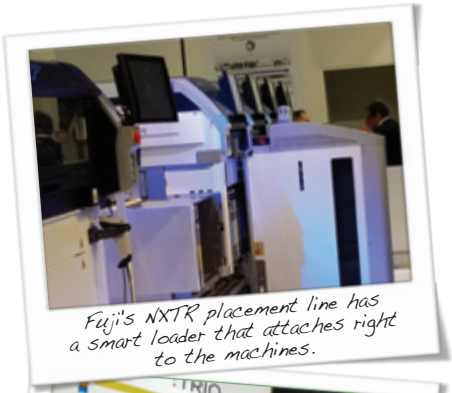
Nordson Asymtek continues to enhance its fully automatic conformal coating concept. The Panorama S-Line uses the area below and adjacent to the conveyor as part of a 10-zone heater. It reportedly cuts the overall line footprint by 50%. Nordson also added progressive cavity pumps to its Forte dispensing platform, which is a faster version of the Spectrum II line.

Speedprint expects to roll out new software in 2020.

Placement

Full-line solutions are the name of the game for the major placement companies. Yamaha showed YST15, an intelligent storage system released at the beginning of the year. It has implemented a solutions engineering division in Europe, which works with customers on integration. Its Advanced Technology Center, launched last year in Japan, is working on AR, big data and self-learning projects. Yamaha Factory Automation, a unit focused on robot technology, has expanded from Japan to Europe and the US.

ASM showed how an operator working in concert with an AGV can move material and changeover lines with minimal manual involvement. In its demo, the operator's role was reduced to feeding new tape into the placement machines, while the AGV did the rest. A tape disposal system collects all waste and transports it away from the line.



Fuji's NXTR placement line has a smart loader that attaches right to the machines.

Posalux's Ultraspeed Trio three-head drill.

Fuji showed the NXTR, a 50,000 cph machine with moving smart loader, that attaches via a rail system to feed up to three placement machines. The loader has sensors for contact detection, parts, and panel height.

Hanwha launched its 520M placement machine in Europe. The new dual-lane platform has two heads, making it lighter, new MMI software and new intelligent feeders.

Juki upgraded its RS-1R component mounter with a Takumi placement head, an eight-nozzle version that automatically adjusts pick-and-placement height on-the-fly.

Soldering/Materials

ITW EAE's Zeva selective solder line now has fiducial recognition for improved accuracy. The non-wetted nozzle has a single direction overflow, and couples with supplemental nitrogen to automatically perform debridging. Board warpage is compensated for automatically as well. The 16 x 20" max. board size is set to be increased. ITW is moving production of its selective machines to Camdenton, MO.

Thermaltronics' new inline soldering robot, TMT-9900S, has an onboard camera used to center and click on the points to solder, locate fiducials for alignment and assist with operator programming, and a laser to align the tip to the board height to ensure proper offset and correct for warpage.

Seho's SelectLine C selective soldering line is designed to handle long assemblies. The new mode for continuous flow eliminates stoppages for fluxing or soldering; instead, the flux and soldering stations move on a bottom-side gantry in the x and y axes while the board is moving. Operators input the flux and soldering path based on a scan of the PCB. This was one of the true new ideas seen at this year's show.

AIM showed a pair of new cored wires: RX 18 for lead or Pb-free machine soldering and CX 18 for hand soldering. Its new paste and bar facility in Malaysia should be online by year-end.

JBC Tools' JNASE rework station regulates temperature and airflow at very low levels in order to avoid movement of adjoining components, making it capable of reworking parts sized down to 008004 components.

ITW's Centurion convection reflow has an optional nitrogen-to-air switch, and reportedly saves nitrogen that is in the machine when switching to air mode. The Dwellflex 4.0 tool on its full tunnel wave soldering systems can adjust contact wave speed on the fly, allowing fast switchover from high mass to low mass boards.

Indium is adding a simulation lab in China, and is moving into new headquarters in Clinton, NY, and converting its former HQ to a manufacturing plant. An additional factory in India is up and running, and expansion is coming in Singapore.

There was not as much movement on vacuum soldering as two years ago. Rob Dimatteo of BTU said interest is high in vacuum to reduce voiding.

Weller made a jump with its station-level connectivity to enhance traceability. Its WX smart platform, coming in the second half of next year, embeds electronics in solder tips to measure the number of joints soldered and when they were soldered, track tip life, and feed data back to the ERP system for reordering. If a tip is moved to another iron, it "remembers" the profile, offsets, and related parameters. An auto-calibration tool can adjust to the correct temperature in seconds. A line

Industry counts on SEMI standards.

SEMI is the global industry association serving the product design and manufacturing chain for the electronics industry.

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semi™

manager can track productivity in real-time via a control panel. The system has a touchscreen interface, and modules for adding hot air or a desoldering vacuum are stackable to conserve bench space. Weller also mentioned its new custom tip service, with a two- to three-week delivery time. Also due in 2020 is the Robot Kit, a soldering tool that attaches to a universal robot and with optional optical recognition to eliminate programming.

Inspection

"2-D inspection is dead" was the refrain from the AOI companies. MIRTEC highlighted its new AI deep learning function. The algorithm takes Gerber and marries it to centroid information, compares it to an internal 2-D and 3-D model database, and assigns the part type and process parameters for each SMT device. Over time it reportedly can cut programming time to around 15 minutes. It comes on the MV-6 Omni, which combines SPI and AOI in the same machine. It is also on the new Alpha 3-D SPI/AOI, which foregoes the traditional moiré approach in favor of an undisclosed "hybrid" technology said to use "close to" real data – basically, less filtering of the raw machine data – to show clearly what is taking place at the solder joint. Alpha has four 18Mp side cameras and a 12Mp topdown camera and can adjust to 35mm high parts.

MIRTEC's Alpha 3-D SPI/AOI has an AI algorithm that "learns" and assigns part type and process parameters for each SMT device inspected.


Direct imagers and inkjet printers, such as this one from Microcraft, drew plenty of interest.

Viscom showed the X8068SL, an x-ray capable of handling parts up to 20kg, such as inverters, chargers and batteries. It sees applications for direct bond copper (DBC) and products where voids are a major issue. The new S3013 Ultra 3-D AOI offers 80mm upper transport clearance and has eight angular and orthogonal views for press-fit and plated-through-hole inspection. 3-D wirebond inspection is next, Carsten Salewski noted.

Koh Young's Ksmart process control software now has an AI engine that, as it recognizes parts and develops an internal master library of shapes and packages, can cut programming time by 80%. The Zenith Alpha 3-D AOI has a fifth projector capable of inspecting 22mm-high parts.

Saki has expanded its R&D operations in the Czech Republic. Its new 3Xi-M200 3D-CT AXI is designed for inspecting insulated gate bipolar transistor power modules and can handle large boards (360 x 510mm) using a two-step process.

Omron has a new inline CT/AXI called the X700, which features single constant measurement for higher throughput, and offline teach capability. It checks both sides of a board at the same time.

Baker Hughes (aka GE aka Phoenix X-ray) showed the Microme x neo, a combination AXI and planar CT system. It has a changeable axis fixture that can be added for 3-D CT (in a different direction). A micro CT inline scanner, called Phoenix speed scan HD, has a 25µm to 50µm resolution and a sub 60-sec. cycle time, and is for complex assemblies, injection moldings and batteries.

ASM showed its new 5D SPI, called Process Lens.

Routing

ASYS showed its Divisio 5100 inline router, the first "smart generation" machine. Every sensor in the system feeds back to the PC. It recognizes use patterns and builds a know-how base, from which alerts are sent to users as spindles become worn. Starting when an order comes, a digital model of the entire machine speeds the configure-to-order (CTO) process. The new Divisio 9000 router uses a green laser for separating flex circuits or thin FR-4 substrates. The laser and guidewave are fixed, leaving no moving parts.

FABRICATION HIGHLIGHTS

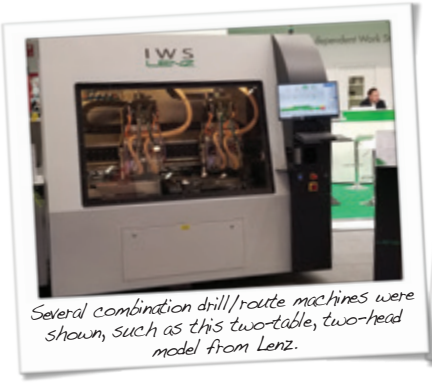
Fabrication is always the lesser twin at Productronica. Fab suppliers take up less than one hall, compared to four for assembly and test. There was, however, more equipment than we have seen the past few shows, with a clear emphasis on large format handling. The downside? Most of the machines shown weren't new.

Polar Instruments has added backdrilling to its Speedstack PCB stackup design tool. Designers can now show fabricators where they want via stubs removed.

Ventec is rebranding its laminates to reflect the potential end-use markets. Expect to see the term AutoLam and, next year, AeroLam.

PrintProcess showed Opal, a tabletop system for layup optical alignment and prebonding. It features four-camera post-etch alignment, for pinless layup and prebonding, innerlayers and coverlays. It can be used on rigid and flex substrates.

First EIE had a lower cost direct imager: EDI 300. It was one of several direct imagers shown, many of which, while not debuting at Productronica, came out in the past year. Another new one was from Screen, whose Ledia 6H has three wavelength light sources for broader coverage of the wavelength regions for exposure, significantly expanding the number of supported resist types. It was shown by Ucamco, which released Iamcam frontend software, a workflow system that



Several combination drill/route machines were shown, such as this two-table, two-head model from Lenz.

ASM is using VR for training operators on machine maintenance.


Fabrication equipment was more plentiful than in years past.


Inside the Nordson Asymtek Panorama S conformal coating line.

automates CAM. According to the company, starting with any dataset, users can input variables such as the finish and copper weight, and it will program the CAM station automatically. The tool, now in beta, is built on Ucamco's Integr8tor engineering platform, with AI added.

RG Elektro-Technologie debuted a pair of machines: the TM-600 PCB printer and the LZ-400 laser marking system, which features a Keyence laser.

Lenz showed LWS combination drill/router, which has a 610 x 650mm working area, two heads, and spindle speeds up to 200rpm.

Schmid updated its InfinityLine etcher with the model A+, which adds automation.

The Taiyo Vision M109SC is a semiautomatic final visual inspection. It has a 5µm or 10µm camera with adjustable title angle and LED illumination. It handles PCBs up to 300 x 500mm.

The Shoda Techtron MVC-720C v-groove scoring machine has an optical scorer, auto-load and unload, and optical alignment. It handles PCBs from 0.3 to 3.2mm in thickness, and max panel size of 720mm.

We saw more than two dozen EMS companies exhibiting, the most we can remember. They ranged in size from top-tier ODMs like Jabil to Tier II firms such as Computime and many smaller local and regional players, mainly from Eastern Europe. Several of them are smallish OEMs that have launched EMS services in the past few years. Conversely, there appeared to be fewer fabricators than in the past.

To call Productronica a massive show is a gross understatement. There are over 1,500 exhibitors, and it's impossible to see everything. Still, if trade shows are a barometer of industry health, the current electronics expansion has some life left in it. ▫

MIKE BUETOW is editor in chief of PCD&F/CIRCUITS ASSEMBLY; mbuetow@upmediagroup.com.

Board Buying, continued from pg. 18

Be a big fish. Leverage your PCB spend by using a few vendors, as opposed to diluting your buying power over many manufacturers. It gives you more bargaining power. This applies regardless of the value of individual purchase orders.

Be wary of amortized tooling. It is easy for manufacturers to hide tooling costs within the piece price. It is also easy to forget – and PCB suppliers hope you do – that the tooling costs have been hidden. You shouldn't pay for tooling indefinitely. There is a reason some PCB suppliers have attractive piece pricing with higher tooling costs and vice versa. If tooling is amortized in the piece price, note on the purchase order that the piece price must be reduced once tooling charges have been fulfilled.

Tooling and test charges are real costs assumed by the PCB buyer over the years. I believe board buyers should ask why they must pay for an electrical test fixture (or program) to prove the manufacturer built the board as designed. If it wasn't in the Gerbers, wouldn't a short or open on a board be the fabricator's fault?

It might be time for the PCB industry to challenge the assumption that buyers will pay for tooling and testing. Until it does, buyers can reduce those costs by knowing how to leverage their annual PCB spend and properly navigate relationships within their PCB supply chain. ▫

In MEMORIAM

A look back at friends and colleagues who left us in 2019.

Joseph Boyd, 98, CEO, Harris Corp.

Gary Burrell, 81, cofounder, Garmin.

Dominick Frank Canace, 87, electromechanical and PCB printed circuit designer with several companies including Tyco Electronics.

Andrew Chase, 55, president and CEO, Sunburst EMS.

Celia Mora Cuadra, 89, PCB assembler, Regitel, Grangers and Lipton Industries.

Carolyn (Puskas) Davis, 76, ex supervisor, Printed Circuit.

Woodie Flowers, Ph.D., 75, robot inventor, co-creator FIRST Robotics.

Tom Gardeski, 75, technical and marketing manager for DuPont, ICI Americas, 3M and Sheldahl; multiple patent holder, chairman of IPC flexible circuit subcommittee.

Robert Gilmartin, 67, founder, Quickdraw Engineering.

Vikram Jandhyala, 47, founder, Nimbic.

Harold Hyman, 91, metallurgist with Alpha Metals HTC, Dynapert, SRT and VJ Electronix.

Mark G. Kassey, 61, former circuit board plater, Circuit Inc.

Darrell J. Lowrance, 80, founder, Lowrance Electronics; developed the first graph recorder and first integrated sonar/GPS unit.

Ed McBain, packaging engineer with Zilog, Harris, Promex and others.

Ralph Morrison, 91, PCD&F contributor and author of more than 12 books on currents and voltage in PCBs.

Michael Mügge, 56, sales engineer, Viscom.

Laurence "Larry" Murphy Jr., 82, salesperson, Alco Electronics.

Mamie L. Robbins, 87, electronics technician, United Technologies.

Betti Mae Sheldon, 89, mechanical engineer and PCB designer, Tektronix.

Ruth R. Spira, co-founder and co-chairwoman, Lutron Electronics.

Thomas Stearns, 86, flex circuit engineer, inventor, author of *Flexible Printed Circuitry*.

Richard Wilson, 61, editor, *Electronics Weekly*.

Steven "Willy" Wilson, 67, ex operator, EMD and Benchmark Electronics.

FISH FINDER
Lowrance

PATHFINDER
Burrell

METAL MAN
Hyman

PACKAGING GURU
McBain

FLEXIBLE THINKER
Stearns

EMI ANALYST
Jandhyala

Dog Ears and Witch Hats

Achieving printing nirvana is largely dependent on solder paste material, print speed and deposit release.

AHHHHH ... screen printing utopia. We process engineers strive for this existence. In a perfect process, printed solder paste would emerge from the stencil as exact replicas of the aperture shape: nice, flat, brick-like deposits. And, while modern printers and advanced materials get us close, solder paste is still, well, solder paste. The materials are not inks; they have a grain structure that is getting smaller in size and distribution and is suspended in flux. Try as we might, with these particles, there will be material undulation at best, and flat paste surfaces will likely never be a certainty.

With printing, we must be pragmatic. It's not a digital process, and many variables come into play. The goal, of course, is to fill all the apertures on the stencil fully with solder paste to obtain the best deposit shape and volume possible. This is easier said than done, as the range of aperture sizes across a stencil can be broad, with 1mm square, 300µm and 200µm openings next to one another. Each of those apertures – from the very large to the very small – must be filled. Since printing with different thickness stencils is a nonstarter (generally and practically speaking), compromise is required, and that challenges our utopian ideal. Squeegee pressure, stencil thickness, print speed and separation speed must be balanced to accommodate variations in required deposit sizes. When all inputs aren't optimized and in perfect balance, solder deposit shape differences can have the potential to introduce process problems. Known in the printing world as "dog ears" on square or rectangular deposits and "witch hats" on circular deposits (**FIGURE 1**), these solder paste deposit peaks may be defect bugbears, especially in the world of high-density, miniaturized assemblies.

Like-minded process engineers out there, however, may be asking if these small peaks really matter. After all, provided solder paste is deposited in the right volume, in the right place, at the right time, then the outcome should be acceptable. Assuming the printing machine is running at the right speed and process pace (the right time), and the SPI machine verifies the proper location (the right place) and quantity (the right volume), then what problems could these small peaks really cause? Depending on the size and location of the dog ears and witch hats, these seemingly inconsequential paste misshapes may contribute to defects – both in placement and reflow. Very small components like 01005s, for example, may skew during placement if the paste peak is too high. While one edge of the component is seated in the paste, a dog ear may prevent the opposite end from being positioned properly. Additionally, with very large material peaks, paste may be dislodged during subsequent processing and cause bridging during reflow.

Preventing dog ears and witch hats from occurring depends largely on the solder paste material, print speed and deposit release from the aperture. So, keeping other variables in balance, what is the best approach to try to minimize these shape abnormalities? Not surprisingly, there are many factors and multiple approaches to consider, depending on the assembly being produced. Here are some probable fixes:

- Separation speed and distance. Stencil separation speed can influence the number of dog ear and witch hat occurrences. Some materials adapt better to a fast release, some to a slow release. My general rule of thumb is if using a fast printing paste (>150mm/sec.), release the stencil quickly (20mm/sec.). With a slow printing paste (between 50mm/sec. and 70mm/sec.), a slower release (5mm – 10mm/sec.) is advised.
- Solder paste. Some solder pastes are just more prone to these peaks than others, so try a new material. While solder requalification is quite an undertaking, leverage a significant product or process change as an opportunity to initiate a material evaluation.

continued on pg. 43

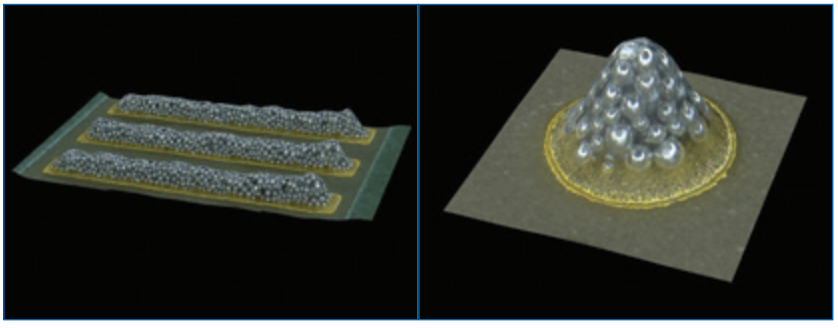


FIGURE 1. Solder paste peaks of dog ears (left) and witch hats (right) may seem benign if the material volume and location are correct, but they can be problematic in certain circumstances.

CLIVE ASHMORE
is global applied process engineering manager at ASM Assembly Systems, Printing Solutions Division (asmpt.com); clive.ashmore@asmpt.com. His column appears bimonthly.

What Solder Ball Size Variation Can Tell Us

Measuring BGA joints can reveal process problems.

THIS MONTH WE show variation in the size of the solder joints on a section of a BGA. Measuring variation on solder ball size after reflow is useful. Even better is when measurements are taken automatically with an x-ray system, as this provides a good comparison tool between NPI and production builds.

Measuring NPI build, and saving the measurement data, provides a good point of reference when problems are seen on a build. It is also useful when moving between contractors or in the event of changes due to other process modifications.

FIGURE 1 is an x-ray image of the corner of a soldered BGA. There is variation in joint size from the device edge to the package center. Variation in ball size most likely indicates warping of the device in the center of the package or at the edges.

We have presented live process defect clinics at exhibitions all over the world. Many of our Defect of the Month videos are available online at youtube.com/user/mrbobwillis. ▫

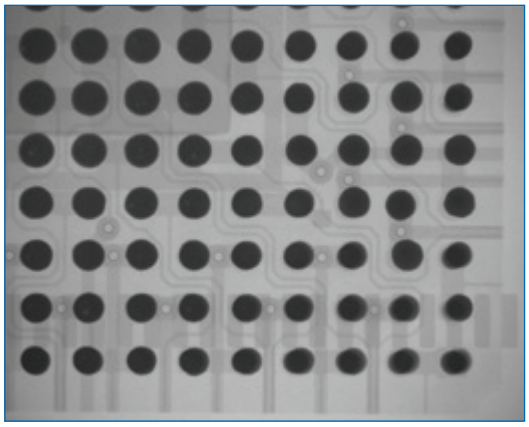


FIGURE 1. This x-ray of the corner of a soldered BGA indicates possible device warping.

BOB WILLIS is a process engineering consultant; bob@bobwillis.co.uk. His column appears monthly.

The Flexperts, continued from pg. 21

tear open sealed bags as they arrive and toss them on the shelf unsealed. If your receiving department does need to open the sealed bags for incoming inspection, they will need to reseal them (with the desiccant and indicator included) before they are put in storage.

The other issue affecting long-term solderability is the final finish. Far and away the most widely used finish in the PCB industry today is ENIG (electroless nickel immersion gold). Other lesser-used finishes are ENEPIG (electroless nickel electroless palladium immersion gold), HASL (hot air solder level), OSP (organic solderability preservative), immersion tin, and silver. Many variables impact the total solderable shelf life of these finishes. For instance, gold thickness and prepackaging contamination of the gold by skin oil or other residue can affect the shelf life of ENIG- or ENEPIG-finished PCBs. Very thin solder coating from HASL can result in reduced solderable shelf life of solder finish. In a nutshell, if the circuits are in sealed bags, you are safe to assume they will remain solderable for two to three months for silver, tin and OSP finishes, and six to nine months for HASL, ENIG and ENEPIG finishes. These estimates are conservative but safe. In practice, the latter three finishes should be good for well over a year, but again, many variables affect this. If long-term solderability is a concern, it is advisable to discuss this with your supplier, so they can take the necessary precautions to ensure maximum shelf life. ▫

Screen Printing, continued from pg. 42

- Stencils/stencil coatings. If solder paste gets stuck in the corners of the aperture, it can pull paste up on release due to surface tension and cause material peaks. Using a stencil coating inside the apertures can encourage a more uniform release. Of course, the release characteristics also come down to the stencil manufacture quality, the type of stainless steel used (standard or fine grain) and stencil tension integrity, so be sure to evaluate these factors too.
- Changing the aperture shape. Putting radii in a rectangular or square aperture can encourage a cleaner release. This adjustment minimizes the tendency of material to stick in the corners of the aperture, which is where the highest surface tension is present. Suggest your stencil manufacturer provide 20µm radii corners. It may reduce dog ear or witch hat occurrences.

Printing is a challenging process and getting increasingly more demanding with modern board designs. It's not enough to rely on SPI data alone, and, often, good old-fashioned process engineering insight is required. ▫

HIGH-FREQUENCY MEASUREMENT

Micro Prober MP series measurement systems (MP502 and MP502-A) continuously inspect high-frequency characteristics of PCBs. Enable high-speed, high-accuracy inspections of characteristics of actual product patterns when combined with a commercial vector network analyzer. High-precision positioning (+/-20µm).

Yamaha Fine Technologies
yamahafinetech.co.jp/en/

PARTS LIBRARY MANAGEMENT

Concord Pro cloud-based software platform is a single, shared library of managed component data said to simplify setup, configuration, use and maintenance of libraries. Offers templated component data authoring – a single, consistent way to define and create component data. Built-in connectivity to Octopart.

Altium
altium.com/concord

3-LIGHT SOURCE LDI

Ledia 6H offers flexible control enabled by three wavelength light sources for broader coverage of the wavelength regions for exposure, significantly expanding the number of supported resist types. Format reportedly improves productivity up to 100% compared to two wavelength models. Proprietary alignment algorithm compensates for substrate distortion.

Screen
screen.co.jp

OTHERS OF NOTE

HIGH-TEMP SOLDER MASK

Imagecure solder mask is for high-temperature automotive applications. Now withstands thermal cycling test criteria at -40°/+180°C for 1,000 cycles and -40°/+170°C for 2,000 cycles.

Sun Chemical
sunchemical.com

TEST MANAGEMENT SOFTWARE

PathWave Test 2020 streamlines test data processing and analysis. Provides data sharing and management between platform software tools, including test automation, advanced measurement, signal creation and generation, as well as data analytics. Application-tailored solutions can be developed and deployed to accelerate electronic test workflows and NPI. PathWave Desktop Edition is for launching and managing applications in design and test ecosystem. Can manage instrument discovery and installed design and test software and share data with a common user experience across all design and test software.

Keysight Technologies
keysight.com

AUTOMOTIVE-QUALIFIED MLVS

VLAS series low-clamp TransGuard multilayer varistors are designed to exhibit lower breakdown and clamping voltage to working voltage ratios. Comprised of zinc-oxide-based ceramic semiconductor devices with nonlinear, bidirectional voltage current characteristics similar to those of back-to-back zener diodes, but with greater current and energy handling capabilities and addition of EMI/RFI attenuation. Qualified to AEC-Q200.

AVX
avx.com

LOW-CROSSTALK CONNECTORS

Strada Whisper R backplane connectors reportedly ensure low crosstalk noise and enable migration path from 56G PAM-4 to 112G PAM-4. Use same mating interface and are backward-compatible with existing Strada Whisper connectors. Come in four-pair configurations and 92Ω impedance for traditional backplane applications. Support 85Ω and 100Ω impedance system requirements.

TE Connectivity
te.com

ALUMINUM ELECTROLYTIC CAPACITORS

GY SMT series conductive polymer-aluminum-electrolytic capacitors come with a rated voltage of 2.0VDC or 2.5VDC and capacitance values of 680µF to 820µF. Low ESR characteristics (3mΩ max.). Withstand +105°C for up to 2,000 hr. RoHS-compliant and halogen-free.

Panasonic Industry Europe
industry.panasonic.eu

POWER CONNECTORS

Multi-Beam Plus connectors provide current per power contact of a max. 140A/contact or 100 A/contact per four adjacent contacts. Scalable and modular design supports greater flexibility in configuration and PCB design. Separated power contacts improve dimension stability.

TE
te.com

AI-DRIVEN 3-D AOI

Alpha comes with hybrid 3-D inspection technology for uniform precision measurement across 3-D measurable range, regardless of PCB density and material characteristics. Reportedly yields superior edge definition and requires less software filtering of raw inspection data. Automatic programming software uses AI-based deep learning methodology to minimize human error.

MIRTEC
mirtec.com

CIRCUIT WEATHERPROOFING

PRO750 GEN4 coating chamber uniformly deposits Parylene coatings. Proprietary controller remotely monitors and controls critical factors, including temperature, pressure and other essential operating parameters in real-time. For batch or high-volume.

HZO
hzo.com

HIGH-SPEED PARTS COUNTER

XQuik III has 10 sec. per reel count time. Requires no models, libraries or connection to the cloud. Automatic algorithms recognize components. Unique imaging technology provides count accuracy. Flexible MES interface easily configured to communicate with any inventory control system.

VJ Electronix
vjelectronix.com

OTHERS OF NOTE

CRITICAL CLEANING SWABS

7020/7022, 7250 and 7060 dry swabs have easy-to-grip handles for hard-to-reach areas. Are ISO Class 4-7 compatible and are comprised of various materials, including polyester knit and microfiber foam. Provide particle entrapment for sensitive applications such as medical device manufacturing.

ACL Staticide
aclstaticide.com

LARGE-BOARD 3-D AXI

TR7600TL SIII has CT capabilities. Designed for inspection of extra-large board sizes up to 1200mm x 660mm. Reportedly ensures quality inspection, lowering escapes and false calls.

Test Research
tri.com.tw

PARYLENE CONFORMAL COATING

SC7130-CC is thinner and sprayable. Withstands extreme testing. Coating thickness is 10-30µm, yet is said to meet performance of 75µm-thick standard acrylic conformal coating in extreme moisture and salt-laden environments. Removable with stripper solvent.

AIT
aitechnology.com

HIGH-SPEED FIXTURE MAKER

Toolmaker is a laser-driven, mini CNC machine for developing fixtures. A laser scans an assembled PCB and makes a mirror image in a foam "blank." Handles panels up to 300mm x 300mm. Resulting fixture supports the board, squeegee and provides a precise planar surface for boards and parts. No CAD data needed; programming is as simple as pressing "Go." A fully formed fixture takes about 2 hr.

Inspire Solutions
inspire-ondemand.com

BGA REWORK WITH VISION

ZM-R7220A is said to offer stable and uniform hot air heating. Lower heater adjustable. Carbon fiber IR preheater and precision PID temperature controls. High-definition 1.3Mp CCD camera and optical alignment. Optional side camera.

Seamark ZM
seamarkzm.com

REFLOW FLUX MANAGEMENT

Aqua Scrub flux management technology comes on Pyramax 125A convection reflow ovens. Is compatible with most known paste and flux types. Flux and solution are automatically contained and packaged for disposal. Mounts to back of oven.

BTU
btu.com

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In Case You Missed It

This column provides abstracts from recent industry conferences and company white papers. Our goal is to provide an added opportunity for readers to keep abreast of technology and business trends.

High-Density Connectors

"Qualification of High-Density Connector Solutions for Military and Avionic Environments"

Authors: Kim Cho, Tim Pearson, David Hillman and Ross Wilcox; kimera.cho@collins.com.

Abstract: This paper discusses the qualification of high-density connector solutions for rugged military and avionics environments. As electronic products have become progressively smaller in size, there has been a corresponding increase in the demand for miniature, electronic components and the development of high-density connectors. The consumer electronics industry has already implemented high-density connectors, while many avionics/military products still use traditional surface-mount and plated through-hole connectors. These traditional connectors are increasingly too large and cannot meet the signal capacity requirements of modern avionics/military product designs within the limited available printed circuit board space. In this study, two major types of high-density connectors, the fine-pitch leaded style and the area-array style, were installed on test boards using automated assembly with tin-lead and lead-free soldering processes. The assemblies were subjected to -55° to +125°C thermal cycle testing in accordance with IPC-9701, *Performance Tests Methods and Qualification Requirements for Surface Mount Solder Attachments*. The first part of this paper discusses results and observations from the new testing of fine-pitch style and area-array style connectors. The second part of this paper compares data for the fine-pitch connectors to previously tested area-array connectors. Tradeoffs between these two types of connectors, including producibility, reliability, printed circuit board space usage, rework, ease of assembly, and defect identification, are discussed. (Collins company white paper, October 2019)

Stretchable Electronics

"Three-Dimensional Curvy Electronics Created Using Conformal Additive Stamp Printing"

Authors: Kyoseung Sim, Cunjiang Yu, Ph.D., *et al*.

Abstract: Electronic devices are typically manufactured in planar layouts, but many emerging applications, from optoelectronics to wearables, require three-dimensional curvy structures. However, the fabrication of such structures has proved challenging due, in particular, to the lack of an effective manufacturing technology. Here, the authors show that conformal additive stamp (CAS) printing technology can be used to reliably manufacture 3-D curvy electronics. CAS printing employs a pneumatically inflated elastomeric balloon as a conformal stamping medium to pick up prefabricated electronic devices and print them onto curvy surfaces. To illustrate the capabilities of the approach, the authors use it to create various devices with curvy shapes: silicon pellets, photodetector arrays, electrically small antennas, hemispherical solar cells and smart contact lenses. The authors also show that CAS printing can be used to print onto arbitrary 3-D surfaces. (*Nature Electronics*, vol. 2, 2019. https://doi.org/10.1038/s41928-019-0304-4)

"Multifunctional Two-Dimensional $PtSe_2$-Layer Kirigami Conductors with 2000% Stretchability and Metallic-to-Semiconducting Tunability"

Authors: Emmanuel Okogbue, Sang Sub Han, *et al*.

Abstract: Two-dimensional transition-metal dichalcogenide (2-D TMD) layers are highly attractive for emerging stretchable and foldable electronics owing to their extremely small thickness coupled with extraordinary electrical and optical properties. Although intrinsically large strain limits are projected in them (i.e., several times greater than silicon), integrating 2-D TMDs in their pristine forms does not realize superior mechanical tolerance greatly demanded in high-end stretchable and foldable devices of unconventional form factors. The authors report a versatile and rational strategy to convert 2-D TMDs of limited mechanical tolerance to tailored 3-D structures with extremely large mechanical stretchability accompanying well-preserved electrical integrity and modulated transport properties. They employed a concept of strain engineering inspired by an ancient paper-cutting art, known as kirigami patterning, and developed 2-D TMD-based kirigami electrical conductors. Specifically, the authors directly integrated 2-D platinum diselenide (2-D $PtSe_2$) layers of controlled carrier transport characteristics on mechanically flexible polyimide (PI) substrates by taking advantage of their low synthesis temperature. The metallic 2-D $PtSe_2$/PI kirigami patterns of optimized dimensions exhibit an extremely large stretchability of ~2000% without compromising their intrinsic electrical conductance. They also present strain-tunable and reversible photo-responsiveness when interfaced with semiconducting carbon nanotubes (CNTs), benefiting from the formation of 2-D $PtSe_2$/CNT Schottky junctions. Moreover, kirigami field-effect transistors (FETs) employing semiconducting 2-D $PtSe_2$ layers exhibit tunable gate responses, coupled with mechanical stretching upon electrolyte gating. The exclusive role of the kirigami pattern parameters in the resulting mechanoelectrical responses was also verified by a finite-element modeling (FEM) simulation. These multifunctional 2-D materials in unconventional yet tailored 3-D forms are believed to offer vast opportunities for emerging electronics and optoelectronics. (*Nano Letters*, Jun. 6, 2019; www.ncbi.nlm.nih.gov/pubmed/31244238)

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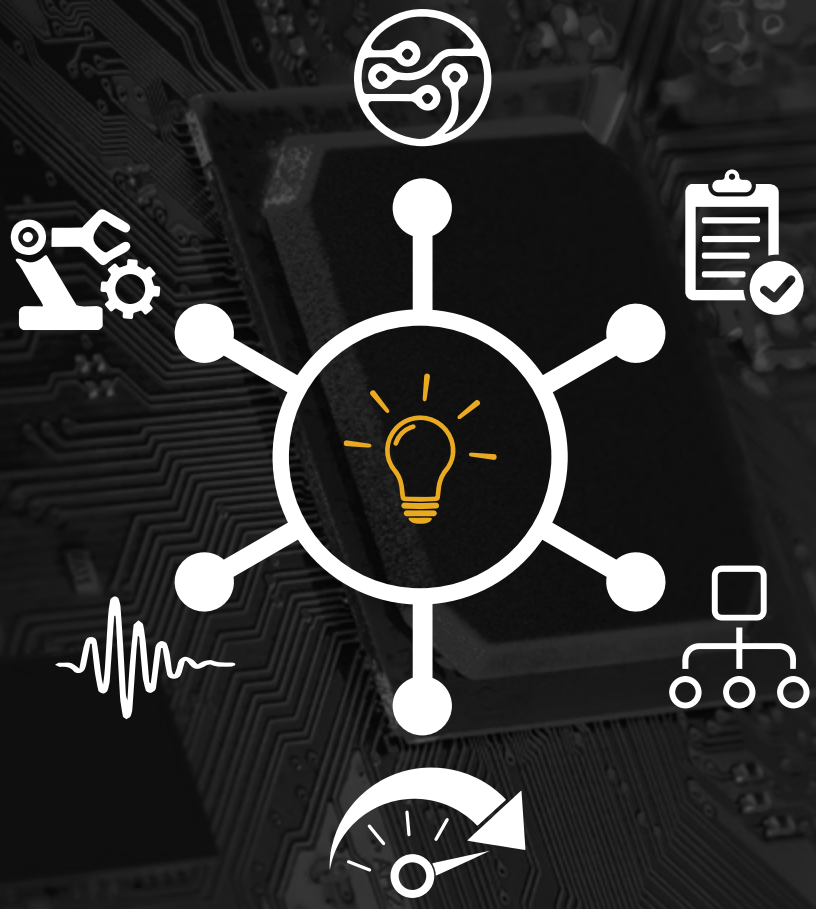

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