Predicting Demand Spikes, p. 41

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March 2021

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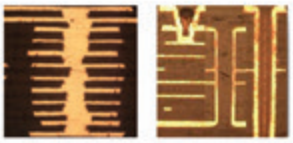
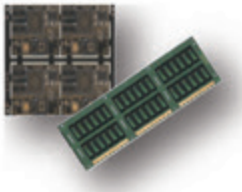
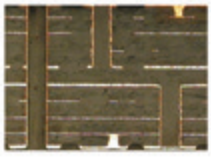
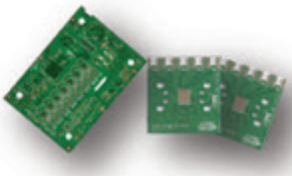


IOT / Build-up Board





Semiconductor TEST B'd
& 5G Network System



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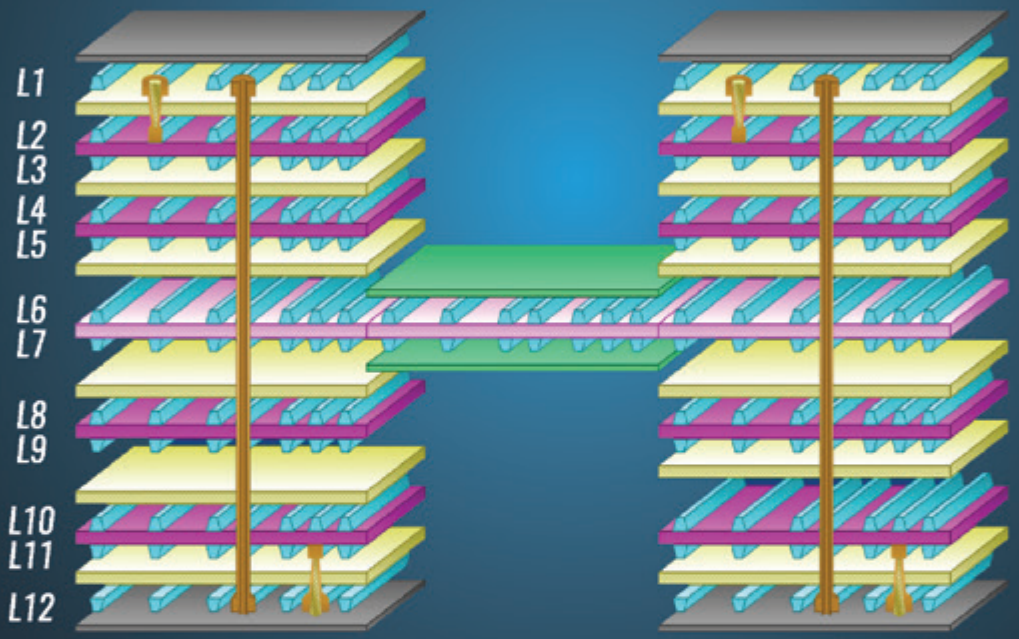

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MIKE BUETOW
EDITOR-IN-CHIEF

An Electronics Holiday?

WHAT DO YOU do when the very thing for which you've been asking, nay, begging for years actually materializes?

That would be US government support for the printed circuit board industry. And it's coming in the form of real dollars, not just platitudes.

As we report in our digital edition this month, the US Partnership for Assured Electronics (USPAE), a subsidiary IPC formed last year to give it room to lobby on behalf of US members without running afoul of its international cohort, has as of late January garnered more than $42 million in taxpayer dollars to manage joint industry-academia programs to tackle electronics-related challenges.

How we've waited for this.

Going back to the 1990s, when I worked at IPC, we spent thousands of hours (and countless more dollars) vainly waving our hands in front of Congress's collective face. And once a year, we would gather in Washington and run from office to office on Capitol Hill telling anyone and everyone how important the industry is. After, we would retreat to our hotel bars and pat each other on the back for a job well done. After many years of this, Congress even passed a resolution. "The PCB industry is important!" they said. "Hallelujah!" we rejoiced. Our souls were saved. Or so we thought. Then the OEMs packed up and moved their orders to Taiwan and China. Poof.

It's no secret semiconductors and software get the lion's share of attention, be it from investors or politicians. Even so, PCBs aren't alone in the fight: The Semiconductor Industry Association in February joined NAM, SEMI, the US Chamber of Commerce and several other tech, medical, auto and business groups in urging President Biden and Congress to fully fund the domestic semiconductor manufacturing and research provisions established in the recently enacted National Defense Authorization Act. The groups also called on Washington to enact an investment tax credit to build and modernize semiconductor manufacturing facilities in the US.

Pounding away at the drums, the semiconductor industry is sending a loud and clear message that the financial pressure of remaining the top dog is overwhelming the market. This squeeze is being felt by none other than Intel, which, as Phil Marcoux notes in senior editor Chelsey Drysdale's industry outlook, starting on pg. 36, "Only a couple of companies can generate enough money to pay for both the product development and the process development/implementation of mass-volume semiconductor manufacturing.… Our worry is the US will lack the necessary manufacturing knowledge and acumen to maintain industry leadership." Sound familiar?

It's nice to have company, I suppose, even if you're stuck in a tar pit.

But we might be levering ourselves out. About four years ago, we offered seven steps the domestic industry should take to regain its international footing. One of them was to educate lawmakers as to what a PCB is and its importance to US defense. "This," we wrote, "means handpicking articulate industry spokespersons, rather than turning scores of well-meaning but uninformed company execs loose in D.C. for the day. I've been to enough industry lobbying days to know the intentions are good, but the execution is wanting. Too many (read: all) legislators look at boards as just another component, and not a particularly critical one at that. It's time to send in the pros."

IPC, it seems, heard the message loud and clear, and to its credit, they made it happen. They tapped an experienced hand in Pentagon acquisitions practices and advanced manufacturing supply chains to run the show. And although USPAE executive director Chris Peters doesn't come from electronics, he is well-tuned to the issues of small- to medium-sized businesses (SMBs), which make up the lion's share of the 150-odd domestic printed circuit board suppliers to the DoD.

There is reason to celebrate, but it's not yet time to declare a holiday. The heavy lifting – meaningful results – is just beginning.

mbuetow@upmediagroup.com
@mikebuetow

P.S. Be sure to register for PCB East (pcbeast.com), coming in June to the Boston area. And check out the upcoming webinars on screen printing, PCB procurement, x-ray inspection at PCB2Day.com.

PCDF People

3D Systems named **Mike Fitts** regional sales manager.

Frontline PCB Solutions named **Lior Furman** product manager – business development.

Ohmega Technologies named **Lisa Wilhelm** director of sales. She joins from TTM Technologies, where she held positions in sales, engineering and program management.

Orbotech named **Avi Greenberg** general manager Americas and vice president sales.

Pioneer Circuits named **Kevin Schuld** staff quality engineer.

PCDF Briefs

A furnace explosion at **AGC's** glass substrate manufacturing plant in Gumi, South Korea, injured nine workers and disrupted the TFT-LCD glass substrate supply chain.

AMD expects the number of notebook designs powered by its new generation of Ryzen mobile processors to grow 50% compared to its previous chips.

Coherent has received multiple unsolicited cash-and-stock buyout bids, including one from **MKS Instruments** that values the laser maker at about $5.78 billion.

Compeq and **Tripod Technology** have seen strong HDI PCB shipment pull-ins from clients for handset, notebook and automotive applications.

DuPont Interconnect Solutions said its $220 million expansion project in Circleville, OH, is expected to be completed in the second half of 2021.

Fauna is using **AT&S** technology for its audio glasses.

Kinetic Vision improved PCB workflow 500% with **Altium** 365.

Nano Dimension has engaged **CarlSquare** to advise on acquisitions in Europe.

PNE PCB is proposing a private placement to raise RM21.1 million (US$5.2 million) to reduce its borrowings and upgrade its existing PCB production.

Rigol Technologies named **TestEquity** distributor in the US.

SnapEDA and Switchcraft are collaborating to distribute digital models for Switchcraft's electromechanical components.

Taiwan-based IC substrate makers are looking to expand capacity for high-end BT-based substrates in 2021 because of demand for SiP (system-in-package) and AiP (antenna-in-package) designs.

Trackwise ordered two **Adix** reel-to-reel direct imagers.

New Dates Announced for PCB East

PCB EAST 2021 Conference & Exhibition

ATLANTA, GA – UP Media Group announced new dates for PCB East when it returns to the Boston area this year. The three-day technical conference now takes place Jun. 15-17 in Marlborough, MA. The event includes a one-day exhibition on Jun. 16.

"As the Covid-19 vaccine rollout continues, we felt the best course of action was to adjust our dates accordingly, so the largest number of PCB industry professionals would be able to attend," said Mike Buetow, conference director. "At this time, Massachusetts is scheduled to begin vaccinating the general population in April, and the adjacent states are planning similar schedules. Mid-June looks to be a safe time to at long last return to face-to-face interaction."

Registration for the event is now open. Visit pcbeast.com for details. (MB)

IPC Releases Standards for BTC Design, Digital Twins

BANNOCKBURN, IL – IPC in February announced the release of a revision to its standard for design and assembly for implementing BTCs. IPC-7093A, *Design and Assembly Process Implementation for Bottom Termination Components (BTCs)* is a complete overhaul and focuses on critical design, materials, assembly, inspection, repair, quality, and reliability issues, the trade group said.

IPC-7093A includes a step-by-step process on how to design and incorporate BTCs into any card layout. Comprehensive descriptions on how to implement robust designs and assembly processes and troubleshooting guidance for common anomalies that can occur during BTC assembly are included.

Revision A adds guidance on elements for thermal pad design, thermal via usage, stencil design, assembly recommendations, reliability considerations, known issues/defects to avoid.

Separately, IPC released IPC-2551, *International Standard for Digital Twins*. The standard is comprised of digital twin product, manufacturing, and lifecycle frameworks. It is said to allow a manufacturer, design organization or solution provider to initiate application interoperability to create smart value chains.

IPC-2551 provides a comprehensive self-assessment mechanism for companies to determine their current digital twin readiness level and map the steps to achieve a full digital twin approach. It is designed for companies in the planning stages for applying a digital twin framework to their operations.

The standard enables interoperability of all forms of processing of digital data that precisely match and represent physical capabilities. The standard does this by defining and precisely laying out a digital twin cell-based architecture. This enables any manufacturer to create and use the IPC digital twin standard to represent every process and possible actions taken on a product within the manufacturing and lifecycle environment, for engineering, modeling, planning, quality and reliability analysis and simulations. (MB/CD)

Ticer Acquires Deposition Manufacturing Assets of Global Firm

CHANDLER, AZ – Ticer Technologies has completed the acquisition of manufacturing assets from another global manufacturing corporation for an undisclosed sum. Ticer is now operating the vacuum deposition/sputtering production equipment.

All processes, equipment and raw materials will continue to be the same during the ownership transition, and Ticer's thin-film resistor copper foil products will remain unchanged.

"As we begin 2021, Ticer Technologies is pleased to be in a stronger position

Re-Engineering the EMS Partnership

At EDM, we do things differently by design. We start by listening to what our customers wish they had in a contract manufacturing relationship and then structure a solution that incorporates that. Variable demand? Our supply chain and production teams design a stocking program with finished goods Kanban that keeps deliveries on time even with changing forecasts. Is labor cost an issue? Our engineering team specializes in custom production automation that minimizes touch labor so well that we've brought projects back from China. Concerned about quality? So is every one of our employee owners on the production floor. Need a better product to beat the competition? Our engineering team has a track record of helping customers enhance their products over multiple generations.

In short, we've been the secret sauce for customers in industrial/instrumentation, transportation/public safety, specialty consumer, medical and telecom industries for more than three decades. If you are looking for a U.S. EMS provider capable of supporting your complete product lifecycle from design through post-manufacturing support or a subset of those services, give us a call at (434) 385-0046 ext. 8163 or visit us at www.edmva.com.

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Trilogy-Net and **Y.I.C. Technologies** signed a North American distribution agreement.

TTM Technologies earned the IPC-1791, *Trusted Electronic Designer, Fabricator and Assembler Requirements Qualified Manufacturers Listing (QML)* at its plant in Sterling, VA.

Unimicron Technology's PCB and IC substrate manufacturing site in Taoyuan, Taiwan, sustained its second fire in four months on Feb. 4.

CA People

Altus Group promoted **Joe Booth** to chief executive.

Anwarson Advanced Research Projects Laboratory named **Hassan Shahzad** chief technology officer.

ASM Pacific Technology named **Waldemar Christen** vice president CRM, SMT Solutions.

Datalink Electronics named **Shane Nooney** SMT engineer.

Ducommun appointed **Christopher D. Wampler** CFO, controller and treasurer.

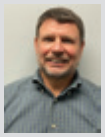
ECD co-owner **Tara Fischer** is now exclusive owner and president. She has been with the company 26 years.

Europlacer named **François Erceau** group strategic direction and marketing officer.

4Front Solutions named **Anthony Jepson** chief operating officer.

Fuji America named **Jason Speelman** Eastern regional sales manager.

Gen3 promoted **Andrew Naisbitt** to CEO.



Libra Industries named **Jim Kircher** president and chief executive, succeeding **Rod Howell,** who cofounded the company in 1980. Prior to joining Libra in October 2020, Kircher was chief commercial officer of Faulhaber.

Kimball Electronics appointed **Jana Croom** vice president, finance.

Memsense named **Tino Gonzales** manufacturing manager.

Milwaukee Electronics promoted **Jered Stoehr** to chief executive after 19 years with the EMS company, most recently as vice president of marketing and sales. He succeeds his father **P. Michael Stoehr,** who will serve as executive chairman.

Murray Percival named **Rayne Lythjohan** business development manager for South Ohio, South Indiana and Kentucky. He most recently worked as a

technically, have greater flexibility and expanded capacity for volume business growth. We are looking forward to offering our expanded benefits to our global customer base," said David Burgess, president, Ticer. (CD)

National Circuit Assembly Merges with Austin Circuit Design

GARLAND, TX – National Circuit Assembly announced on Feb. 16 a merger with Austin Circuit Design, adding design and sourcing to its electronics manufacturing services. Financial and other terms were not disclosed.

NCA was founded by Mike Tieu in 2006. It operates a 30,000 sq. ft. factory northeast of Dallas.

ACD was founded as Circuit Design Consultants by Greg Ochoa in 1985. It incorporated and became Austin Circuit Design in 2002. The firm was sold to its current ownership in 2015.

"As a longtime partner of ACD, we understand the processes and ways that the design firm operates, and we know it fits in with NCA's operations well," NCA said in a press release. "Now NCA and its partners can enjoy a more streamlined process, from walking in the door to having a finished product running out the door. We aim to reach a broader audience with the addition of ACD and their capabilities to the NCA team."

ACD COO and co-owner Minh Nguyen becomes NCA vice president of sales and sourcing. "NCA and ACD have worked hand-in-hand closely for several years already, and we're looking forward to a smooth transition into working with our partners together," he said. (MB)

AEM Holdings Proposes Acquisition of CEI for $75M

SINGAPORE – Electronics manufacturing company AEM Holdings has launched a S$99.7 million (US$75.2 million) bid for contract manufacturer CEI. AEM plans to delist CEI from the Singapore Exchange and take it private.

AEM is offering S$1.15 in cash, or a mix of cash and new AEM shares, for each ordinary share in mainboard-listed CEI.

CEI shareholders can opt to accept the offer for either 85% cash and 15% new shares or 70% cash and 30% new shares at an issue price of S$3.55 for each new share in AEM.

Founded in 1999, CEI has annual revenues of about $100 million primarily from customers in the industrial equipment market. It operates sites in Singapore, Indonesia and Vietnam. (CD)

Motorola Opening Video Security Manufacturing Plant in TX

RICHARDSON, TX – Motorola Solutions is opening a 136,000 sq. ft. Video Security and Analytics manufacturing facility here. The new site consolidates smaller manufacturing facilities from Allen, Plano and Carrollton, TX, and will serve as the manufacturing hub for at least six companies.

The new facility is expected to ship nearly 400,000 cameras and produce one million PCBAs in 2021. It will employ some 250 staff, with expected growth to 300.

"We have quite a large employee base in Texas, approximately 1,000 employees, with a majority of them in the Dallas area," said John Kedzierski, senior vice president and general manager of Video Security & Analytics, Motorola Solutions. "We wanted to consolidate into one world-class facility that had the size and scale for us to continue our growth. We chose to stay local because it would be convenient for our current employ-

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Naprotek named **Daniel Everitt** president and CEO.

PVA named **Dale Hall** business development manager, 2K Meter Mix, and **Marco Reyes** business development manager, Industrial Products. Hall has 30 years' experience in the chemical manufacturing and robotic industry, while Reyes spent the past 15 years in business development and sales with Graco, Dymax and Simco-Ion.

Sanmina promoted **Richard Henrick** to regulatory compliance manager.

CA Briefs

ACDi purchased a **Juki** FX-3L SMT line and a **Nordson Dage** Assure x-ray component counter.

Amazon is setting up its first device manufacturing line in India to make Fire TV sticks and is partnering with **Cloud Network Technologies,** a subsidiary of **Foxconn.**

BEST Inc. installed an **ERSA** IR/PL 550 BGA rework system.

Circuit Technology Center purchased an **SCS** Ionograph BTSP series ionic cleanliness tester.

Cogent Technology increased the size of its Suffolk, England, EMS plant by more than 60,000 sq. ft., to 80,000 sq. ft. overall.

Cogiscan announced a strategic long-term partnership with **Vayo Technology.**

Continental plans to open a $170 million auto electronics factory in northern Serbia.

Dymax added **Electronic Assembly Products** as channel partner in North America.

Eriez completed a 38,000 sq. ft. expansion to its manufacturing plant in Erie, PA, including a new electronics lab, and a software and circuit board development area.

ExcelTech purchased a **Nordson YesTech** FX-940 3D Ultra AOI.

Foxconn and **Geely** announced a joint venture to supply electric car manufacturing to third parties. Foxconn's India business unit is gearing up for an IPO worth Rs 5,000 crore ($683 million), per public reports. Vietnam awarded a license to Foxconn to build a $270 million plant to produce laptops and tablets, according to Reuters.

Hyundai has issued a recall notice for more than 93,500 Tuscon mid-sized SUVs due to a faulty circuit board in the ABS module that has the potential to start an engine-bay fire even when the car is turned off.

ees, the facility worked out very well for us and we had good access to the airport.

"We're proud to be building upon our commitment to provide advanced video security offerings that help our customers make better informed decisions. With this new state-of-the-art facility, we will be manufacturing critical, NDAA-compliant safety and security video solutions on the doorstep of American public safety agencies and businesses." (CD)

Intervala has signed a long-term lease finalizing the relocation of its corporate headquarters and EMS manufacturing operation in Westmoreland County, PA.

ITW has entered into an agreement to acquire **MTS Systems'** Test & Simulation business following the closing of **Amphenol's** acquisition of MTS.

Jabil acquired **Ecologic Brands,** a sustainable packaging provider specializing in the paper bottle and paper-based packaging solutions. It also will invest more than HUF 1 billion ($3 million) at its automotive electronics plant in Tiszaújváros, Hungary, according to reports.

Kulicke & Soffa acquired a 100% equity stake in **Uniqarta,** including Uniqarta's patent portfolio and other intellectual property rights.

Kyzen named **Kurt Whitlock Associates** to sell its cleaning products in Florida.

The US has launched a patent infringement investigation against **Luxshare Precision Industry** over possible import violations.

Mesago Messe is cancelling SMTconnect due to the continuing high rate of infections and the associated restrictions.

Northrop Grumman awarded **Kitron** a NOK 10 million ($1.15 million) order for production of a sub-assembly for the F-35 fighter aircraft radar.

Note signed a deal worth SEK 85 million annually to build electronics in Estonia for an international medtech company.

NovaCentrix appointed as manufacturers' representatives **MaRC Technologies** in the Pacific Northwest US, and **PIT Equipment Services** in Southeastern New York, New Jersey and Eastern Pennsylvania.

Patriot American Solutions purchased an **Austin American Technology** X30 stencil cleaner.

PDR named **Circuit Technology** manufacturer's representative in North and South Carolina.

Pegatron has gained land use rights for a 423,195 sq. ft. industrial site in Mahindra City, India, outside Chennai.

Plasmatreat founded the subsidiary **Plasmatreat Schweiz** to better serve the Swiss market.

Promation has moved into a larger facility with more office space and a tech demo center in Kenosha, WI.

Radisys selected **Keysight's** user equipment emulation (UEE) solution platform, radio unit simulator, Open RAN Studio software and PROPSIM channel emulators.

S and Y Industries installed multiple **Europlacer** placement machines.

Sanmina purchased **Osram's** digital lighting components production plant in Bulgaria.

SMTC will expand its EMS campus in Chihuahua and close its operations in Fresnillo, Mexico.

Thermaltronics named **PCBASupplies.com** an authorized distributor for its hand soldering products throughout the US.

Trotter Controls purchased an **Austin American Technology** AquaTherm 9100 PCB cleaner.

Vexos selected **MIRTEC** as its 3-D AOI "Partner of Choice."

Vinatronic installed a **Glenbrook** JewelBox 70T x-ray inspection system.

ViTrox named **MTSC** distributor in Thailand. It also installed its 100th V810i 3-D AXI in the US.

VTech Holdings has signed an agreement to acquire **QSC's** production facility in Mexico to manufacture wood enclosure loudspeakers.

XDry has relocated its corporate headquarters to Dallas.

Xiaomi said it has filed a lawsuit against the US Defense and Treasury departments, seeking reversal of a decision to block US investments.

Yamaha Motor Robotics SMT Section has opened the Yamaha SMT Virtual Reality Showroom showing the latest technology for electronics assembly, inspection, and component handling.

Z-Axis added a second low-pressure injection molding machine for wire and cable assembly production.

Zero Defects International received notice of compliance with and renewed registration for ITAR.

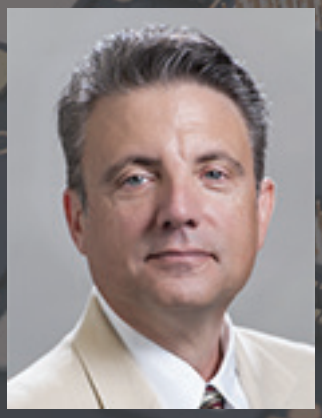
Zestron and **GEN3 Systems** are collaborating on a new test service in the US to help develop objective evidence required by the latest release of IPC-J-STD-001H.

WEBINAR

PCB2DAY

May 19, 2021
1:00 pm – 4:00 pm EST

How to Save Up to 25% on Your PCB Purchases



Greg Papandrew

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Trends in the US electronics equipment market (shipments only)	% CHANGE OCT.	NOV.	DEC.	YTD%
Computers and electronics products	2.3	-1.5	0.6	4.5
Computers	1.7	-0.5	-3.4	-6.6
Storage devices	17.7	-1.8	0.0	24.7
Other peripheral equipment	2.1	3.1	-6.2	9.3
Nondefense communications equipment	10.7	-7.4	3.4	13.6
Defense communications equipment	0.0	8.7	-11.3	7.3
A/V equipment	1.4	-3.8	-12.9	-2.2
Components[1]	1.5	0.7	-1.0	10.4
Nondefense search and navigation equipment	2.4	-1.2	-0.9	-5.0
Defense search and navigation equipment	0.7	-2.2	0.2	2.2
Medical, measurement and control	1.7	-0.5	1.0	0.3

[r]Revised. *Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: U.S. Department of Commerce Census Bureau, Feb. 4, 2021

US MANUFACTURING INDICES

	SEP.	OCT.	NOV.	DEC.	JAN.
PMI	55.4	59.3	57.5	60.5	58.7
New orders	60.2	67.9	65.1	67.5	61.1
Production	61.0	63.0	60.8	64.7	60.7
Inventories	47.1	51.9	51.2	51.0	50.8
Customer inventories	37.9	36.7	36.3	37.9	33.1
Backlogs	55.2	55.7	56.9	59.1	59.7

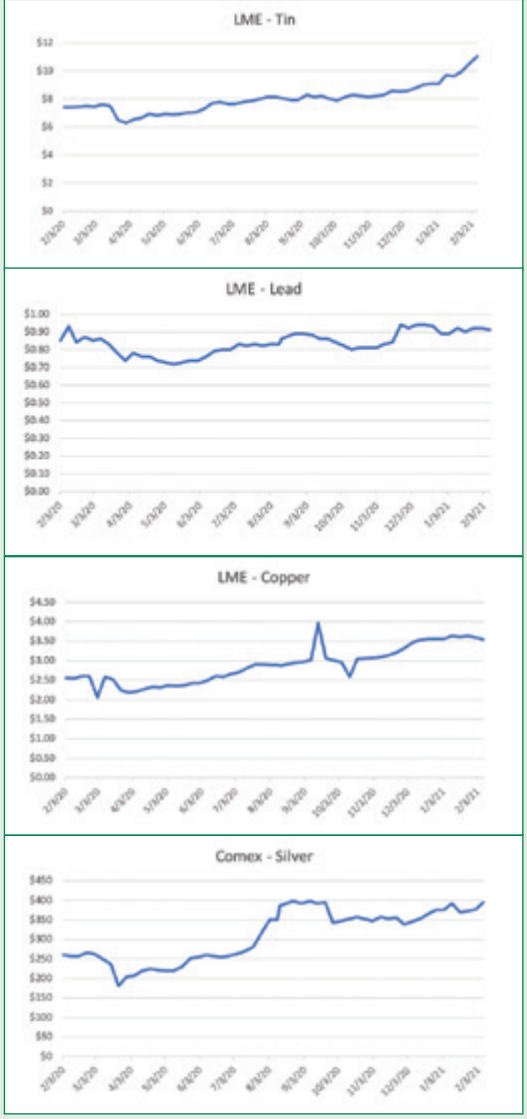
Source: Institute for Supply Management, Feb. 1, 2021

KEY COMPONENTS

	AUG.	SEP.	OCT.	NOV.	DEC.
Semiconductor equipment billings[1]	32.5%	40%	27.3%	23.1%[r]	7.6%[p]
Semiconductors[2]	4.94%	5.79%	5.86%	8.4%[r]	8.3%[p]
PCBs[3] (North America)	0.94	0.93	0.97	1.05	1.10
Computers/electronic products[4]	5.22	5.15	5.01	5.13[r]	5.13[p]

Sources: [1]SEMI, [2]SIA (3-month moving average growth), [3]IPC, [4]Census Bureau, [p]preliminary, [r]revised

METALS INDEX



Hot Takes

- **Consumer electronic revenues** rose 7% to $358.5 billion in 2020. (Strategy Analytics)
- **Electronic components** showed strong sequential growth in January, and stronger performance is expected in February. (ECIA)
- **The worldwide tablet market** had 19.5% year-over-year growth and shipments totaling 52.2 million units in the fourth quarter. (IDC)
- **The German area electronics industry** expects 5% growth in 2021, after production fell 7% in 2020. (ZVEI)
- **The worldwide smartphone market** grew 4.3% year-over-year in the fourth quarter. (IDC)
- **The flexible electronics in healthcare market** will exceed $8.3 billion by 2030. (IDTechEx)
- **FCBGA package revenue** is expected to reach $12 billion by 2025, driven by AI, data center and HPC momentum, a CAGR of 3% between 2020 and 2025. (Yole)
- **China's IC wafer capacity growth** accelerated 14% in 2019 and 21% in 2020 and is expected to grow at least 17% in 2021. (SEMI)
- **Fourth quarter PC shipments** grew 26% year-over-year to 91.6 million units. (IDC)
- **Notebook ODMs** are considering hiking prices to reflect rising costs of components, transportation and other expenses.
- **Taiwan's PCB industry output** grew 5.6% on year to a record high of NT$667.2 billion (US$23.83 billion) in 2020. (TPCA)
- **December EMS orders** were up 13.2% year-over-year and down 5.2% sequentially. (IPC)
- **Microprocessor sales** climbed 12% in 2020 to a record $87.7 billion, and are expected to grow another 9% in 2021.
- **The wearable electronics market** is poised to grow $41.2 billion from 2020-2024, a CAGR of 15%. (Technavio)

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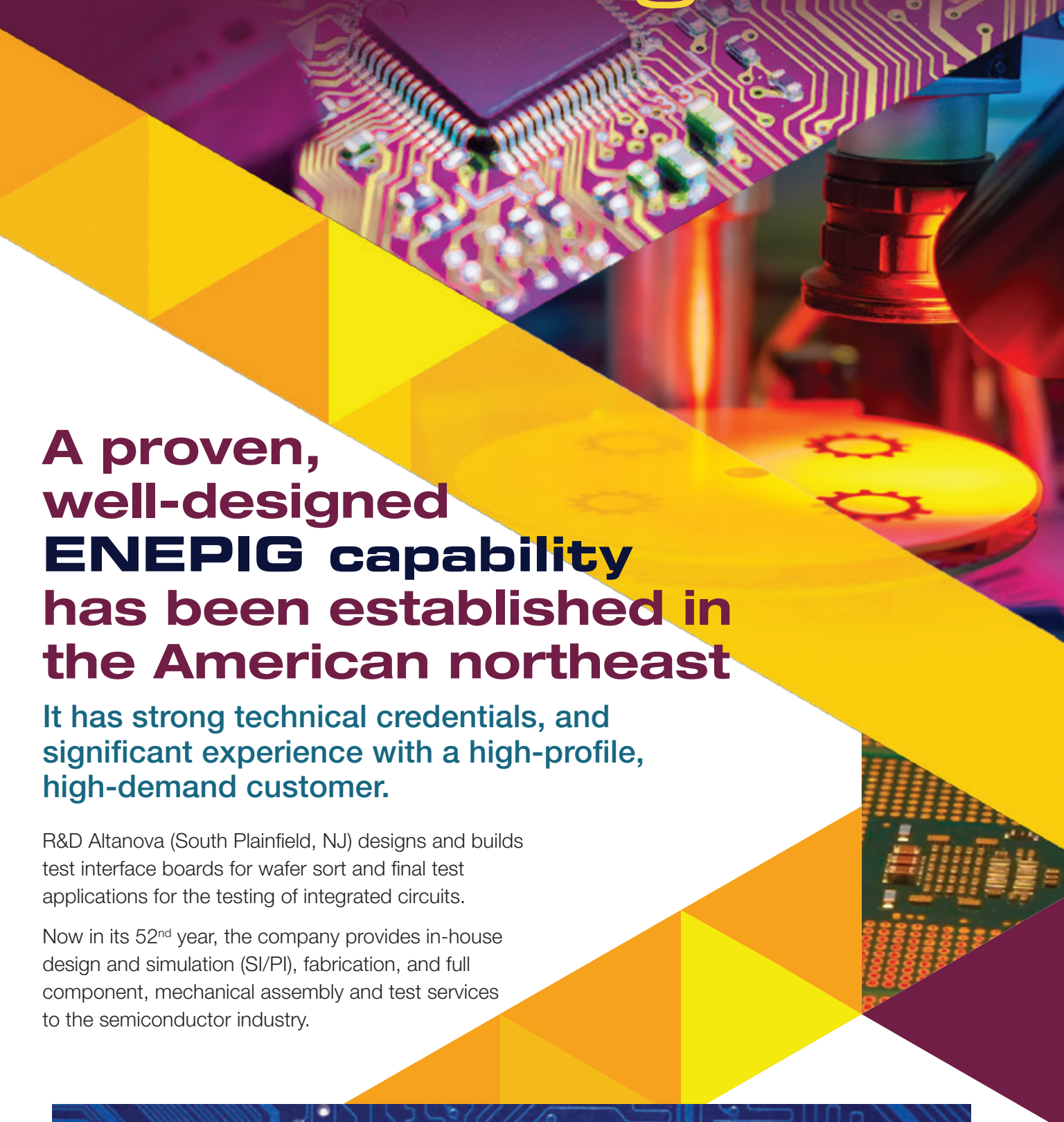


A proven, well-designed **ENEPIG capability** has been established in the American northeast

It has strong technical credentials, and significant experience with a high-profile, high-demand customer.

R&D Altanova (South Plainfield, NJ) designs and builds test interface boards for wafer sort and final test applications for the testing of integrated circuits.

Now in its 52nd year, the company provides in-house design and simulation (SI/PI), fabrication, and full component, mechanical assembly and test services to the semiconductor industry.

Fully automated ENIG/ENEPIG plating line uses Uyemura's newest reduction-assisted immersion gold process ("RAIG").

R&D Altanova is best known for solutions that include fine pitch load board fabrication down to 0.2mm, probe card fabrication with coplanarity specifications as low as 12 µm per inch, multilayer organic substrates with pitches as small as 45 micron, boards with aspect ratios of 50:1, and embedded component solutions for PCBs and daughter cards. The company is also recognized as best in class for designing and delivering printed circuit boards for high frequency applications.

In 2019, R&D Altanova became the first East Coast PCB facility to install Uyemura's Reduction Assisted Immersion Gold (RAIG) ENEPIG process, and offer contract plating services.

The RAIG ENEPIG process developed by Uyemura is formed by the deposition of electroless nickel, followed by electroless palladium, with an autocatalytic immersion gold layer. RAIG ENEPIG's performance is unrivaled in solderability, shelf life and solder joint reliability. It is an exceptional final finish for soldering, gold wire bonding, aluminum wire bonding, and low contact pad resistance.

SEM studies and elemental analysis shows that palladium at the joint interface dramatically reduces intermetallic propagation. This, along with its ability to produce a non-porous gold surface, has made ENEPIG the preferred final finish for packages requiring soldering and wire bonding with lead-free SAC type alloys.

ENEPIG has also proved an excellent solution for IC package PCB substrates. Unlike electrolytic processes, it carries no requirement for bussing lines, a factor which translates to maximum flexibility in circuit design, and compatibility with the highest board densities.

R&D Altanova operates under the leadership of CEO & President Seyed Paransun, a thought leader within the semiconductor and electronics industries with a strong vision about the company's role in the commercial arena, as well as the military sector, where ENEPIG has growing support.

"There is a lot of opportunity and demand for onshore turnkey services for design, fabrication and assembly using fine pitch substrates. This is particularly relevant due to the growing importance of being able to supply a full system in a package. R&D Altanova's ability to provide full turnkey and quick-turn substrates, along with ENEPIG "creates a strong value proposition for the marketplace."

Quoted in this article:

Don Gudeczauskas

Seyed Paransun

Rich DePoto

Yubing Wang

Vassilis Danginis

R&D Altanova serves a broad range of customers for ENEPIG. Its preeminent customer relationship is with Micron Technology. "Micron SIG (Systems Integration Group) designs and manufactures dedicated automated tester solutions," explains Paransun. "RD Altanova provides the PCBs that connect the automatic test equipment to the device under test."

Originally, the ENEPIG process was outsourced, which proved problematic. "There were quality issues, as well as longer cycle times," recalls Paransun. "ENEPIG is just one step of the process in a complex PCB manufacturing environment. As a turnkey house, we understand the exact requirements for pre-clean, ENEPIG, post-ENEPIG and inspection, so when the board is delivered to the customer, it's ready for deployment."

R&D Altanova has aggressively invested in new tools, materials, technology and capacity. In 2019, the company doubled annual spending to $5 million in Cap Ex, including the ENEPIG line. "Commensurate to our investment in technology, we hired highly skilled individuals to support our ramp-up in technology and capacity. R&D Altanova is now ready to support our customers in 5G, AI, radar, autonomous vehicles and the IoT space," says Paransun.

During the ENEPIG selection process, Micron also specified Uyemura as the chemical supplier. "Our team evaluated alternatives, but no other chemical supplier was qualified, in our view. There is great technical trust in the trifecta we built between Micron, R&D Altanova and Uyemura," Paransun said.

R&D Altanova is actively marketing its ENEPIG processing capabilities within its traditional markets, and in evolving ones as well. The strongest interest, according to Paransun, comes from current users of ENEPIG who expect world class quality and service, and users of hard gold.

"Usually," he says, "boards get thick gold and hard gold. With too much gold, you can't bond properly; not enough gold causes other issues. ENEPIG strikes a great compromise. I'm optimistic that momentum is building to make the ENEPIG process ubiquitous for a broad base of applications."

Rich DePoto, Business Development Manager for Uyemura, suggests that other factors favoring ENEPIG are wire bondability and extended solderability. "Contract assemblers particularly appreciate that ENEPIG's exceptional solderability allows it to handle the numerous steps including possible rework that are often involved."

The ENEPIG line at R&D Altanova was designed by a team that included Uyemura Vice President Don Gudeczauskas, Senior Applications Engineer Al Gruenwald, and Rich DePoto, as well as Director of Process Engineering Dr. Yubing Wang and his team at R&D Altanova. Wang explains, "this is a fully automated hoist line with 2 nickel baths, and 2 gold baths, so we can process 2 loads simultaneously. The process cycle is 45-60 minutes; capacity is 3000 boards per week. Like all of our factories, the line is engineered to support 3 shifts and is located in a dedicated on-site building.

"Also," he adds, "although the line has been fine-tuned to where we wanted it to be, we continually work on techniques to expand its process window and improve yield and throughput. For example," he explains, "we have developed proprietary tech-nologies that extend gold bath life beyond what is

High throughput hoist system provides full coverage of high aspect ratio holes, accommodates fine pitch geometry.

being achieved anywhere in the US– or Asia. That particular accomplishment was something we learned together with the Uyemura team."

Military customers who are historically reluctant to change are clearly moving in ENEPIG's direction – "and quickly," according to DePoto. "We talk with military OEM suppliers weekly on applications where they would like to use this technology. This process is a powerful business driver for expanding ENEPIG's universe.

"Everyone would love to run ENEPIG, and many are trying to figure out how they can take advantage of its capabilities," says DePoto. *(Note: Uyemura ENEPIG can be integrated into an existing surface finish line with limited tank additions. The alternative ENEPAG approach requires thin immersion followed by electroless gold, thereby requiring 2 active gold tanks.)* "Electroless palladium can be a tricky process to run and putting gold on palladium is trickier still. The process in small volumes can be expensive to run efficiently. I predict that industry will benefit from outsourced ENEPIG for quite a while.

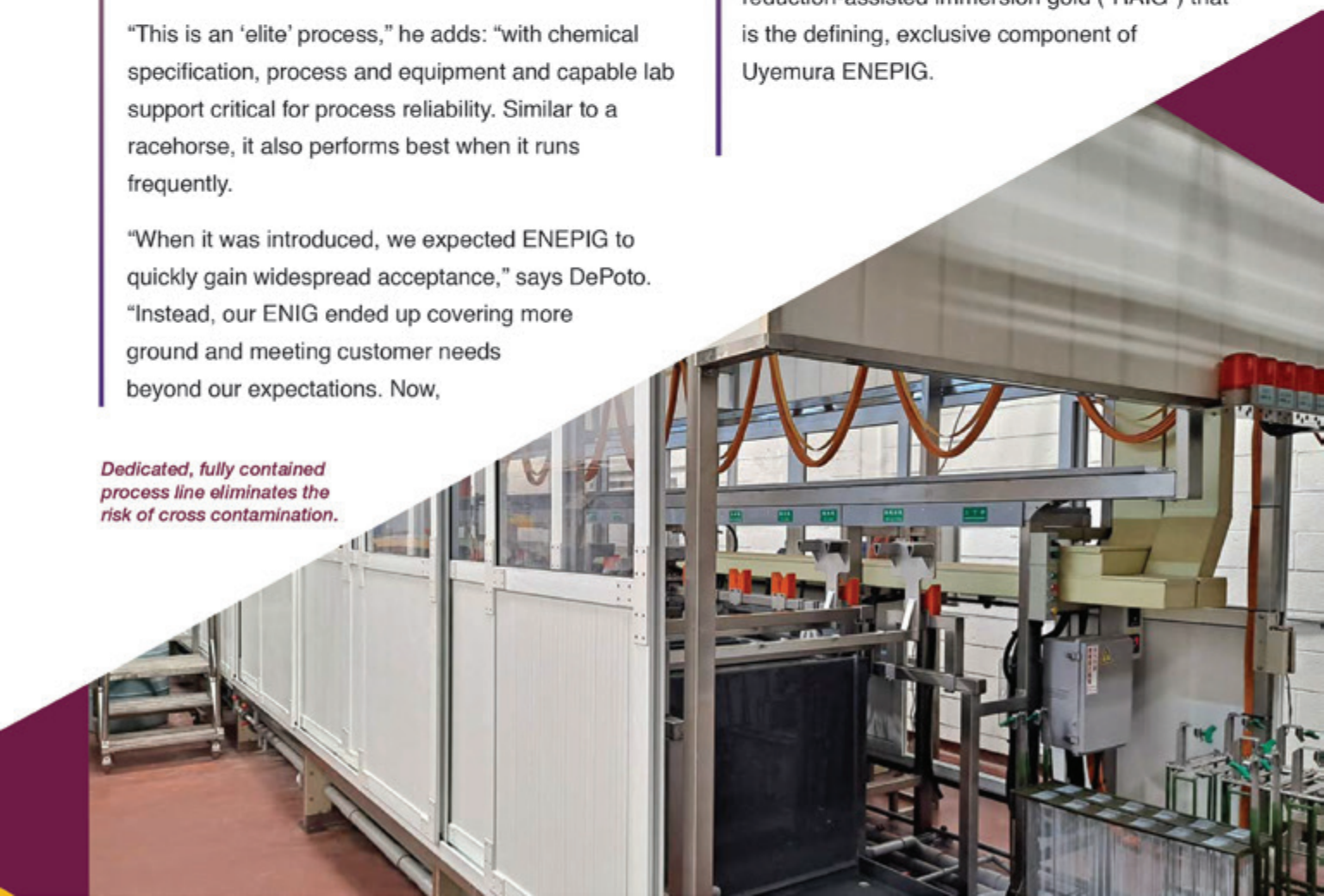
"This is an 'elite' process," he adds: "with chemical specification, process and equipment and capable lab support critical for process reliability. Similar to a racehorse, it also performs best when it runs frequently.

"When it was introduced, we expected ENEPIG to quickly gain widespread acceptance," says DePoto. "Instead, our ENIG ended up covering more ground and meeting customer needs beyond our expectations. Now, ENEPIG demand is increasing. Few shops are set up for the planning, testing and production level that ENEPIG requires. And bringing on that capability for lower volumes is often simply not practical."

At R&D Altanova, ENEPIG operates under a process engineering team headed by Yubing Wang. "We develop the process flow, test every variable to assure process robustness, then run pilots. When we're comfortable with the process and are sure it's solid, we move to low level manufacturing, document the process, and release it to manufacturing. The manufacturing team then runs it, while we continue researching ways to make it more robust, and compatible with ever-finer geometries."

According to Vassilis Danginis, VP of Quality, the company is ISO9001 certified and has been audited by numerous tier 1 consumer and military customers with exceptional outcomes.

Uyemura's ENEPIG technology is state-of-the-art, and no other company is running as high a level of ENEPIG as R&D Altanova. This is largely due to the reduction-assisted immersion gold ("RAIG") that is the defining, exclusive component of Uyemura ENEPIG.



Dedicated, fully contained process line eliminates the risk of cross contamination.

ENEPIG analytics, chemistry and auto dosing are managed by R&D Altanova's own lab.

TWX-40 RAIG was developed by Uyemura's Central Research Labs

for applications that require an immersion gold deposit thickness significantly greater than the minimum values required of ENIG / ENEPIG specifications.

RAIG allows the deposition of 4-6 µin gold directly on electroless nickel or electroless palladium. This hybrid or "mixed reaction" bath employs both immersion and autocatalytic (electroless) modes of gold deposition. The autocatalytic aspect means that the gold layer is deposited directly without displacing the underlying base metal.

The RAIG bath is highly stable, with a wide operating window. Distribution is exceptionally uniform and independent of pad size, PCB surface geometry, and residual capacitance potential. Low coefficient of variation in gold thickness uniformity contributes to optimum process control and an absence of concern regarding nickel or palladium corrosion.

RAIG, through its reduction-assisted reaction, assures compliance with IPC4552. It provides fine geometry edge resolution and long-term deposit layer reliability.

RAIG is a proven alternative to previous attempts to achieve heavier gold deposits, i.e. extended dwell times, or depositing autocatalytic gold over immersion gold, both of which degrade the nickel and palladium under-layers.

As IPC specs change with 4556 and beyond, R&D Altanova is substantially ahead of the curve for corrosion and thickness control of gold. "This line was created for where the industry is going in the next 5 years," says Paransun. "We are more prepared on ENEPIG than anyone, committed to being the best, and ready to demonstrate what it can do."

> ***"ENEPIG (with RAIG) produces a gold surface that is ultimately free of porosity – a major reason why Micron consistently delivers pogo pin reliability at the highest level."***
>
> **Daniel Cram**, Mechanical Engineering Manager, Micron Technology

ENEPIG from R&D Altanova

- **Reduction-assisted gold process produces a uniform corrosion-free gold deposit**
- **Process delivers extreme tight pitch/spacing capability**
- **Excellent through-hole plating capability, full coverage up to 25:1 aspect ratio**

R&D Altanova Leadership

Seyed Paransun CEO and President

- 36 years in the semiconductor/PCB industry
- B.S. Electrical Engineering, M.S. Electrical Engineering, MBA
- Patented Pin Scale Systems Flexible Test Solution for Highly Complex Devices

What is the single most important trait in a good vendor partner?

"Consistent quality, the ability to help customers 'future-proof' their products, and service."

Vassilis Danginis Vice President, Quality

- 36 years in the semiconductor/PCB industry
- Responsibilities: Direct R&D Altanova Global QA activities, establish best-in-class quality goals for the PCB industry
- M.S. Materials Engineering & Electrochemistry
- Published works: Photoelectrocatalysis of Phthalocyanine and Its Metal Derivatives, and Failure Analysis Techniques for VLSI Circuits

What is the single most important trait in a good vendor partner?

"Effective communication and full accountability regarding quality issues."

Yubing Wang Director of Process Engineering

- 15+ years in the semiconductor/PCB industry
- Ph.D. in Chemistry
- 5 patents
- Over 20 published technical articles

What is the single most important trait in a good vendor partner?

"The ability to reliably build-in quality, and anticipate what customers will need in the future."

Richard Morbit Customer Service Representative

- 32 years in the customer service profession
- Responsibilities: serve as Altanova customers' primary contact for R&D programs; job status management, fabrication outsourcing, liaison with assembly houses.

What is the single most important trait in a good vendor partner?

"Dependability"

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When What You Want Isn't What You Need

Solving the age-old dilemma between design and manufacturing.

DEVELOPING A NEW product or process – or even aggressively refining them – is a juggle of "wants" and "needs." As manufacturers in an industry that constantly pushes the envelopes of performance, real estate, and – yes! – cost, our industry is precisely where the rubber meets the road in reconciling needs and wants.

Manufacturing is a curious profession that often relies on older equipment, processes and employee skills to produce cutting-edge "new" products. The catalyst is, of course, people: people who design and people who take those designs and make functioning product. As smart, talented, dedicated and thoughtful as these people may be, however, they often fail to communicate the needs vs. the wants.

Indeed, it can be hard to know what's on the other side of the hill.

I personally experienced this while involved with an OEM of instrumentation equipment. The company's CEO was a brilliant engineer who over decades had designed virtually all its expansive product line. He was truly an engineer's engineer. One little problem, however, was manufacturing the instruments was difficult, with abundant scrap at many stages of the production process. The machine shop had a devil of a time producing components that met specifications. Trying to outsource was a disaster because "merchant" shops failed miserably on the specifications, no-quoted the parts, or walked from the business. Not wanting to disappoint the CEO, everyone on the shop floor sucked it up and dealt with the high levels of scrap, rather than address the root cause. This high-end manufacturer had to charge healthy prices in part to compensate for the high cost of manufacturing.

As the CEO began to eye retirement, he decided it was time to cut back on some day-to-day engineering responsibilities by hiring a seasoned engineering manager to oversee the large engineering staff. Upon arriving at the company, the new engineering manager heard the horror stories from manufacturing about yield issues stemming from the tight, demanding tolerances. Trying to understand exactly why the tolerances were specified so tight, considering the function of the instruments, the engineering manager asked his staff why they chose to specify those tolerances.

The responses boiled down to two basic answers: The junior engineers said they took the specifications from existing products and applied them to new ones they were working on. Asked why, they responded, "That's the way it's always been done." And the senior engineers said, "Those are the tolerances the CEO requested."

The engineering manager then sought out the CEO and asked why such tight tolerances were needed on all the many component parts, as well as final product. He expected a lengthy technical explanation related to performance, patents, reliability, etc. – the things that created the "secret sauce" that made these products so great. Instead, the response was surprisingly simple: "I asked for those tolerances, but we don't need them. I figured if there was a problem with the tolerances someone would say so, and we would adjust accordingly."

When you have designed most of a company's products, and your name is on the building, employees tend not to mention when the "wanted" tolerances are both overly difficult to achieve, costly and not really "needed." Ditto, most junior engineers will cut-and-paste, not focusing on details such as tolerances or costly surface finishes, especially when told "that's the way it's always been done!"

I have seen similar scenarios play out over and again. Engineers specify materials, surface finishes, component placement and especially tolerances they "want," rather than understanding the manufacturing challenges that could be avoided by specifying what they actually "need." And too often, those on the shop floor will moan and groan about a given process or specification without bringing their concerns – and recommendations for improvement – to the design staff, so a possible improvement can be achieved.

Manufacturers in a fast-moving, technologically forward industry that supports customers even more focused on rapidly developing cutting-edge products too often lose the understanding between what is needed and what is wanted. This usually can be avoided.

Early communication between the design and engineering team and the fabrication and manufacturing team to discuss processing parameters of materials, surface finishes, balanced placement of components, and appropriate and achievable tolerances can make the difference between profitable and marginal success. This communication is most often appropriate at the time a part is quoted. The contract review that incorporates everything from initial quoting through order entry should be an open, proactive discussion to ensure what is "needed" is the top priority by all, and that what is "wanted" does not derail an otherwise successful product.

Understanding what is needed vs. wanted is a fundamental challenge when designing and manufacturing any product. Achieving a reasonable balance is not always easy but is worth the effort to eliminate wasted time and cost for all. ❑

PETER BIGELOW
is president and CEO of IMI Inc.; pbigelow@imipcb.com. His column appears monthly.

Bringing PCB Manufacturing Back is Easier Said Than Done

Government incentives are just part of the formula.

GOVERNMENT-LED DIRECTIVES of late are aimed squarely at bringing manufacturing back to the US. President Biden recently signed an executive order requiring the federal government to buy more goods produced in the United States and limiting the ability of federal agencies to issue waivers on overseas purchases.

Earlier, President Trump had approved regulations that increased the share of a product's components that must be produced domestically to qualify as US-made. He also imposed a 25% tariff on goods imported from China.

The $740 billion 2021 National Defense Authorization Act (NDAA), which took effect in January, includes a provision forbidding the purchase by the Department of Defense of printed circuit boards manufactured in potentially adversarial countries such as China, Russia, North Korea and Iran. Many in our industry have welcomed this new directive as a means of rebuilding the once-robust PCB manufacturing climate in the United States. But shoring up the domestic PCB industry will require much more.

It will take a Herculean effort that lasts well beyond the four or eight years of a political administration. It will take the kind of determination America poured into the space race after President Kennedy's "We Choose to Go to the Moon" speech.

Here is my shortlist of what I believe needs to be done to get North American PCB manufacturing headed in the right direction:

Education investment. China offers college degrees in PCB manufacturing. Most training in the US, by contrast, is on the job. Sure, trade associations and other third-parties provide training, and there are a variety of educational books on the subject. (I have authored one myself.) But while we talk as a nation about needing more products "Made in America," we don't encourage people to enter the manufacturing world through higher education. A degree is not necessarily required to be successful in electronics manufacturing, but certain skillsets *are* needed, whether one is on the plating floor or sitting in front of a CAM station.

I applaud companies that offer manufacturing internships, but I believe there should be a national initiative to establish vocational certification and associate degree programs in electronics manufacturing. It would make it easier for companies to scale up production when they can find skilled labor. And when they do find skilled workers, domestic manufacturers need to be willing to offer a competitive salary and benefits package to attract and retain good employees.

Equipment/supply-chain incentives. It's more complicated than just building a PCB factory in the US. For starters, the Chinese government (unlike in the US) subsidizes the construction and equipping of new manufacturing facilities. That puts our board builders at a disadvantage. How many small North American PCB fabricators – the majority of what is left in our industry – can afford to buy the latest direct imaging systems, laser drills and horizontal plating equipment, as is vital to remaining competitive?

In addition, most of that high-tech equipment is not manufactured here. In China, everything required to make a PCB can be found just a truck drive away, while America produces a limited amount of PCB laminate material, and most of the chemistry required for PCB manufacture is produced overseas. So, even building PCBs in the US is reliant on overseas sources. To truly bring PCB manufacturing back, we would also have to bring back manufacturing in a variety of related industries.

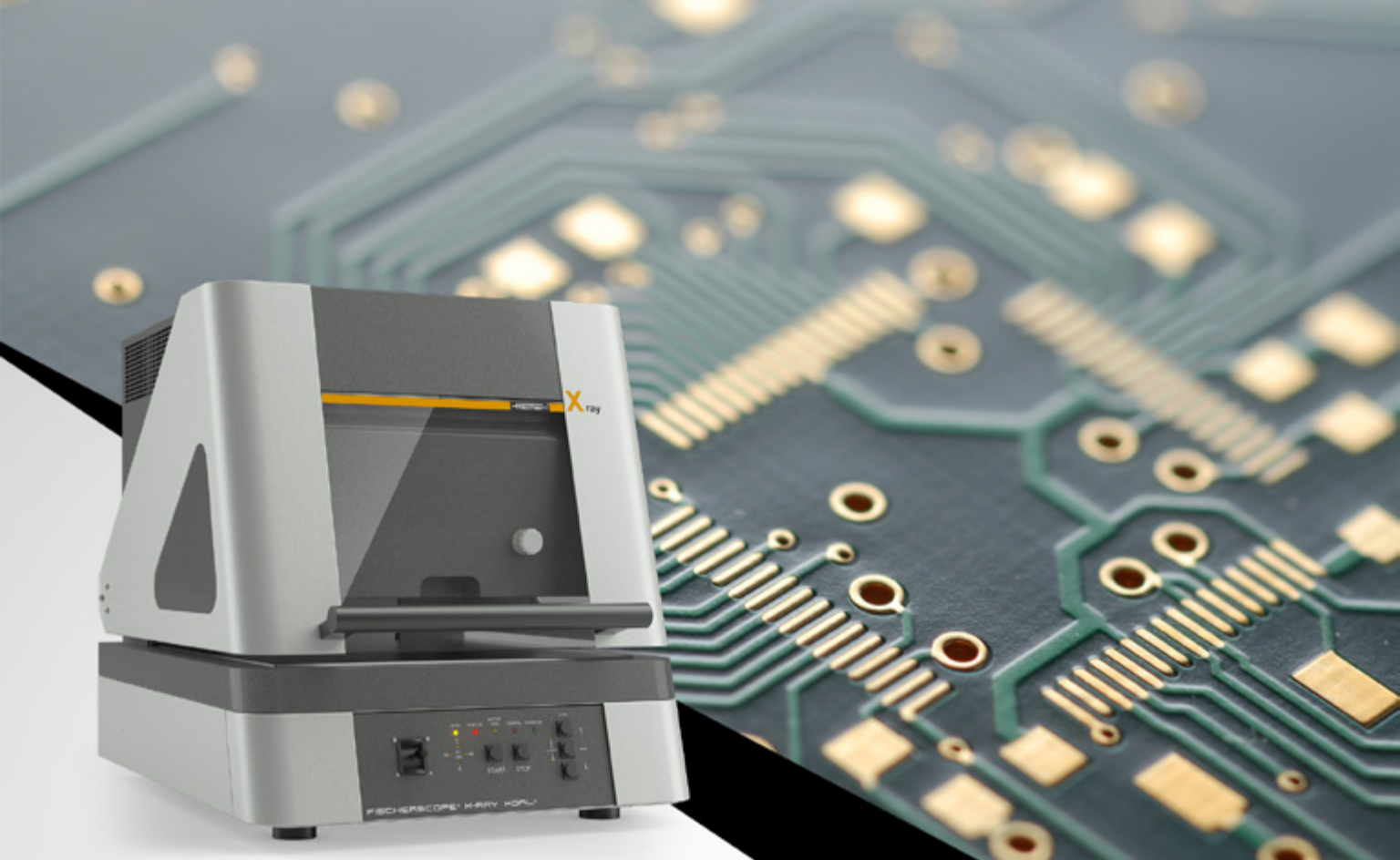
Government incentives for capital investment in manufacturing capacity may be necessary for PCB manufacturing to return onshore. Right now, domestic board shops lack sufficient capacity to reshore the industry even if they wanted to. As industry icon Hayao Nakahara says, "Rule #1: PCB revenue growth is directly dependent upon production capacity."

No ITAR offshore manufacturing allowed. I believe the American government should forbid building ITAR PCBs in "friendly-to-the-US" countries. For ITAR PCBs, a US manufacturer is required to maintain a secured facility, meaning all entry to that facility is locked. Employees who are US citizens or who hold a valid green card are required to wear badges while on the job and to gain access to the facility itself. Visitors need to register at the front desk and wear a special badge. Non-citizens must be escorted, even to use the restroom. If an unauthorized person is in a facility where ITAR work is present, it is considered "export by default," even if that person never saw or had access to the protected files.

On the other hand, I have visited unsecured offshore facilities that legally produced ITAR PCBs for US customers. Employees, some from non-friendly

continued on pg. 18

GREG PAPANDREW has more than 25 years' experience selling PCBs directly for various fabricators and as founder of a leading distributor. He is cofounder of Better Board Buying (boardbuying.com); greg@boardbuying.com.



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Solderability is More than Selecting the Right Solder

Quality is found in the design as well as the process.

SOLDER DEFECTS ARE inevitable. Reducing their risk is mandatory, especially if you're aiming to make money as a result of operations. Machines are certainly not "almost human," but they do go through seasonal changes and have moods. Without proper upkeep, they fall into disrepair. The goal in assembly is to dial in the thermal profile of the soldering equipment to minimize solder defects.

Footprint model accuracy is an enabler, but that work can be undone by improper routing and copper-flooding techniques. Placement too near the edge of the board where the temperature fluctuates to a greater degree can decrease yields through the soldering process. Tombstoning is one thing to watch for, but other dangers are present on the frontier.

The Goldilocks zone. Another defect can occur when one lead of a component is close to the edge while the other is farther inward. Wirewound resistors and inductors can become open circuits or more insidiously latent defects, where the wire pulls away from the lead only when there is a temperature rise or a mechanical shock to the system. Ceramic caps can actually crack when one lead solidifies before the other one.

From an electrical engineering standpoint, it is often desirable to place a DC blocking cap next to the RF in port. Further, the RF port is often on the edge of the PCB. It's common to position connectors along the edges. This means the leads will be exposed to widely varying temperature profiles, particularly when there are multiple rows of leads **(FIGURE 1).**

Likewise, placing a component in the "shadow" of a taller component can prevent the part from reaching the temperature sufficient for proper reflow. Somewhere between getting too hot and not getting hot enough is the "Goldilocks zone" where everything comes together just right. Managing placement issues of this sort relies on strong DfA rules built into the CAD system.

Consistency of the land patterns is of paramount concern. A flooded over SMD pad requires more time to reach reflow temperature than a pad isolated from the copper by thermal spokes. To meet emissions standards, we are advised to pour a ground plane on both outer layers to act as a Faraday cage around the electronics. This is one of several conflicts of interest the PCB designer faces.

We PCB designers are gatekeepers between the electrical engineering department and the factory. If this wasn't important, they wouldn't need us. Creating a PCB that meets the electrical requirements while maintaining manufacturability is our reason for existence. Don't ever forget that. The EE means well when they chase that last 1% of margin while sending the assembly yield into the tank. Balancing that zeal with the reality of manufacturing is the reason they hire us to do the layouts.

Thermal pads and solder volume. While many components have uniform lead sizes, some have one large pad and a number of smaller ones. It's easy to "overcook" the smaller perimeter-leads while trying to get the ground-slug to reflow. Reducing the amount of paste deposited on the ground slug will permit it to get more in line with the signal leads.

Rather than a single opening in the paste stencil, it is advised to create a number of windows in the stencil, to deposit a lesser but more controlled amount of solder paste on the ground paddle. One large opening in the middle of the ground paddle permits the squeegee to scoop out a little off the top of the paste window. Getting the same amount of coverage using an array of openings will give the solder a better chance of proper reflow **(FIGURE 2).**

An efficient board won't be roomy. Why? Because PCB real estate costs money for the material and makes the end-product larger than it has to be. If there is room for improvement in that area, it's a safe bet someone somewhere will do a better job of it and win the socket. Smaller is inherently faster, but the circuit density also gives rise to higher operating temperatures. We walk a tightrope between these two competing factors.

As the geometry shrinks, it gets harder to pour a clean ground plane. It's worth the effort to improve the DfA of the virtual board in the CAD software before getting into mass production. As density increases, the layer-count

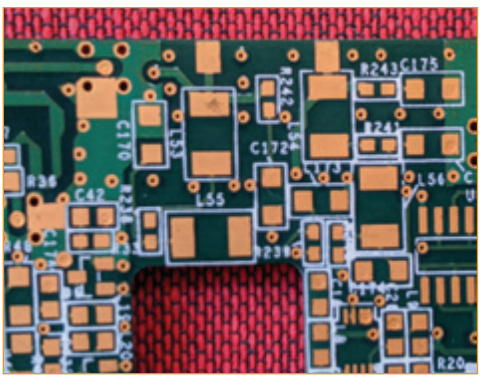

FIGURE 1. We paid the price in assembly for the feel-good moment of installing inductors too close to the edge of the PCB. Any edge, whether it is the outline or a slot, experiences more extreme temperatures during reflow.

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goes up. Half the layers might be ground planes. That can create a huge imbalance between various leads on the same device if proper thermal isolation is not designed in **(FIGURE 3).**

We must be careful with through-hole connectors with respect to the ground leads in cases like that. If the ground lead lacks thermal relief, it will reach soldering temperature much more slowly than the signal leads. The higher melting point of lead-free solders doesn't help our cause. The process window of solder that is hot enough to flow but cool enough to stay together gets tougher to maintain as we turn up the technology. Boards can blister, pads can lift, metal can migrate, and all these things can shut down an assembly line.

Prior to assembly, bare PCBs can be baked to reduce the amount of water molecules in the dielectric sponge. They can be cleaned to remove any oxidation on the lands. Extra flux may be applied to areas where wetting is found to be insufficient. Using local fiducials around fine-pitch components can aid in alignment of the pick-and-place operation. Quality is found in the design as well as the process.

Striking a balance between performance and DfA. The cruel part is the things we do to increase performance are often the cause of assembly issues.

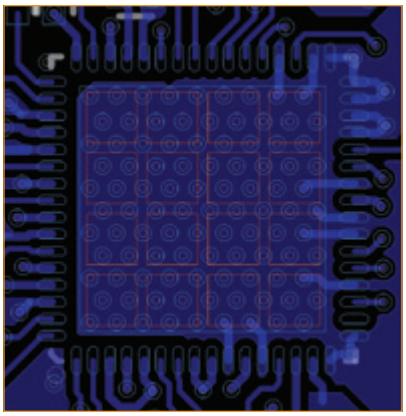

FIGURE 2. The heatsink provided by all these vias is nice for performance but could be a hindrance during reflow assembly. It could be too much of a good thing.

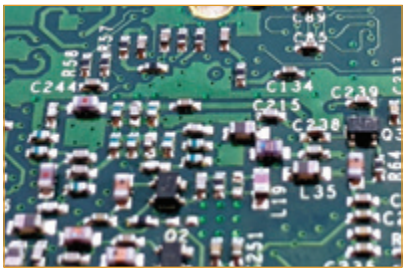

FIGURE 3. Use ground planes sparingly, with thermal relief as the norm.

We want to make a heat sink as good as possible for some pads to maintain optimal operating temperatures. Meanwhile, our high-speed signals are typically much thinner than the traces or shapes used by the power and ground leads.

Still, our goal is to design the board so all solder joints are as equal in thermal mass as possible. Running a board through reflow is like making the entire turkey dinner in that one big pan, including the pie! Everything wants to cook its own way.

One way to improve soldering results with disparate thermal loads is with a more gradual ramp to reflow temperatures. Fluxing agents and the granularity of the solder paste are two other levers the SMT operator can pull. While they can affect the process to some degree, good DfA practices can open the process window enough to avoid defects in the first place.

Nailing the tactical and technical challenges makes assembly a forever-learning process. At the end of the day, our job is to balance the competing requirements of great performance and acceptable yields. It starts with good footprint design and manifests through smart layout decisions. There will be people who are uncomfortable with the compromises. If everyone is equally uncomfortable, you've probably found the best way forward. ❑

Board Buying, continued from pg. 16

nations, appeared to have free access in and out of the facility. I never was asked to show proof of citizenship or issued a visitor's badge to wear. The government-controlled files received by those offshore manufacturing facilities were sent by US companies that had to abide by a stricter set of rules and take on additional costs. But there is apparently no organization or agency operating in friendly countries tasked with enforcing the rules imposed upon US facilities.

I was initially a proponent of the manufacture of ITAR PCBs in non-adversarial countries, but after discovering two sets of rules are applied when it comes to the handling of ITAR or EAR work, I changed my mind. I now believe a PCB with ITAR/EAR requirements should be kept stateside.

Improved customer service. Price isn't necessarily the only reason PCB customers choose to buy from offshore manufacturers. Many Chinese fabricators offer better quality and higher on-time delivery rates than their US competitors. All that aside, my frustration with poor customer service from certain American manufacturers – often due to a lack of employee training and use of obsolete equipment – has forced me overseas.

I've sold PCBs for nearly 30 years. It's not always about price. Sometimes it's a manufacturer's willingness to jump through hoops for a customer that keeps a job at a certain facility.

Of course, plenty of US PCB fabricators meet or exceed customer expectations, but overseas competition, while not perfect, gets better all the time. American manufacturers should take note.

If we want to increase the fabrication of PCBs in the US, an ambitious investment in people, places and things is needed. And to protect and strengthen the electronics supply chain that is vital to both national defense *and* commercial markets, there is likely a role for government to play as well. ❑

Footprints: Small Steps with a Giant Impact

Musings on land patterns and moon landings.

IN THIS MONTH'S column, I celebrate the importance of the humble PCB component footprint. I suggest that creating and leaving positive professional footprints on all we do in the Printed Circuit Engineering Association is imperative to the success of our industry. Next, I hand it off to PCEA Chairman Steph Chavez for some inspiring words as we tread into the new year. And as always, I provide a list of events coming up.

PCEA Updates

Not a day goes by that I don't come across hundreds of footprints. Not all are related to electronic components used in PCB design. Around a cattle ranch, for instance, some are left by turkeys, deer, cattle and other outdoor critters as they go about their daily business foraging for food in the snow. Some footprints are my own, which I make as I go about my daily business taking care of outside chores. Sometimes I make "bad" footprints, tracking them into the kitchen if I fail to shed my Muck Boots in the mud room before entering. These are hardly lasting footprints, as I'd like to point out. They are made without much thought and quickly fade with the next snowfall or the wipe of a mop across the floor.

Lasting footprints are quite different.

July 20, 1969 – Apollo 11. Over 50 years have passed since Neil Armstrong made the first footprint on the moon. As he climbed down the ladder from the lunar landing module "Eagle" and prepared to hop down onto terra Luna, he made the profound statement: "One small step for man, one giant leap for mankind." He took that step and made a footprint.

That iconic image of a footprint on the moon represents so much more than someone going about their daily business. The footprints made by Armstrong and fellow astronaut Buzz Aldrin on the dusty surface of the moon at Tranquility Base represent millions of actions and pieces of information – data, people, machinery and processes. They also represent their mission-critical project stakeholder Michael Collins, who stayed back to pilot Apollo 11's spacecraft Columbia, and all those working behind the scenes at mission control. All aspects of the mission had to fit together perfectly to achieve a common goal putting human footprints on the moon and returning to Earth safely.

We who work in printed circuit engineering know the importance of information and accuracy pertaining to the footprints made to be placed and remain forever on the surface of the printed circuit board. Component footprints must represent current, accurate information and feedback from all the PCBA project stakeholders. Circuit engineering, mechanical engineering, supplier management, component manufacturers, suppliers of solder paste, solder stencils and personnel in the business of looking at, considering or placing and inspecting a part in the component footprint: All these persons must be represented in that geometric imprint on the surface of the PCB.

The Printed Circuit Engineering Association recognizes all the realms of electronics must come together for the printed circuit assembly industry to work properly. We consider this our mission. Our goal is to make significant, lasting footprints on the face of the electronics industry through meaningful collaboration between our membership and the electronics industry overall. We seek to make giant leaps in educating our membership over the next few years to be able to dock with new technologies coming from beyond the horizons. We hope our actions will leave lasting footprints on the surface of the entire industry, which will serve to inspire those who come after us.

Message from the Chairman

by Stephen Chavez, MIT, CID+

January 2021 came and went. It's a month that always seems to fly by. Most, if not all of us, in the industry hit the ground running at the beginning of each year. With new aspirations or continued focus on attaining our respective short- and long-term goals, we eagerly get in the mindset and attack the new year with refreshed and rejuvenated minds coming off the holiday break. Each of us attacks January in our own way. Some start off with an aggressive attitude and game plan for success, while others may be a bit hesitant or cautious in their approach to the new year, and others simply take one day at a time as they let the new year unfold. However you start your new year, my advice is to go after it with all your passion and with the most positive attitude for success. I believe by doing this as we start off every January, we set the tone of success for the entire year. PCEA is doing just that!

PCEA hit the ground running in January and, by the time the month ended, we were in full stride setting the tone for the new year. As we headed into February, we continued to accelerate our momentum. We are doing it with passion and the most positive attitude possible! In doing so, there continues to be a lot of great activity within PCEA. From our individual members, to our existing regional chapters and newly

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formed chapters, to our new chapters in their infancy stages, to our newly added sponsors (Polar Instruments, American Standards Circuits, and NCAB Group) with others in the works, and finally within our internal PCEA Executive Board members, the PCEA collective continues to have excitement, and the PCEA buzz continues to be in the air!

Coming off a recent successful dual San Diego and Phoenix virtual chapter meeting at the end of 2020, I was excited to participate in our second multi-chapter virtual event in late January. The newly formed Minneapolis St. Paul chapter, along with Ontario, CA, and Greater Michigan, held a tri-chapter event, sponsored by American Standards. It was another PCEA virtual event held with great success! I recommend any individuals in those respective areas get connected and involved with local PCEA collectives.

As PCEA continues our core mission to "Collaborate, Inspire, and Educate" within in the industry, we continue to do our part to collaborate with many in the industry through the virtual world, while inspiring both industry veterans and the new generation of printed circuit engineers, and by adding valuable industry educational content and professional development in support of the evolution of today's printed circuit engineer. When I think about all the industry educational content, free and fee-based, offered through so many virtual events nowadays, it's hard to open my e-mail inbox and not find a virtual event (or two) offered by one company or another, or by an industry subject matter expert (SME) here and there, or from one industry source or another offering educational content.

Due to how 2020 unfolded, since mid-year last year, our inboxes have been filled with many "virtual" educational events offered. It's hard enough to find time to attend at least one of these events in each of our respective busy schedules. It's even harder to know which will provide the best or most valuable content. The challenge, then, becomes filtering what is considered "good content" or "not so good content," or what is just industry "noise." Which virtual event is "right for you" to squeeze in your already busy schedule and attend? That's the million-dollar question. I know this because I always have this dilemma daily as I go through my e-mail inbox every morning and continue this process throughout my day. Personally, if I had the time, I'd attend everything I could get my hands on related to printed circuit engineering. You never know where that "golden nugget of knowledge" will be found or who that next individual you may sync up with is who may add positive value or inspiration for you.

With PCEA, we do our best professionally and with passionate due diligence to ensure our educational content and virtual events are on point, so there is true industry collaboration. We promote the latest industry educational content, related directly to the evolving industry technology. Finally, with passion and excitement, we continue to offer inspiration for growth, professional development, and success to each individual taking advantage of all that PCEA has to offer. The next time you find yourself opening your email inbox and happen to come across that PCEA email, read it so you can take advantage of the PCEA opportunities. Don't just "swipe left!" From one printed circuit engineer to another, you won't be disappointed. I'm sure of this!

Refer to our column and the PCEA website to stay up to date with upcoming industry events. Many webinars are offered for "free". Take advantage of these opportunities as much as you can! If you have not joined the PCEA, I encourage you to do so by visiting pce-a.org.

I continue to wish everyone and their families health and safety. Best of success to all as 2021 unfolds.

Next Month

At press time we have more PCEA chapter meetings coming up to report on. Some exciting new chapters are forming, and we will touch base with some of our international chapters.

Upcoming Events

Below is a list of upcoming events:

- Mar. 8-12: IPC Apex Expo (online)
- May 11–13, 2021: IPC High-Reliability Forum 2021 (Baltimore, Maryland)
- Jun. 7-10: Zuken Innovation World (Scottsdale, AZ)
- Jun. 8-9: CadenceLive (online)
- Jun. 15-17: PCB East (Marlborough, MA)
- Oct. 5-8: PCB West (Santa Clara, CA)
- Nov. 10: PCB Carolina (Raleigh, NC)

Spread the word. If you have a significant electronics industry event that you would like to announce, please send me the details at kelly.dack.pcea@gmail.com, and we will consider adding it to the list.

Conclusion

Whether we realize it or not, we leave footprints across every activity we take part in. We leave physical footprints from our walk into the office. We leave digital footprints on the internet while searching for data used to create component footprints for our PCB design libraries. Hopefully, the professional footprints we leave throughout our careers will not only show that we collected data to achieve our own personal goals. Hopefully, our footprints will show interwoven paths to people whom we helped along the way to achieve their goals, too. Lasting footprints not only reflect two surfaces that happen to have contacted one another. They reflect all the brilliance of the people and ideas above and below their contact surfaces.

See you next month or sooner! ▫

Wearable Technology is Looking Good

For real-time and predictive interventions, smart patches are in style.

FOR MANY OF us in the technology sector, markets for high-tech products have remained resilient in the face of the effects of the pandemic. Despite lockdowns and restrictions, businesses are finding innovative ways to continue operating safely. Indeed, some seem to be thriving.

Gartner predicts the wearables market will grow 18% in 2021, reaching $81.5 billion. Ear-worn devices represent almost 50% of this market, with the current strong sales attributed to the WFH trend – as people upgrade from standard headphones for video conferencing – and the latest smartphones that have no 3.5mm jack.

Gartner notes, however, the increasing contribution of smart patches in the wearables space, rising to third in importance as sales of wristbands decline. This technology has ample potential to realize innovations in fields such as medicine and wellbeing that are so far undiscovered.

Bringing together multiple exciting technologies, such as flexible electronic materials, miniature sensors capable of detecting movement and various biomarkers, and micro-needles to deliver medicines when needed, smart patches are already changing healthcare. Conditions such as diabetes can be managed by detecting glucose levels in sweat on the surface of the skin and automatically injecting the appropriate quantity of insulin through an array of micro-needles. Researchers in the UK have considered similar patches to administer coronavirus vaccines.

In addition, sports such as American football and rugby are adopting inertial-sensing wireless patches placed in locations such as the base of the skull to monitor players' activity and measure the severity of impacts. The information captured can be used in various ways to prevent excessive stress and long-term injury, particularly brain injuries, by improving training or compelling individual players to take a time-out during a game.

It's intriguing to consider how smart patches can develop in the future to detect other signs of distress or illness that could prompt timely intervention. I've discussed my views on technology's role in improving care for the elderly on many occasions. Here we can see great potential to use data from smart patches to provide support without surveillance to safeguard our loved ones' privacy.

We want to know if an elderly relative has fallen or could be in danger, but installing video cameras or room monitors such as movement sensors is unacceptably intrusive. Using data from smart patches, which can be worn unobtrusively and more or less forgotten, an AI can acquire a picture of the wearer's normal day-to-day routines and quickly spot genuinely worrying deviations without showing specific data to healthcare providers or other third parties. Combining the knowledge built up over time with live data such as movement and heart rate can distinguish between the stillness of a regular nap and, say, an unexpected period of inactivity that could indicate a problem. A carer can then be advised to call or visit.

Alerts for abnormal health indicators could be helpful for younger people, too. The professional golfer Nick Watney discovered he had Covid-19 after his tracker wristband indicated a marked change in his normally steady breaths-per-minute rate. Although he was otherwise asymptomatic, the warning – which alerted him to get tested – allowed him to withdraw early from an imminent tournament when the result came back positive. He was able to start treatment quickly, as well as protect other golfers and officials on the tour.

In market terms, fitness-tracking wristbands are losing share. Smart watches are taking their territory as they integrate the fitness functions and many others besides into a convenient do-it-all device. Smart patches can coexist with the smart watch and – when combined with the smartphone and reinforced with analytics in the cloud – form a powerful fusion that can provide accurate early warnings of various conditions and encourage wearers to seek professional help without waiting to "feel" ill.

The combined power of wearables fits neatly with the emerging science of physiolytics, which captures and analyzes physical, biological, and behavioral data. Commercial organizations are among the early adopters of physiolytics, using the technology to monitor worker activities and performance. Not surprisingly, this has been contentious. Some say it amounts to spying and is narrowly focused on work rate, whereas on the other hand the information can be used to identify improvements to processes or tools that can help raise productivity and prevent overexertion. Physiolytics also goes together with employer wellness programs and health insurance, helping to tailor services and premiums. I am convinced we will see the science evolve, and more programs will be developed to address more scenarios in the future, amid ongoing arguments for and against.

Medical technology is among the markets least

continued on pg. 27

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The Rise of Power Integrity Analysis for Designers

Assumptions made in simulation may not reflect live board conditions.

As simulation and analysis continue to mature, the evolution is from a mechanism for finding problems to a methodology for preventing them. Many design teams have advanced beyond checking for violations and now use the tools to make informed design decisions early in product development. This results in better products reaching production floors despite condensed schedules.

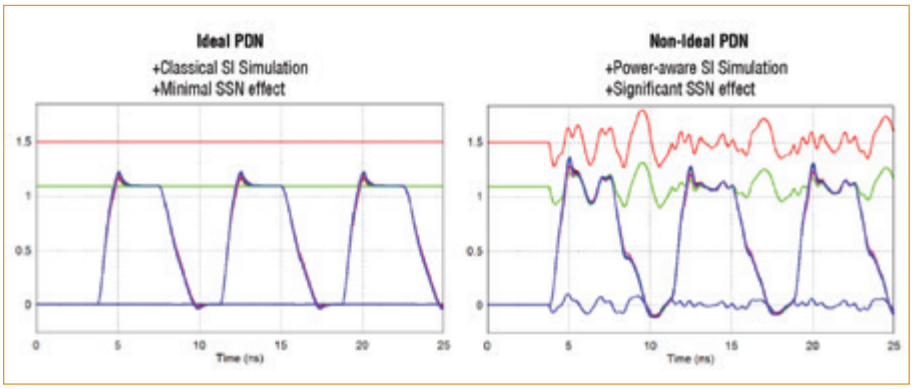

FIGURE 1. Most simulations fail to include accurate power information, leaving engineers to design with their head in the sand. By including power, you can see the entire picture and make informed decisions to create a reliable board that acts predictably.

Chasing correlation. With increasing reliance on simulation and analysis comes the responsibility to understand the capabilities and limitations of these tools. While able to calculate remarkably accurate results, they do rely on some basic assumptions. Not long ago, the "via" was assumed to be a plated hole extending the full thickness of the circuit board, resembling a coaxial cable, and could be sufficiently modeled as such. The drive for miniaturization and advances in manufacturing revolutionized this structure, introducing laser drilling, buried and blind, nested, and stacked constructs that quickly invalidated the coaxial cable model. Now they can be modeled in detail using 3-D solvers. Design teams, likely aided by simulation, recognized the via as the single structure in the signal path that presented both the greatest threat to signal integrity and the largest contributor to discrepancies between simulation and measurement. Had we not challenged the assumptions made regarding the via, simulation and measurement would continue to diverge as complex via structures became mainstream. Instead, traditional simulation, aided where necessary with 3-D electromagnetic field solvers, continues to produce results predictive of the actual measured product.

The ability to study, sweep, optimize, rinse and repeat every physical parameter, such as trace width, via size and material property of any (or every) structure in a signal's transmission path, enables a virtual explosion in data throughput. Where we once struggled moving from 2.5GHz to 3.125GHz, we leaped from 5GHz to 40GHz in a single product generation. This intensive, microscopic almost hyper-focused examination of every element along a signal path enables the throughput needed for technologies such as 5G, high-definition video and more. It has also exposed one of the fundamental principles: Electricity flows in a loop. In fact, every electron that rocketed down our meticulously groomed signal path must return to complete the loop **(FIGURE 2)**.

Measuring the whole loop. Not unlike the "via assumption," which served its purpose well until modern constructs rendered it obsolete, many signal integrity solutions utilize a "ground assumption," an idealized model for the return path, assuming an uninterrupted ideal reference. Made up largely of power and ground planes, the "return" has historically been modeled as continuous copper and had little effect on a signal's fidelity. Like the via, power and ground planes have undergone significant change in their composition on modern circuit boards. Shared voltage layers, often with substantial voids due to anti-pads and isolation areas, as well as the multilayer nature of power/ground routing today, have again put us in a situation where the assumptions made within the simulation environment may not reflect the conditions seen on the actual constructed board.

Complicating this is the variability in the path itself. While most routed signals follow an intuitive route from pin-to-pin, the return is much more complex, often containing numerous connections and redundancies. The actual route of the returning current can be difficult to establish, as it is highly influenced by inductive forces directing current flow to the path of least impedance (not necessarily the shortest point-to-point distance). Further, the returning current will change its route with

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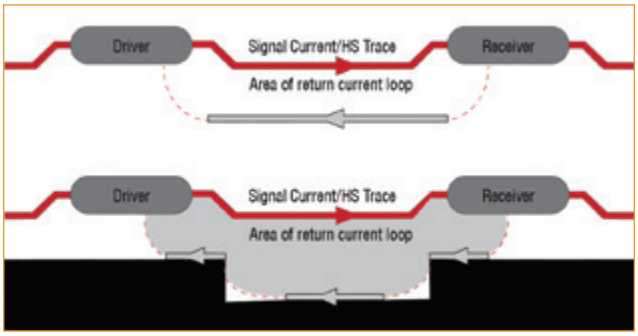
frequency, making the structural model-by-element approach used for the outgoing signal nearly impossible **(FIGURE 3)**.

Fortunately, much like we use the 3-D solver to overcome via challenges, power integrity (PI) offers a solution for return path and power management. PI can be used (like the solver for vias) to create a detailed model of the power and ground system, or power distribution network (PDN).

Power-aware signal-integrity simulation with integrated 3-D EM modeling represents the pinnacle of the electrical simulation market today. Phrases like "virtual prototype" and "digital twin" are used largely and without exaggeration to describe the accuracy achievable with these tools in the proper hands. The combined technologies – SI, PI and 3-D EM – can be used to predict a product's behavior without building, yet it is not an all-or-nothing gain. Tremendous incremental benefits are in each area as simulation understanding grows. Much has been written about signal integrity, and its virtues are well accepted. Power integrity, by comparison, is a relative newcomer and its use and value not as widely known. The benefits associated with visualizing power noise and signal noise simultaneously when making signal quality measurements are straightforward and desirable but may require greater effort than necessary for every signal.

An intermediate approach may be to use PI and SI tools independently. Power analysis can ensure the power and ground system provides the return path meets predefined requirements. SI analysis can then proceed with confidence, knowing any deviation from the assumed "perfect" return path, native in the tools, will be bounded and predictable based on the PI results. Additionally, PI can ensure the full supply voltage – and therefore the same voltage swing being simulated – is available to even the farthest chip from the supply.



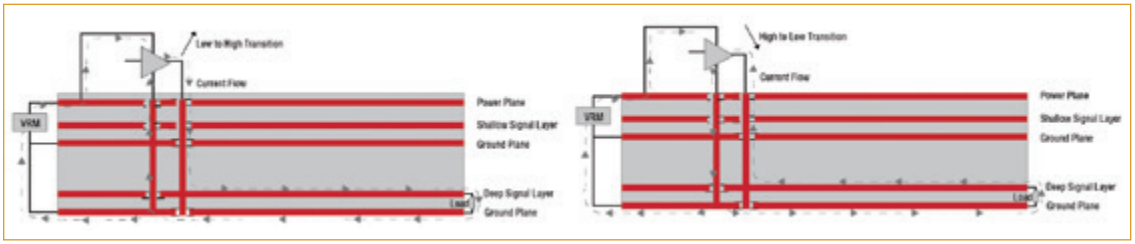
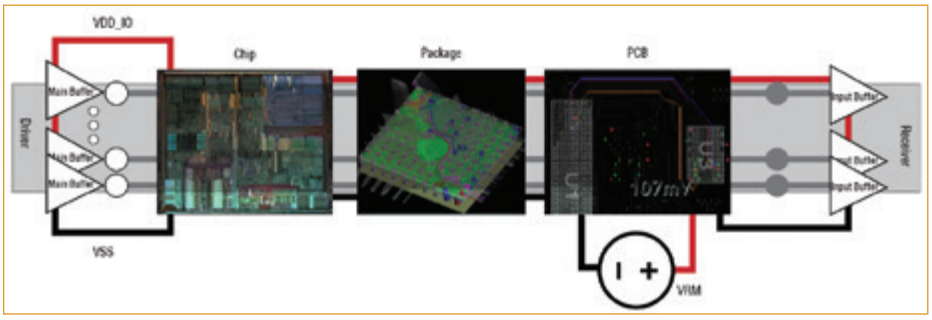


FIGURE 2. Electricity flows in a loop. Critical design flaws can be missed by not taking return path into consideration in simulations.



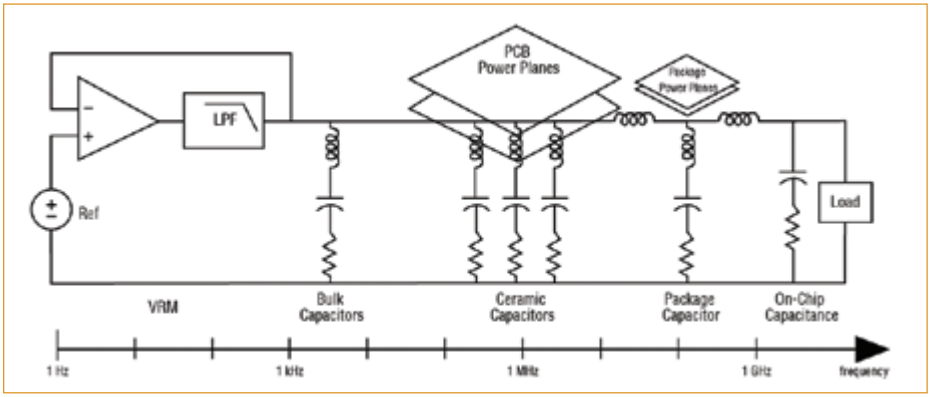


FIGURE 3. EM solvers enhance the accuracy of simulation; adding power integrity completes the picture.

Solving the power problem. Conceptually, creating a functional power delivery network is easy; simply provide a continuous copper path from power source to each load capable of supplying adequate current at a steady voltage and an uninterrupted, continuous return path for each switching signal. The difficulty is not in the complexity, but rather the enormity. Multiple voltage requirements,

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Winning the War against Analysis Paralysis

The "founder" of TMI asks, How much is more analysis worth?

JUST BECAUSE SOMETHING *can* be done doesn't mean that it *should* be done.

A few customer encounters this past month caused an issue to ricochet around in my mind like a 1970s pinball machine. I'm referring to a trap we've all fallen into: analysis paralysis.

Three interrelated definitions I have for analysis paralysis are worth enumerating:

1. The condition of being indecisive while overanalyzing alternatives. (Classic analysis paralysis.)
2. Allowing a project to mushroom into something bigger than it needs to be to get the job done. (This column is a good example.)
3. Using data from the most expensive tools you own just because you have the tools or the data (e.g., it's expensive and took a lot of time, so it must be good).

It's not that analysis or expensive tools aren't good, but their employment is an optimization process.

Relative to the above, I can't and won't lecture on trying to rely on overanalyzing things or using "too much information" as if I have a solid handle on it. When non-engineers say to me, "That's TMI," I say, "I invented TMI."

Perhaps my first (but probably not *the* first) major encounter with this problem was my final semester as an undergraduate engineering student. The class was computer-aided design, and our final project was to develop a CAD program to solve an engineering problem. Every decision I made on the project was ill-advised. I spent hundreds of hours writing thousands of lines of code alone in the bowels of the open-all-night engineering labs, writing a masters-thesis program for an undergraduate class. Stupid, stupid, stupid. It consumed me. I kept adding features, and I somehow thought this program that would never see daylight had to optimize a heat-removal problem for a hypothetical nuclear power plant. A rendering of me in the all-night engineering labs is shown in **FIGURE 1**.[1]

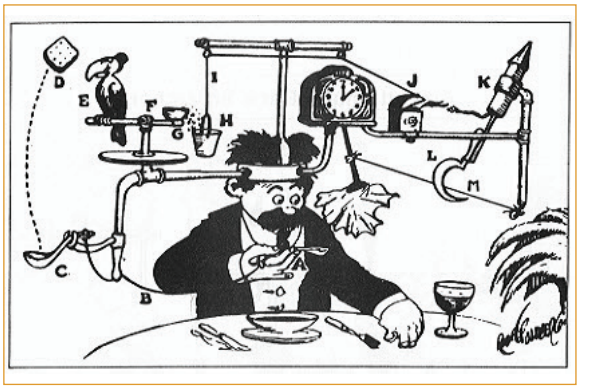

FIGURE 1. Cartoonist Rube Goldberg's depiction of Professor Butts and the Self-Operating Napkin (1931). Soup spoon (A) is raised to mouth, pulling string (B) and thereby jerking ladle (C), which throws cracker (D) past toucan (E). Toucan jumps after cracker and perch (F) tilts, upsetting seeds (G) into pail (H). Extra weight in pail pulls cord (I), which opens and ignites lighter (J), setting off skyrocket (K), which causes sickle (L) to cut string (M), allowing pendulum with attached napkin to swing back and forth, thereby wiping chin. (Public domain; originally published in *Collier's*, Sept. 26, 1931.)

I'm obviously not the only one who has struggled with this. Lee Ritchey once quoted his CPA as saying, "Electrical engineers were the smartest dumb people … designing all sorts of innovative, clever products, but often having no idea what things cost and often seeming not to care or thinking cost containment was part of the job. These same engineers had the financial success or failure of the company they worked for in their hands and didn't seem to know it."[2]

What I want to focus on here is the cost in terms of *time and effort*. We should always ask, "How much is more analysis worth?"

Here are the questions that crossed my radar last month while abstracting the discussion to address anyone who's ever wrestled with TMI and analysis paralysis:

- While demonstrating some cool productivity-enhancing stackup-design features, a guy interrupts the demonstration to ask, "Some tools do Monte Carlo analysis. Does this do Monte Carlo analysis?" (Note: completely orthogonal to the discussion.)
- Can you make the software do something with an invalid modeling premise, utilizing our existing VNA measurement data, while collaborating with a third-party tool?

I won't discuss question two in detail here, but I'm reminded of several parallels that have been bouncing around in my head since these questions popped up.

Time to shoot the engineers and ship it (T2SE). I'm not sure who coined this phrase, but I'm glad they did. It's not intended to mean "ship shoddy products." It says engineers, left to themselves, may tend to lose sight of profitability in favor of "further analysis."

Sir R. A. Watson-Watt, the inventor of radar, described how a "good enough" design led to a turning point in World War II. "The best design had to be rejected because it

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would never be achieved, and … the 'second best' would be achieved too late to be used by the armed forces when they needed it. The third best would be adequate and was available in time, and it was what won the Battle of Britain."

All models are wrong, but some are useful. George Box, another Brit, was a statistician known for his work in quality control and experimental design. This quote is actually a paraphrase of Box's 1976 paper[3], which is generally considered the earliest source. The full quotation is, "Since all models are wrong, the scientist cannot obtain a 'correct' one by excessive elaboration. On the contrary, following William of Occam ("Occam's Razor"), he should seek an economical description of natural phenomena. Just as the ability to devise simple but evocative models is the signature of the great scientist, so overelaboration and overparameterization is often the mark of mediocrity."

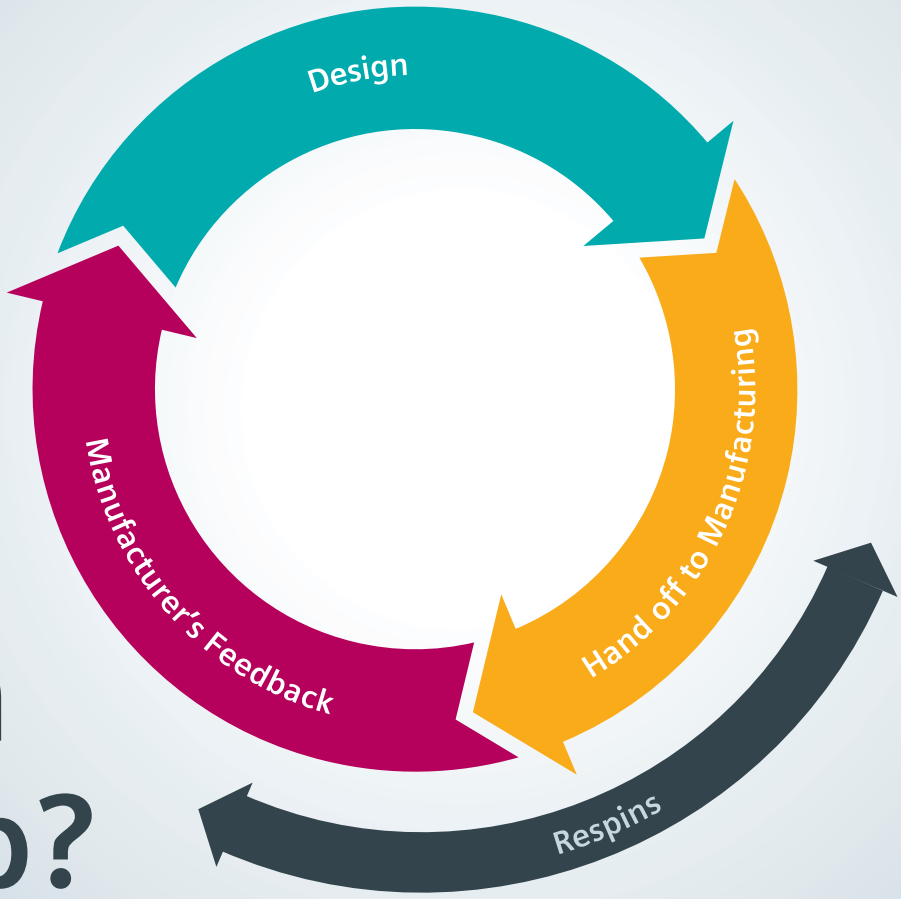
Amen, Brother Box.

Embrace this and you'll be free to get actual work done, rather than stressing about searching for the Holy Grail.

When the Monte Carlo question came up, I thought of the sign in FIGURE 3. Two trails circle the Lava Canyon on the south side of Mt. St. Helens, connected by a suspension bridge. Living as I do in the Pacific Northwest, I've made this hike many times with my family. The northern route is treacherous, and the southern side is more manageable. Regardless of the route (I take the southern one), if you get close to the edge, as some have done, you can end up a statistic. I've never performed a Monte Carlo analysis of US Forest Service data on wind direction, coefficients of friction, time of day (light/darkness), temperature, precipitation, etc. Instead, I simply assess where my feet and kids are relative to the failure criteria. I don't do the hike in the middle of the night or in the rain, for example. We all survived, not because we performed

FIGURE 2. All models are wrong, but some are useful. (Image courtesy of Todd Westerhoff, Siemens EDA.)

SIEMENS



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detailed statistical modeling and analysis, but because we used good, old-fashioned common sense and stayed on the trail – just as I recommend here for PCB stackup design.

Everything should be as simple as possible. Albert Einstein famously said, "Everything should be as simple as possible (but no simpler)." A Russian engineer reminded me of a story that speaks to this.

> A billionaire wanted to develop a method to predict which horse would win races. He gave the task to a biologist, a mathematician, and a physicist. They had months to come back with an answer, and the successful proposal would get a million dollars.
>
> The biologist said, "Well, if I know the exact pedigree of the horse, the success of its parents, how it was fed, how it was treated, I can accurately predict a horse's maximum speed."
>
> The mathematician said, "If we have accurate statistics on previous races, I can predict the approximate results of this ..."
>
> The physicist said, "With 10 years, 50 million dollars, a lab and a staff, we can predict the outcome. I've already built a model of the motion of an elastic, spherical horse in a vacuum!"

I guess the good news is you can model it in the frequency domain if you know the radius ….

Management implications. Peter Drucker, the Mark Twain of management authors, is the guy who coined the term "knowledge worker." One of the reasons I like him is he says things like, "There is nothing quite so useless as doing with great efficiency something that should not be done at all."

It's been said that when you have a hammer, every problem looks like a nail. From my recent experience, I'd say a corollary is, "When you have an expensive VNA and a bunch of measurement data, you'll be tempted to look for unreasonable places to use it, even if it goes against common sense." I see this in day-to-day interactions more often than you might think.

In decision theory, the expected value of perfect information (EVPI) is the price one would be willing to pay in order to gain access to perfect information. It's an attempt to assess how much we'd be willing to pay for a perfect answer or a perfect model with zero risk. Perhaps without knowing it, this is what we're pursuing with many simulations and simulation models. Return on investment (ROI) always needs to be factored in.

An informal, possibly unspoken part of an engineering manager's job is to keep their team from going sideways on projects by analyzing things to death. The problem is it's an optimization process, and engineering managers may not have a clear handle on the "value of perfect information." Communication is key here, and engineers are attracted to complexity like moths to a flame.

Back to Monte Carlo analysis. I suppose most readers know what Monte Carlo simulation is, but here's a brief explanation. According to Wikipedia, Monte Carlo experiments rely on repeated random variation of multiple parameters to solve problems that are difficult or impossible to solve using other approaches.

Monte Carlo analysis clearly has a place, but you need to have good process and process-variation data to make it work. Theoretically, Monte Carlo analysis would give the expected limits of the actual outcome (with confidence factors). Even if you could do it, putting in valid data for the different process variables and sufficient data to be statistically relevant is a massive challenge. And it would not likely be consistent across multiple fabricators.

EDA (electronic design automation) tools, including those made by my company, can be super-useful, if you know what they are really modeling. Even here, the results are only as good as the data put in. As an example, most roughness models are "wrong," but useful and needed.

In the context of this discussion the dependent variable of interest is *impedance*. The primary parameters that affect impedance are shown in **TABLE 1**, including their relative contributions.[5]

Virtually everything I do is focused on getting these parameters right. If you work this list top to bottom, starting with

FIGURE 3. Sign on Lava Canyon Trail, on the south side of Mount Saint Helens.

TABLE 1. Factors Influencing Impedance

Factors	Type	Rank	Description	Influence	Contribution
Dielectric Thickness	Material	1	Core	Thickness uniformity	51%
		2	Prepreg	Resin content; resin flow and % thickness	
	Process	3	Lamination	Board thickness	
Dielectric Constant	Material	4	Core		22%
			Prepreg		
Trace Width	Process	5	Exposure	Exposure undercut	18.5%
			Etching	Etch factor	
Copper Thickness	Process	6	Plating and scrubbing	Distribution; current density	5.5%
Solder Mask Thickness	Material	7	Ink viscosity	Trace thickness; gaps/ spacing	3%
	Process		Printing		

getting a better handle on dielectric thicknesses and working your way down, you'll be better equipped to dial in your nominal parameters with enough margin to know you're not going to fall off the cliff. And yet every week, I see engineering teams straining to perform complex analyses using datasets with questionable merit, without fully grasping the parameters and priorities (1 through 7) noted above.

With enough effort and data gathered over time, we can eventually model all the above using statistical methods like Monte Carlo. **FIGURE 4** shows the results of tons of effort.

Conclusion

Detailed statistical analysis is a reasonable enterprise for a materials or process guru. But it's a ton of work and unless you're paid to do science projects, it's probably not worth it. If your main work product is to get products that work into production, it's probably sufficient to understand where you are relative to the edge of the cliff. Do the best you can with the seven parameters noted above, and you should be fine.

Do everything you can to reduce or remove unknowns, by all means, but use common sense before leaning into modeling methods and tools that give an artificial sense of comfort.

I'll wrap up with a comment I heard from a wise engineering manager over 20 years ago: "I want to know what time it is, not how to build a watch!"

Shoot me an e-mail if you agree. Bonus points if you include an example! □

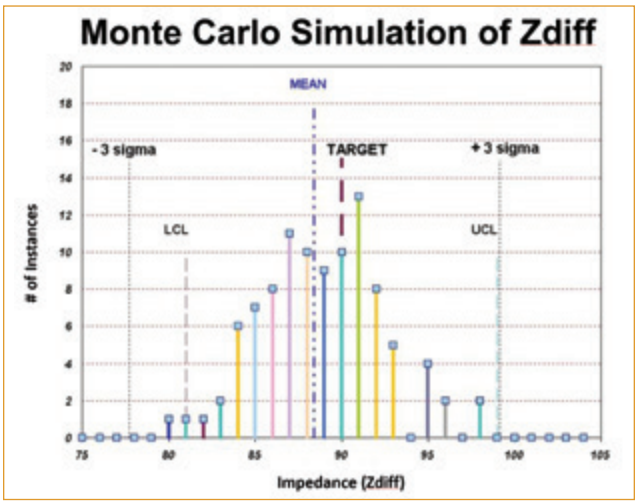

FIGURE 4. Differential impedance distribution from Monte Carlo simulation. (Data courtesy Happy Holden.)[5]

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5. Happy Holden, e-mail correspondence.

Material Gains, continued from pg. 19

impacted by the Covid-19 pandemic, according to commentary by Yole. In the longer term, I believe the sector could thrive, as behavioral patterns are likely to change significantly.

Conversely, Gartner shows disappointing figures for smart clothing. Tremendous untapped potential is here to improve comfort and wellbeing and protect the environment by harvesting the wearer's energy to power other wearables placed around the body. It could be that unexciting clothing styles have held back progress so far. Effective partnerships could provide a way forward, bringing fashion and technology brands together to create smart clothes that look good and function well. The aesthetics are critical, and tech companies will never do that as well as experienced fashion designers.

It's a sector that's seriously lagging in this otherwise fast-growing market, and it needs to catch up. □

PI, continued from pg. 23

rising power consumption and increasing circuit density are but a few of the challenges facing the power system. Even the simplest products routinely have multiple power domains occupying the same physical space as a single voltage once did. Exacerbated by a relentless drive toward miniaturization, they combine to create a PDN that has evolved to a point where there is just too much for visual inspection to be reliable. With methods in place to ensure quality power delivery, we will shift focus to the secondary, albeit equally vital, role of the PDN, the return path. Disruptions in the return path, including ground slots and reference layer changes, are fast becoming the most problematic issues seen in SI. Often difficult to detect in a lab setting, these troubles originate in the power plane routing, but routinely evade detection as they fall in the area where the SI simulators are assuming conditions that do not reflect the actual PCB.

Going forward, this series will address problems commonly associated with the power side of system design, discussing how to improve power integrity through simulation in both power delivery and the return path. Ultimately, we hope to encourage design teams to embrace simulation, understand its limitations, and continue to incorporate complementary technologies, like 3-D solvers and power integrity, to extend their current capabilities. □

GETTING EMBEDDED with IPC-2581C

The new data transfer format provides comprehensive support for embedded components. by **CHRIS SHAW**

Board designers today must provide fabricators files beyond those containing the design data in order to describe what is needed for embedded components. It's a nonstandard process, different for each designer-fabricator relationship, so every fabricator must contend with multiple, disparate, nonintelligent formats and communications. Sometimes the additional files get out of sync with the design data, thus requiring phone calls or more revisions of the files to sync up what is intended. This is a slow, manual and error-prone process, which is still used even with other intelligent data transfer formats.

An additional challenge is that while some ECAD tools may now support state-of-the-art embedded components – e.g., face-up (flipped), pins on both top and bottom, formed (etched, printed) – the handoff to manufacturing formats has not evolved to support them at the same pace.

Ideally, every type of component defined in the CAD tool would be accurately represented in the handoff to manufacturing format, so fabricators could automatically read all requirements without the need for additional documents or phone calls.

New Attributes

IPC-2581B introduced basic support for embedded components, but this was only for traditional surface-mount components with all their pins underneath the package body.

In IPC-2581C, the *mirror* attribute is enhanced to indicate not only a component mounted on the underside of a board (that is, the underside of the bottom layer), but also to indicate mounting on the underside of *any* layer of the board. Therefore, embedded components mounted on the underside of internal layers can be described. In addition, a new attribute called *faceUp* is introduced to describe a component flipped on its back before being mounted on the same side of the layer. As previously noted by Shah[1], **FIGURE 1** shows the full range of embedded mounting options provided by combining the *mirror* and *faceUp* attributes for the case of an IC with pins on the underside of its package.

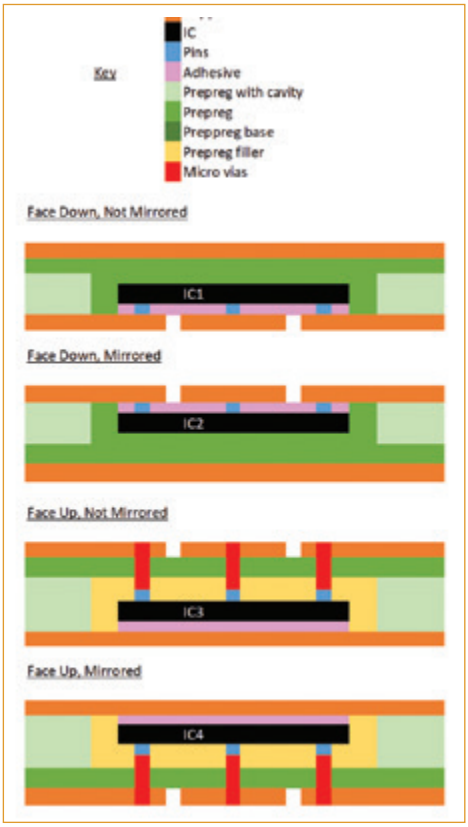

FIGURE 1. Embedded mounting options.

A new attribute attached to the component, called *slotCavityRef*, identifies and locates the cavity in the bare board in which the component will be placed. In addition, the component package definition is enhanced to permit pins and their associated markings on the topside of the package. Now, packages can be defined with pins on both the topside and underside, or topside only. Moreover, the underside of a package extending below the plane of the mounting layer can be defined **(FIGURE 2)**.

The IPC-2581 schema describes all details of a PCB (outline, stackup, artwork, etc.) within a *Step* element, and a step can be repeated to produce a panel array. In IPC-2581C, two or more steps, each representing an entirely different PCB or custom IC die, can be linked by newly introduced *Port* elements. A port represents one of three physical connection types: wirebond, connector mating, or surface mount pad. Therefore, numerous hierarchical/system scenarios can be described in a single IPC-2581 file, including the examples shown in

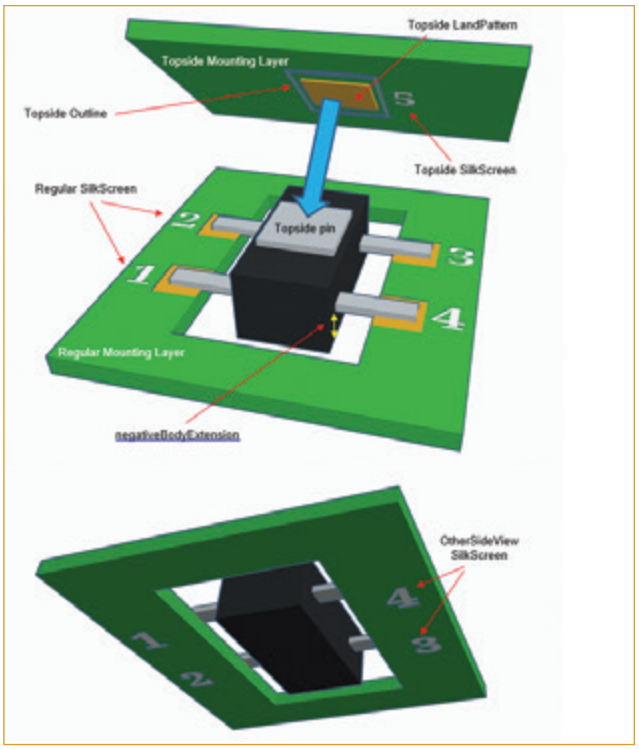

FIGURE 2. New attributes attached to the component broaden the way packages can be defined.

FIGURE 3. Uses for ports include system simulation or system assembly instructions.

Etched or printed formed components are supported too at both surface and embedded locations. A new layer function type of COMPONENT_FORMED is assigned to either the etched resistive layer or the printing material layer. This is the new full list of component mount types in revision C: SMT | THMT | EMBEDDED | PRESSFIT | WIRE_BONDED | GLUED | CLAMPED | SOCKETED | FORMED | OTHER.

Embedded coins or heatsinks, such as solid pieces of conductive material, are becoming more prevalent in PCB design. IPC-2581C defines not only the cavities in the PCB substrate to house this material, but the material itself, as defined by the new *Model* element as a series of dimensioned 3-D extrusions **(FIGURE 4)**.

A *Component* definition of the coin/heatsink references both the model and its cavity. Its material specifications are either referenced from the model or from a spec referenced in the bill of materials (BoM).

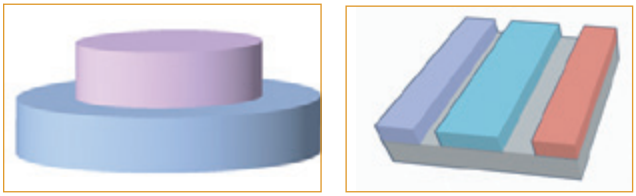

FIGURE 4. Among the shapes that can be defined are embedded coins or heatsinks.

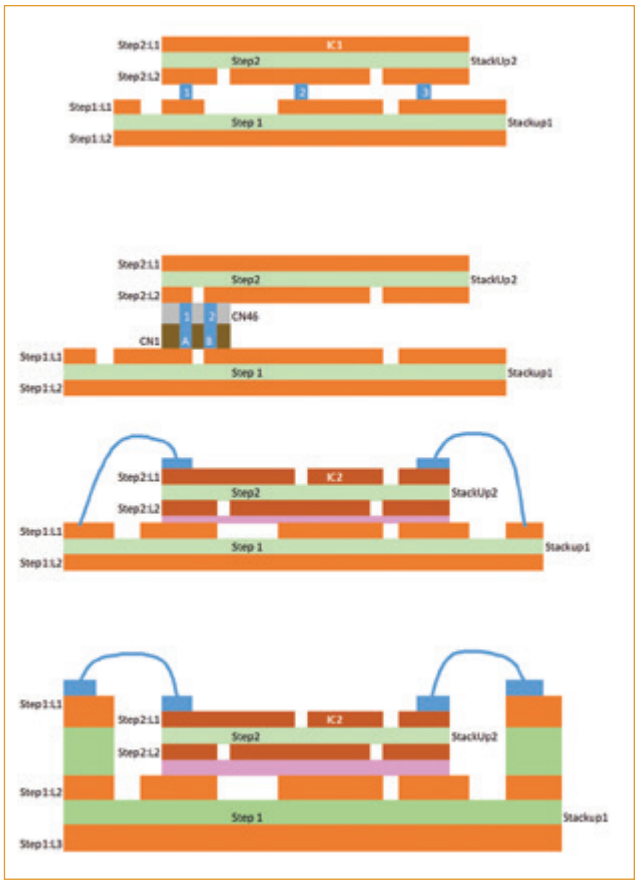

FIGURE 3. IPC-2581C can describe a custom IC with pins that connect to a motherboard (top), a motherboard connected to a daughtercard by connectors (middle), and a non-embedded custom IC wire-bonded to a motherboard (bottom).

Benefits

With comprehensive support for embedded components, cavities and hierarchical system definition, PCB designers can pass on this information to manufacturing partners using IPC-2581, an intelligent format in a single file, eliminating slow, error-prone processes.

Summary

IPC-2581C provides a rich option set for defining state-of-the-art embedded components, for fully automated hand-off to manufacturing. Visit ipc2581.com for more information about companies that support it, test cases for revisions A, B and C, as well as links to download free IPC-2581 readers from several companies. ▫

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PCB Design and Fabrication Concerns for MILLIMETER-WAVE CIRCUITS

Essential for mmWave applications, phase accuracy is affected by a host of variables. **by JOHN COONROD**

Applications for millimeter-wave (mmWave) circuits are growing rapidly, from collision-avoidance radar systems in autonomous vehicles to high-data-rate fifth generation (g5G) new radio (NR) cellular wireless networks. Many such applications are driving higher frequencies, above 24GHz, where wavelengths are smaller and the smallest attention to circuit design and fabrication can make the biggest differences in electronic product performance. Understanding the differences between PCBs at mmWave frequencies and lower frequencies can help avoid circuit manufacturing mishaps for many applications that are soon to require millions of double-sided and multilayer PCBs at those higher frequencies.

RF PCB Technologies Overview

Compared to lower frequency circuits, high-frequency RF/microwave circuits are sensitive to circuit materials and fabrication processes. Whereas some electrical circuit functions such as power lines and digital control may be well-supported with low-cost FR-4 circuit materials, RF, microwave and mmWave circuits require much higher performance circuit materials to minimize signal losses and distortion. Many multilayer mixed-signal PCBs with many different electrical functions are a blend of different types of circuit substrate materials, with materials selected according to behavior best suited for the types of circuit functions fabricated on that layer.

High-frequency PCBs are typically based on one of three common circuit configurations: microstrip, stripline, or grounded coplanar waveguide (GCPW) circuits **(FIGURE 1)**. The conductors and ground planes are configured differently for each circuit type, with electric (E) fields and current density depicted for each with single-ended transmission lines. The E fields are shown as coupled from the conductors to the ground planes. For differential circuits, two conductors are used. For a differential microstrip circuit, for example, the E fields would be coupled between two signal conductors on the top layer and the ground plane below. High-frequency circuits based on such transmission-line configurations are sensitive to circuit material parameters and PCB fabrication details, especially at higher frequencies.

The depictions of the three circuit types in Figure 1 are rough approximations and will appear differently with changes in frequency. At higher frequencies, current density will be thinner in a cross-sectional view due to skin effects, while the E fields will be more condensed. Electromagnetic (EM) waves generated by variations in each circuit's E and magnetic (M) fields (not shown) would propagate in a direction perpendicular to the two-dimensional circuit depictions, outward from the page.

The performance of all three types of high-frequency transmission lines depends on the dielectric material supporting the conductors. In the stripline case, the conductor is surrounded by dielectric material; for microstrip and GCPW circuits, in which the E fields extend beyond the dielectric material, the air surrounding the circuit contributes to the total dielectric environment of the circuit, so propagating waves in these circuits travel through media with a dielectric constant (Dk) that is a combination of the Dk of the substrate material and air, which is approximately 1. The resulting dielectric environment for microstrip and GCPW circuits is what is known as the effective Dk.

The GCPW depicted in Figure 1 is tightly coupled, with small

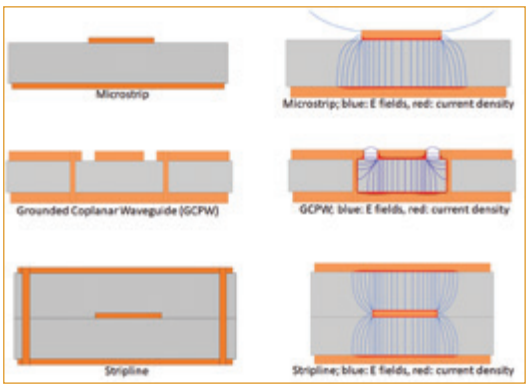

FIGURE 1. Cross-sectional views (left) for three common high-frequency circuit types, microstrip, grounded coplanar waveguide (GCPW), and stripline circuits, and corresponding electric (E) fields and current density for each circuit type (right).

spaces between the ground planes and signal conductor on the top coplanar circuit layer. Larger spaces result in a more loosely coupled GCPW circuit. Tightly coupled GCPW have a greater percentage of E fields in air compared to loosely coupled GCPW, with the air contributing to a lower effective Dk for tightly coupled GCPW than for loosely coupled GCPW, where a greater percentage of the E fields is in the dielectric substrate material (with a higher Dk than air).

Available signal power tends to decrease with increasing frequency, requiring close attention to minimizing signal loss in high-frequency circuits. Maintaining an impedance-matched environment is critical for minimizing the loss of interconnected components in a high-frequency circuit or system, such as the transmission line between the signal generator and load in **FIGURE 2**. A passive component such as a high-frequency transmission line will exhibit some amount of insertion loss, typically due to conversion of signal energy to heat, even when impedance-matched to generator and load. But when it is not impedance-matched (Figure 2b), signal reflections at mismatched transmission junctions result in return loss, increasing the total loss of the transmission line from a nominal 3dB in the matched state to 6dB in the unmatched state. When signal power must be conserved, insertion loss and return loss must be minimized. They can be measured with a vector network analyzer (VNA) by making scattering (S) parameter measurements of S_{21} for insertion loss and S_{11} for return loss.

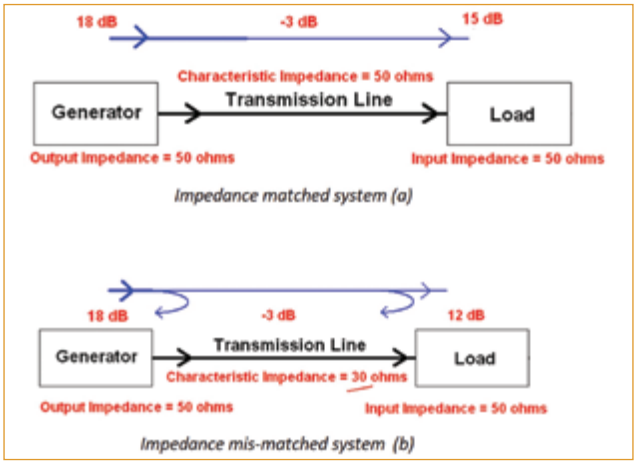

FIGURE 2. Less signal power will be lost between a generator and load with impedance-matched transmission line (a) than when using a transmission line not impedance-matched to the source and load (b).

The insertion loss of a high-frequency circuit is the sum of several different types of loss, including conductor loss (from the metal conductors), dielectric loss (from the substrate materials), radiation loss (from energy radiating away from the circuit), and leakage loss (from energy leaking between the cop-

per planes). A reduction in any one of the four types of losses will result in less insertion loss for a high-frequency circuit.

Leakage losses are typically a concern for substrate materials with relatively low-volume resistivity, such as semiconductor materials, but not for high-frequency circuit materials that typically exhibit high-volume resistivity. Leakage loss can be an issue for high-power circuits but is usually not a concern for the signal power levels used in mmWave circuits. Radiation loss can be a concern at mmWave frequencies, and it can be modeled as part of any investigation of a circuit's total insertion loss, but for now the effects of conductor and dielectric losses are the main concern.

Conductor losses are more dominant for circuits with less dielectric material; i.e., circuits fabricated on thinner substrates where the copper planes are not widely separated. For thicker dielectric substrates, in which the copper planes are farther apart, conductor losses are a smaller percentage of the insertion loss compared to the greater amount of dielectric material in a thicker substrate. **FIGURE 3** shows how the conductor losses for a microstrip circuit decrease (compared to dielectric losses) as the dielectric substrate thickness increases.

Insertion loss testing in Figure 3 was performed on 50Ω microstrip transmission-line circuits using the same copper-clad laminates for identical circuits but with different dielectric substrate thicknesses. Test results are compared with modeled data[1] that predict the total insertion loss and the contributions of conductor and dielectric losses to the total insertion loss.

Figure 3 shows how conductor losses increase for thinner circuit substrates of the same dielectric material. The roughness of the copper at the interface of the dielectric substrate and the copper also plays a role in conductor loss, with a rougher copper surface yielding increased conductor loss compared to a smoother copper surface. Rougher copper conductor surfaces will also slow the EM wave propagation of high-frequency circuits such as microstrip and increase the phase angle of propagating EM waves as if the Dk of the substrate material is higher than its nominal value.

When a thin substrate is needed for a high-frequency design and low insertion loss is also a key requirement, the type of copper is an important consideration. Smoother copper will yield high-frequency circuits with lower insertion loss. For example, in Figure 3 high-profile electrodeposited (ED) copper was used for the conductors and ground planes. This type of copper contributes high conductor loss to the overall insertion loss of a circuit. Conductor loss can be reduced by using a circuit material with smoother copper. Similarly, insertion loss can be reduced by controlling dielectric losses. A thinner substrate will result in dielectric loss being a smaller percentage of a circuit's total insertion loss; selecting a substrate material with lower dissipation factor (Df), a material loss parameter, can also contribute to lowering a circuit's overall insertion loss. For example, the results shown in Figure 3 were achieved using a substrate with Df of 0.0037; dielectric loss (and insertion loss) is less using a substrate with Df of 0.0010.

Precise about Phase

Phase is a critical electrical parameter in many high-frequency circuits, especially in many emerging mmWave applications such as automotive radars and 5G wireless networks, where phase is the basis for many advanced modulation formats. High-frequency circuits must maintain consistent phase response so systems such as radars and wireless communications provide reliable information. A high-frequency circuit's phase response is usually characterized in terms of phase angle or phase velocity. For example, a circuit processing an ideal sine wave would have a 360° phase angle response. **FIGURE 4** shows the phase angle response for a reference microstrip circuit and several variations, with the reference designed to provide a 360° phase angle response, or physical

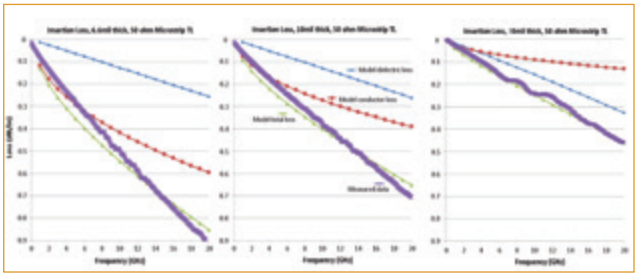

FIGURE 3. Conductor losses contribute less to the total insertion loss of a microstrip circuit for thicker dielectric circuit materials.

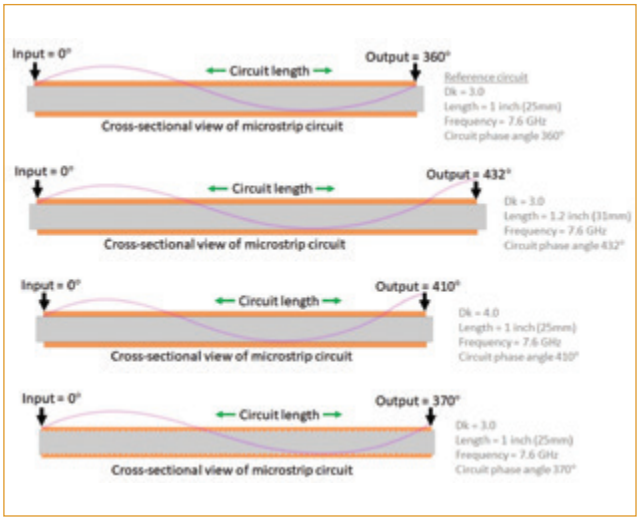

FIGURE 4. The reference microstrip circuit design (top) has a phase angle response of 360° or one wavelength at 7.6GHz. Changes in circuit length and substrate characteristics result in changes in phase angle response.

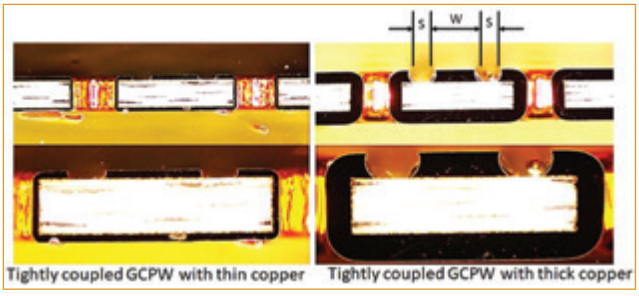

FIGURE 5. These micro-section images illustrate tightly coupled GCPW circuits with thin (left) and thick (right) copper plating on a circuit.

length equal to one wavelength, at 7.6GHz for a particular type of circuit material (with Dk of 3.0).

As Figure 4 illustrates, phase angle response can be affected by small changes in circuit design and circuit material characteristics. The microstrip reference circuit is designed with a physical length of 1" (25.4mm) for a phase angle response of one wavelength or 360° at 7.6GHz. Since wavelength decreases with increasing frequency, the same reference circuit has a phase angle response of two wavelengths or 720° at twice the frequency (15.2GHz). For two wavelengths at 7.6GHz, the reference circuit requires a physical length of 2" (50.8mm).

High-frequency circuit design is often based on supporting specific frequency bands and ranges, such as for communications channels, and the physical features of a circuit are very wavelength-specific, even involving the use of circuit features with fractional wavelengths such as quarter- and half-wavelength features. Given that one wavelength for the reference circuit in Figure 4 is 1" at 7.6GHz, and that wavelength decreases with increasing frequency, it is easy to see how circuit dimensions can become almost microscopic for circuits at mmWave frequencies.

Various circuit material parameters can impact a circuit's phase angle response, such as Dk and copper roughness. For example, for a 1" microstrip circuit fabricated on a substrate with Dk = 4.0 (the third circuit in Figure 4), the phase response increases to 410° at 7.6GHz. Similarly, the phase response decreases in wavelength with decreasing circuit material Dk value. Compared to smooth, low-profile copper, rougher copper results in slower wave velocity and an increase in the phase angle response (as the bottom circuit in Figure 4 approximates).

For mmWave circuits based on phase responses to function properly, the phase angle consistency is a key performance parameter. While a 1" microstrip circuit may exhibit a phase angle response of 360° at 7.6GHz, a microstrip circuit with that physical length on a substrate material with Dk = 3.0

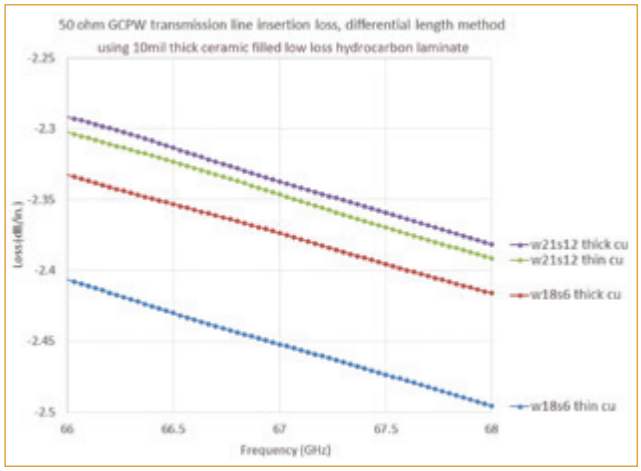

FIGURE 6. Insertion loss comparisons of circuits built on the same sheet of material, but with thin and thick copper and loosely coupled (w21s12) and tightly coupled (w18s6) GCPW circuits.

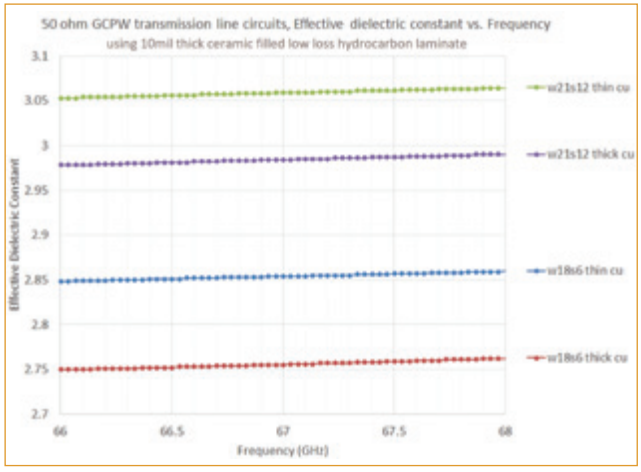

FIGURE 7. The effective Dk values are compared here for circuits built on the same sheet of material, but with thin and thick copper and tightly coupled (w18s6) compared to loosely coupled (w21s12) GCPW circuits.

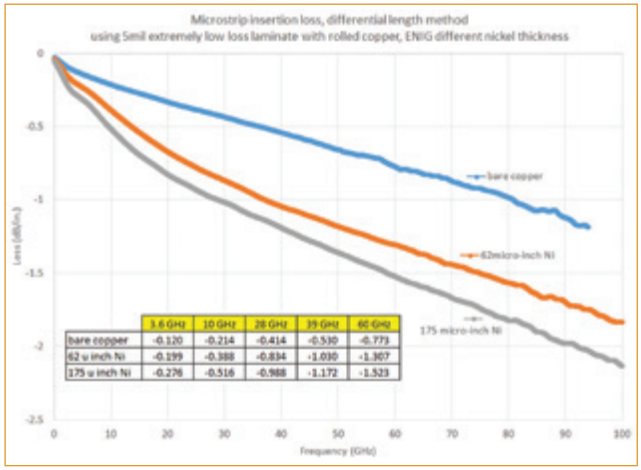

FIGURE 8. The insertion loss of microstrip transmission-line circuits was compared through mmWave frequencies with different Ni plating thicknesses, using bare copper circuits as reference.

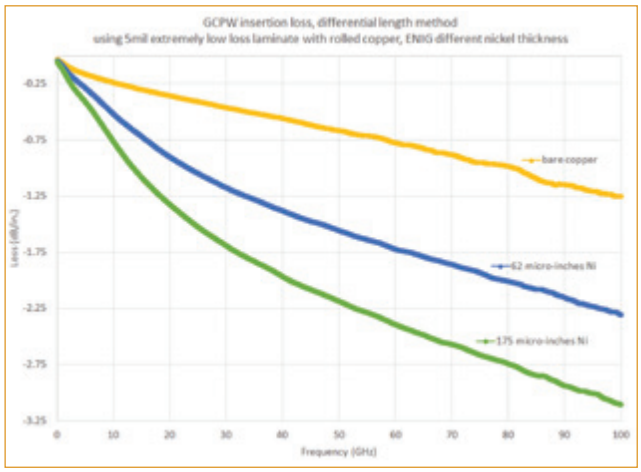

FIGURE 9. The insertion loss of GCPW transmission-line circuits was compared through mmWave frequencies with different Ni plating thicknesses, using bare copper circuits as reference.

may have a phase angle response of greater than 4,000° for a 77GHz radar, and phase angle variations of as little as ±30° can result in errors in radar detection (such as in automotive collision-avoidance systems). For mmWave circuits at lower frequencies, such as the 26GHz and 28GHz frequency bands used in 5G NR systems, phase response is also important for maintaining accuracy in phase-modulated networks, but with the lower frequencies and longer wavelengths, those circuits are less sensitive to variations in phase angle.

Designing PCBs for mmWaves

Many variables affect the performance of a PCB at the small wavelengths of mmWave frequencies, starting with how high-frequency signals are launched onto the PCB from a connector interface. An impedance anomaly generally exists at that interface, and a variation in impedance can cause signal reflections, elevated return loss and distortion. The junction of a high-frequency connector to the PCB may be an extremely short distance, and the impedance anomaly may only affect a physical distance of about 0.1" (2.54mm), but that length can equal a significant fraction of the wavelength at mmWave frequencies and can cause distortion of the wave. For example, at 40GHz, the wavelength is 0.18" (0.46mm). Such an impedance anomaly is less of a concern at lower frequencies where the wavelengths are much longer and less affected over that short distance.

Impedance anomalies at fractional wavelengths can impact mmWave circuit performance. How much is too much? An impedance anomaly of one-half wavelength will typically impact wave performance. A one-quarter-wavelength anomaly may also wreak havoc on mmWave circuit performance, but not as much as the one-half-wavelength anomaly. Generally, impedance anomalies of one-eighth wavelength or longer will influence wave behavior, and anomalies should be kept to one-tenth wavelength or shorter to minimize circuit performance problems at mmWave frequencies.

Ensuring circuit features such as substrate thickness and conductor width are less than one-tenth wavelength at a frequency of interest can prevent performance problems, such as unwanted resonances, at mmWave frequencies. For example, a mmWave circuit fabricated on a circuit substrate with one-half-wavelength thickness at the operating frequency will exhibit resonant conditions between the signal plane and the ground plane due to the thickness of the substrate. A conductor width equal to one-half wavelength at the operating frequency will also cause resonant conditions across the width of the circuit's conductors. By keeping the substrate thickness and conductor widths at one-tenth wavelength or less of the operating frequency, unwanted resonant conditions can be avoided.

Proper PCB Fabrication

The fine dimensions of mmWave circuits require well-controlled PCB fabrication processes to achieve circuits with repeatable, high-quality performance. Variations in copper plating thickness and the final plated-finish placed on copper surfaces can impact the performance of a mmWave circuit, and both processes must be tightly controlled for success with mmWave circuit fabrication. For laminated circuit materials, variations in the thickness of the raw copper on the laminates are typically held to a tolerance of ±10%. But for circuits using plated through-hole (PTH) technology for circuit interconnections, the base copper on a laminate will be thicker in support of the PTH process. The copper plating process yields normal variations related to circuit design and the type of fabrication process. Copper is typically plated thinner in the middle of a processed circuit panel and thicker closer to the edges of the panel, but such variations in copper thickness can be a source of performance variations at mmWave frequencies. For mmWave circuits manufactured in large volumes, for example, variations in copper thickness can result in circuit-to-circuit variations in insertion loss and phase response. GCPW circuits and most circuits with coupled circuit features can be affected by the circuit material's variations in copper thickness.

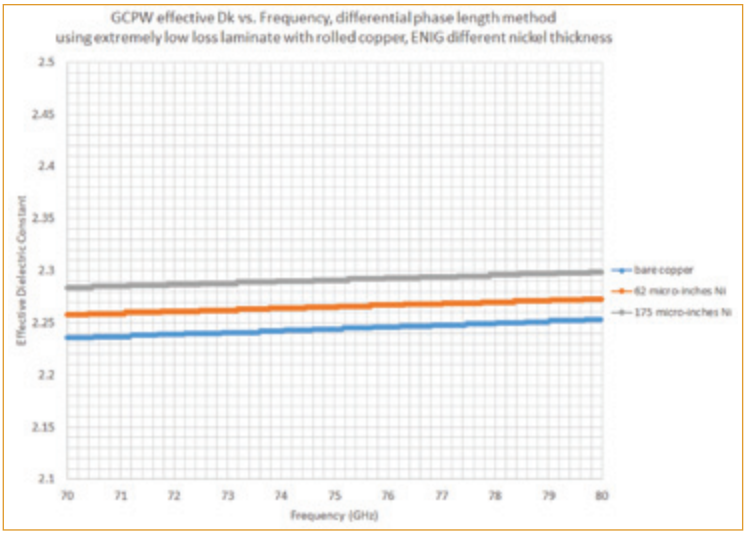

FIGURE 10. With a bare copper circuit as a reference, the effects of ENIG with different nickel-plated thicknesses on the effective Dk of GCPW transmission-line circuits were mapped from 70 to 80GHz.

A study[2] performed years ago based on 10 mil-thick hydrocarbon-based circuit material evaluated several circuits with different copper thicknesses that were fabricated on the same sheet of material to minimize dielectric material variations. Starting with a 24 x 18" (610 × 457mm) panel of circuit material, it was cut in half, and the halves of circuit material were processed with thin and thick copper plating. Each half panel had the same circuits fabricated on them, consisting of microstrip, tightly coupled GCPW, and loosely coupled GCPW transmission-line circuits. The circuits with thinner copper plating had total conductor thickness of 1 mil, while the circuits with thicker copper plating had total conductor thickness of 3 mils. A 3 mil difference in copper thickness that occurs in even a small percentage of millions of circuits as part of a high-volume manufacturing process can be costly.

Among the different circuits fabricated on these panels, single-ended microstrip transmission-line circuits showed little difference between circuits with thin and thick copper. The circuits with thicker copper had slightly lower insertion loss and lower effective Dk than the same type of circuits fabricated with thinner copper. The thicker copper conductors produced more fringing E fields in the air, with its low Dk, causing the effective Dk to drop and insertion loss to decrease. But at mmWave frequencies, microstrip transmission-line circuits with thicker copper can experience a greater number of wave interference problems than microstrip with thinner copper, due to the increase in surface waves with thicker conductors at such small wavelengths.

In contrast, tightly coupled, single-ended GCPW transmission-line circuits revealed significant differences (**FIGURE 5**); loosely coupled, single-ended GCPW transmission-line circuits were also evaluated in the study, but the results are not shown here. The circuits were named according to a convention that lists signal conductor width (w) and space (s) between conductors and neighboring ground planes, such as w18s6 for a tightly coupled circuit with signal conductor width of 18 mils and coplanar spacing of 6 mils. A loosely coupled circuit, as an example, had dimensions according to w21s10.

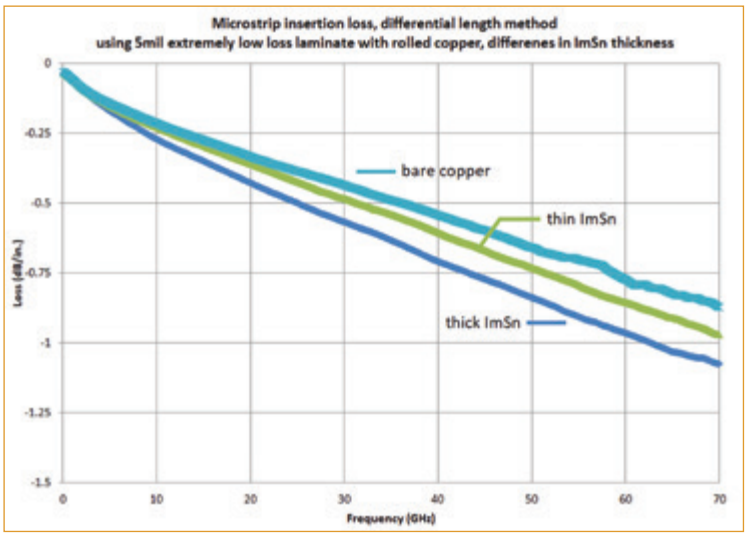

FIGURE 11. Microstrip circuits were evaluated across a wide frequency range to compare the effects of different thicknesses of ImSn plated finishes on rolled copper using a low loss, 5mil circuit material.

In addition to GCPW circuits with thicker copper conductors having more E fields in the air than GCPW circuits with thinner copper conductors, the thicker copper results in conductors with more of a trapezoidal shape than thinner copper with conductors that have more of a rectangular shape. The differences in conductor shapes impact the behavior of the E fields and affect mmWave performance according to the copper conductor thickness.

FIGURE 6 offers a comparison of insertion loss for tightly coupled and loosely coupled GCPW transmission-line circuits with thin and thick copper conductors. The GCPW circuit with conductor width of 21 mils and spacing of 12 mils (w21s12) with thick copper had the lowest insertion loss due to having more E fields in air with its low Dk value and having a wider signal conductor with reduced conductor loss. The GCPW circuit with 18 mil conductor width and 6 mil spacing (w18s6) on thin copper had the highest insertion loss because of having the lowest percentage of E fields in the air and a narrower signal conductor with its increased conductor loss. The frequency range (66GHz to 68GHz) chosen for evaluation was a band where all circuits had return loss of better than 15dB.

The circuits were also evaluated for phase response, with phase angles measured at different frequencies. The effective Dk of each circuit was determined by the differential phase-length method, where a known difference in the physical length of a transmission line corresponds to a known difference in phase angle. In this test method, phase angles are measured for two circuits built side-by-side on the same circuit material panel, with the circuits identical except for transmission lines with different physical lengths. The effective Dk is determined by a simple formula that relates the difference in measured phase angle to the difference in physical length.

FIGURE 7 shows the GCPW circuits with the lowest effective Dk are those with 18 mil-wide conductors and 6 mil spacing (w18s6) with thick copper. With their tight coupling, these circuits have increased E fields in the coupled areas (and in air). The thick copper contributes to tall, coupled conductor sidewalls with more E fields in air. The GCPW circuits with the highest effective Dk are those with 21 mil conductor widths and 12 mil spacing (w21s12) with thin copper, since fewer E fields are in air (with their low Dk value).

Because many mmWave circuits, such as 5G NR small cells and radar systems, rely on maintaining consistent and precise phase responses, phase-angle response deviations must be held within acceptable limits according to frequency and to the requirements of an application. For 77GHz radars, for example, circuits may have total phase lengths of thousands of degrees, so a phase deviation window of 50° (or ±25°) may be acceptable. Depending on design requirements and frequencies, some radar systems may operate acceptably with even larger phase deviations, while some may require a phase deviation window as tight as ±10°. Designers and fabricators of PCBs for these applications should keep in mind how circuit material characteristics and PCB production techniques can impact the phase response of a circuit, especially at the small wavelengths of mmWave frequencies. For example, the difference in effective Dk of 0.1 shown in Figure 7 translates to an approximate phase angle difference of 60° in the 67GHz band. This much of a phase angle difference is attributed to variations in circuit copper thickness alone, with many other variables, including dielectric material thickness variations, Dk variations, and even the type of final plated finish of the copper, affecting the phase angle response. Since copper thickness variations can significantly impact coupled circuits such as GCPW, other circuit configurations, such as microstrip, which are less affected by copper thickness variations, are typi-

cally used at mmWave frequencies.

The final plated finish applied to a circuit's copper is usually evaluated in terms of its effect on insertion loss. But at mmWave frequencies, plated finish can also play a role in a circuit's phase angle response. Generally, the effect of plated finish on performance will depend on the type of circuit, such as single-ended or coupled circuits, and the influence of skin depth at different operating frequencies.

FIGURE 8 shows how plated finish can make a difference in the insertion-loss performance of microstrip transmission-line circuits. It compares loss for circuits with rolled copper and different thicknesses of nickel (Ni) plating, using electroless nickel immersion gold (ENIG) plating. The ENIG process normally undergoes some amount of nickel thickness variations, and those variations can impact the insertion loss and phase response of high-frequency circuits at mmWave frequencies.

The high-frequency circuits in Figure 8 exhibit the edge effects of each final plated finish. Microstrip circuits have high concentrations of RF current and E fields on the left and right edges of their signal conductors. When the edges of the conductors of a high-frequency circuit are coated with a metal finish that is not as conductive as copper, the conductor losses will increase, adding to the overall insertion loss of the circuit. In a GCPW circuit, however, with a conductor structure consisting of four edges, the effects of a plated finish that is not as conductive as copper will be much greater than in a microstrip circuit with two conductor edges. **FIGURE 9** shows test results for tightly coupled GCPW circuits and how they are more significantly impacted by plated finish than the microstrip circuits of Figure 8.

Reference circuits in Figures 8 and 9 use bare copper without plated finishes for comparison to the circuits with plated finishes. Often, circuit designers will perform simulations on circuits using a material with specific characteristics, such as its values of Dk and Df, but will not include the effects of a plated finish on their modeled circuits. Those plated finish effects may be difficult to model, but they can affect the performance of both microstrip and GCPW circuits, with increased insertion loss at mmWave frequencies.

FIGURE 10 shows how PCB plated finishes affect the effective Dk, and thus the phase angle response, of tightly coupled GCPW circuits from 70 to 80GHz. Circuits with thin and thick Ni plating exhibit a difference of about 0.02 in effective Dk. The larger difference in effective Dk for tightly coupled GCPW circuits with plating thickness difference compared to microstrip circuits means those circuits will experience greater deviations in phase angle response as a function of plating thickness variations compared to microstrip circuits. A 0.02 difference in effective Dk translates to a phase angle difference of about 60° from 70 to 80GHz. Such large phase angle response deviations can be significant for many mmWave applications requiring consistent phase performance, including radar systems and 5G NR cellular wireless networks.

To minimize the insertion loss of the plating finish at higher frequencies, most mmWave circuits avoid the use of ENIG finish. The variations in Ni-plated thickness of ENIG finishes can also cause excessive variations in phase angle response. As low-loss alternatives, immersion tin (ImSn) and immersion silver (ImAg) plated finishes are more commonly used for mmWave PCBs. In addition, some organic solderability preservative (OSP) finishes with low loss and long shelf lives are used for circuits at mmWave frequencies. ImSn finishes will add some insertion loss and small variations in phase angle response to a mmWave circuit, but because they are so thin, the thickness variations are minimal compared to ENIG finishes, with little effect on the insertion loss and phase response of a mmWave circuit.

Data shown in **FIGURE 11** extend from DC to 70GHz, although data were collected through 110GHz. Data for those higher frequencies were not plotted because of the poor return loss for the test circuits above 70GHz. The high return loss can degrade the accuracy of insertion-loss measurements, so only the results to 70GHz are shown. At 70GHz, the difference in insertion loss between microstrip circuits with thin and thick ImSn plating finish is about 0.12dB/in., which is considerably less than the difference of 0.25dB/in. at 70GHz for the ENIG thickness variations shown in Figure 8 for microstrip test circuits. Although not shown, the difference in ImSn plating difference for microstrip circuits at 70GHz translates to a phase angle difference of slightly less than 3° at 70GHz.

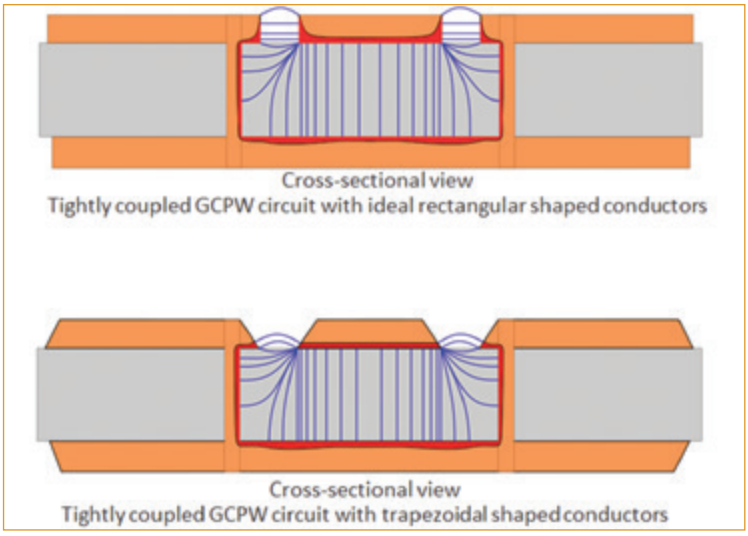

FIGURE 12. These cross-section views show how differences in GCPW conductor shapes can affect a circuit's E field patterns, with rectangular-shaped conductors in the top view and trapezoidal-shaped conductors in the bottom view.

Staying in Shape

Due to the small features of mmWave circuits, circuit etching must be accurate and repeatable. For example, conductors should be formed with ideal rectangular shapes, and trapezoidal conductor shapes should be minimized not only for coupled circuitry such as GCPW but in microstrip circuits as well. Conductor shape variations will have more impact at higher frequencies, with trapezoidal-shaped conductors altering circuit performance at 77GHz, but have little effect on

circuits operating at 24GHz. Most circuits designed for 77GHz are based on the use of thinner circuit laminates, such as 4 or 5 mils in thickness, to avoid unwanted resonances. Thinner substrates will use narrower signal conductors than thicker circuit materials, and trapezoidal shapes will have more impact on narrower conductors compared to wider conductors. At lower frequencies, such as 24GHz, thicker laminates are typically used. They have wider conductors in which trapezoidal conductor shapes have less impact on high-frequency performance.

For large-volume production, variations in trapezoidal-shaped conductors can cause variations in the performance of GCPW circuits but also affect microstrip circuits due to circuit-to-circuit variations in the fringing fields. As more or less of the fringing fields propagate in air, the low Dk of air alters the effective Dk of each circuit. Signal conductors with more pronounced trapezoidal shapes will have less E fields in air, resulting in less lowering of the effective Dk due to the low Dk of air compared to more ideal rectangular-shaped conductors with more of the E fields in air. The circuit-to-circuit variations in conductor shapes are exhibited as variations in phase angle response, which will impact the performance of phase-sensitive circuits at mmWave frequencies, particularly more for coupled circuits such as GCPW than microstrip circuits **(FIGURE 12)**.

Conductors are often produced with trapezoidal shapes due to thick copper or a fast-etching process in which an insufficient amount of copper is etched away to form the more ideal rectangular conductor shape. The fast-etching processes typically used in high-volume PCB manufacturing can leave behind copper dendrites on the left and right edges of a high-frequency conductor, and these added copper flakes can cause phase distortion in microstrip and GCPW circuits. Conductors that are more rectangular-shaped (with less circuit-to-circuit phase angle response variations in high-volume production) than trapezoidal-shaped can be produced using thinner copper and better controlled (although typically slower) copper etching processes.

Solder mask used in the production of PCBs can raise the insertion loss and phase deviations of high-frequency circuits and must be removed, especially from mmWave circuits. Liquid photoimageable (LPI) solder mask is typically used in manufacturing high-frequency microstrip and GCPW PCBs. If not removed from the conductors of a microstrip circuit, for example, the E fields normally in air will be in the solder mask with its higher loss and Dk than air, resulting in increased insertion loss and phase angle for that circuit. For coupled circuits such as GCPW, solder mask on the conductors will cause even greater degradation of insertion loss and phase angle response.

Depending on wavelength, it may be possible to use small amounts of solder mask, such as for solder damming, without significantly degrading the performance of a mmWave circuit. As in the case of circuits with impedance anomalies, the solder mask does not affect a portion of the circuit that is more than one-tenth wavelength at the operating frequency. For a 77GHz circuit, one-tenth wavelength is about 10 mils. At lower frequencies, a solder mask patch can have a much greater length without having deleterious effects on circuit performance. For example, at 24GHz, one-tenth wavelength is about 33 mils, and a solder mask patch with that physical length will not pose resonant conditions or significantly affect the circuit's wave properties.

The copper surface roughness at the substrate-copper interface has an impact on PCB phase response at mmWave frequencies. Unfortunately, copper foils used in PCB manufacturing will exhibit a certain amount of roughness, with variations in the amount of copper roughness from sheet to sheet and even within the same sheet. For example, ED copper with an average copper surface roughness of 2µm RMS (also known as Rq or Sq) may have a copper surface roughness that varies from 1.7 to 2.3µm. Circuits produced with that range of copper surface roughness will exhibit significant variations in phase angle response and insertion-loss performance, especially at mmWave frequencies.

The copper may be part of the laminate manufactured by a circuit material supplier, or a foil is used by a PCB fabricator to build a PCB. Generally, copper with a smooth surface will have fewer variations in surface roughness and will yield fewer variations in phase response than copper with a rougher surface. Rolled copper is a type of copper with little variation in surface roughness (and phase response), with average surface roughness of 0.35µm RMS (compared to the average surface roughness of 2µm RMS for ED copper). It is extremely smooth with very low conductor loss, contributing to circuits with less insertion loss than those with ED copper.

In general, mmWave PCBs rely on precise fabrication of circuit features and positioning of components due to the small wavelengths and how physical size variations translate into phase variations over the nominal mmWave frequency range of 30 to 300GHz. A growing number of applications will rely on mmWave signals and PCBs, from autonomous vehicle radars to 5G wireless networks, and phase accuracy is essential for those applications whether for radar target detection (for collision avoidance) or for phase-modulated communications.

The phase performance of a PCB can be affected by many design and fabrication variables, including substrate Dk variations, copper surface roughness variations, substrate thickness variations, copper plating thickness variations, final plated finish variations, etching consistency, conductor trapezoidal shape variations, the moisture absorption properties of the circuit material, and the circuit material's thermal coefficient of Dk (TCDk). For GCPW circuits, variations in the locations of PTHs that connect top and bottom ground planes can cause variations in mmWave phase response. The consistency of lead-free solder-reflow processes and the choice of final plated finish can also affect the phase performance and loss performance consistency of PCBs when they are intended for mmWave frequency ranges, which many applications in need of additional frequency bandwidth will reach. ▫

REFERENCES

1. Circuit simulations were used to compare test results in Figure 3 for different components of microstrip insertion loss for thin and thick circuits at microwave frequencies.
2. Rogers Corp. study shows copper thickness variations for GCPW circuits based on 10-mil-thick RO4350B circuit material.

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US DEFENSE SUPPLIERS Have Begged for Help. A Pandemic Helped Them Get It

How a new trade group is aiding the DoD's desire for a trusted supply chain. **by MIKE BUETOW**

For decades the printed circuit industry has asserted the lack of government support has a deleterious effect on the supply chain's ability to properly supply the US military. Attempts to correct this over the years have been numerous but largely unsuccessful.

Led by IPC, industry has lobbied the US Congress since the early 1990s to reduce barriers to winning military contracts, and, as margins were slashed beginning in the early 2000s, to fund research and development that could be shared among Defense Department suppliers to help their competitiveness.

IPC, for its part, has threaded the needle in terms of trying to support its domestic constituents and meet the needs of the DoD while not alienating other members that are foreign-based. It has provided support and advocacy to the Executive Agent for Printed Circuit Boards and Interconnect Technology, a position funded by Congress in the annual National Defense Authorization Act and assigned to the Navy. The EA's role is to help the DoD access reliable, trusted and affordable PCB fabrication and assembly products, and facilitate R&D collaboration. In practice, it's a politically intense position that comes with unwritten but very real limits on how hard the EA can push for funding and priorities. The results are clear: The US industry remains behind several geographical competitors in terms of capabilities and capacity. Moreover, as new edicts were handed down to promote greater security of IP, smaller companies, especially fabricators, have found it financially treacherous to remain on the DoD's acquisition list.

One of the barriers to breach was the way the US Congress views the domestic industry. As John Mitchell, CEO of IPC, explains, "The vast portion of the Hill views electronics as semiconductors and software. We spend a lot of time explaining that they have to put the chip on something."

After years of observing well-intentioned but ultimately futile attempts to rebalance the industry, IPC launched a nonprofit subsidiary that would enable the organization to separate its domestic and international interests and placate DoD concerns over funding research that might end up in offshore hands.

The result, the US Partnership for Assured Electronics, was formed in February 2020. The organization is made up of fabricators and assemblers, suppliers of materials and other "unique" technology, and academia, according to executive director Chris Peters **(FIGURE 1)**. Membership recruitment, aided in part by Matt Turpin, a former EMS executive, has a target of 170 members by year end, which USPAE expects to reach with ease.

The Impact of Covid-19

As many predicted, it would take a crisis to get the attention of Congress. That crisis came in the form of a pandemic: Covid-19. "The shortage of ventilators brought it laser-focused that it isn't well understood [to Congress]," Mitchell said.

FIGURE 1. Chris Peters, executive director of USPAE.

Adds Peters: "Covid was a clear catalyst. The US couldn't get enough PCBs to ramp up production of ventilators because the PCBs came from China. There's much higher awareness now of this reliance on foreign sources. Our focus in the past year was to open the aperture, to get government to consider the entire electronics supply chain, which includes PCBs, semiconductors, components, wire and cable and assembly. We have seen a lot of attention on the semiconductor industry, but we must address all segments of the electronics industry."

Peters came to electronics after 15 years focused on advanced manufacturing supply chains for the DoD. His manufacturing experience has largely focused on metals – machining, castings, forgings and so on. His work for the DoD focused on how to improve and strengthen the defense industrial base, with special attention paid to small- to medium-sized businesses (SMBs).

That segment is where great ideas are born but too often die, Peters suggests. "That's where a lot of the innovation happens and a lot of opportunities are, but we also have a lot of challenges. The US DoD places a lot of burdens on those companies, and it's hard for them to bear those burdens. I want to make sure government is aware of those challenges and how they affect the electronics industry."

With Covid the catalyst and the USPAE the receptacle, Congress is at long last ready to act. In late January, it announced the founding of the Defense Electronics Consortium and awarded $42.3 million to the USPAE to manage it. The consortium will manage a number of programs in concert with industry and academia designed to solve the government's electronics-related challenges.

The first of those is the lead-free defense initiative, which Congress allocated $3.9 million for the first year and will appropriate another $10 million for the second year. This is an effort to accelerate adoption of Pb-free electronics in defense systems. Four universities and eight major companies are involved, says Peters, with Purdue, the University of Maryland and Auburn leading the way.

FIGURE 2. The USPAE aims to match US electronics innovation with Defense Department needs.

Asked how DEC ensures the work performed at university labs matches real-world conditions, Peters says, "The way you make sure is to include industry in the project: BAE, L3 Harris, Plexus, Northrup Grumman, Lockheed, Boeing, and others are all involved. That's how you make sure you balance academia and industry."

Moving forward, the participants will vary by project, with work performed at industry facilities or federal labs.

Just what direction the next programs take is being rounded out. In January the Office of Industrial Policy in the Pentagon issued the 2020 *Industrial Capabilities Report to Congress*[1] (https://media.defense.gov/2021/jan/14/2002565311/-1/-1/0/fy20-industrial-capabilities-report.pdf). Five pages are dedicated to electronics, including PCBs and assemblies, with a matrix of needs **(FIGURE 3)**. "That's good insight into what DoD is thinking in terms of what they need," Peters said.

Peters shared that USPAE anticipates taking on technical roadmap activity. "That's one of the tasks in the DEC award. The EA does some of that roadmapping, and we'll collaborate with them.

"The US electronics industry has to be more globally competitive, so it is ready to respond to the needs of the DoD when they are needed. We may not be able to compete with Foxconn (in size). But you think about commercial markets and automotive that are high-volume, low-mix, with lots of automation and productivity. Defense/aerospace is low-volume, high-mix. It's not as efficient because we are changing materials and equipment. We are going to look at some of those areas: How can we bring some of those efficiencies to LVHM, so we can reduce those high costs of changing materials and equipment to produce LVHM as efficiently as HVLM?"

Given the EA is tied to the US Naval Warfare Center in Crane, Indiana, and Crane also seeks government funding for PCB-related research, does this pose a duplication of effort, or even a national competitor for scarce resources? Peters says no. "I have weekly conversations with the PrCB Executive Agent's office. We look at this as a partnership between industry and government, and we support their efforts where we can. The PrCB Executive Agent is the technical lead for the lead-free project, so that relationship will grow stronger. There may be an opportunity to use Crane's resources for some of the work we've talked about."

Contrary Opinions

Past efforts to gain Congress's attention have shown fleeting results. Scores of executives have walked the halls of the House and Senate buildings to press their case. They cheered when, after repeated attempts, the House passed a resolution in the early 2000s in support of the American PCB industry. No money followed, however, and a few years later, industry representatives testified on Capitol Hill that the domestic industry was in the throes of a collapse.

Even of late, there have been detractors. Fears over changes to the supply chain have led some formidable nongovernment organizations to contest many DoD proposals. The Acquisition Reform Working Group, a body made up of the Associated General Contractors of America, the Information Technology Industry Council, the Computing Technology Industry Association, the National Defense Industrial Association, the American Council of Engineering Companies and the US Chamber of Commerce, contends that domestic bills that limit purchases of PCBs from non-allied sources such as China are unnecessary. In a letter to Congress last fall, ARWG recommended Congress order the Secretary of Defense to "implement a design verification standard to ensure [printed circuit boards] present no national security risk regarding counterfeiting, quality, or unauthorized access." In a separate letter, the Chamber said, "Congress should direct the Secretary of Defense to determine if PCB suppliers should either participate in a 'trusted supplier' program or adopt a design verification standard to ensure the integrity of PCBs in the supply chain." The Chamber notes key American industries rely on

Taiwan, South Korea, and other friendly nations that would be excluded as suppliers of circuit boards.

Still, the pressure to act has been received at the highest levels, starting with then-President Donald Trump's Executive Order in 2017, which forced a critical evaluation of the resiliency and capacity of the manufacturing and defense industrial base and supply chains. President Joe Biden, says Peters, is expected to go further, diving into critical raw materials whose continued supply is at risk due to pandemics or reliance on other nations.

Asked who the government champion is for the latest acquisition reform, Peters pointed to none other than the White House. "There are certainly champions throughout government, in the DoC, in the DoD, but they all have come to recognize the importance of electronics. This is particularly important for the DoD as the US enjoys an asymmetric warfare advantage because of our capability in electronics," he said. (As this article went to press, the White House indicated President Biden will sign an executive order requiring US government to produce unclassified assessments of key industries and their supply chains, including semiconductor manufacturing and rare earth minerals. An updated report for PCBs was not explicitly mentioned, but might not be needed.)

Technology	Copper Interconnect/ Solder Joint Advances, Ruggedization	Thermal Management Advances	Improved Size, Weight, Power/ Finer Circuit Traces/ Smaller Vias	New Materials	Business Impacts	Advances in PrCB and PrCB Manufacturing
Hypersonics	X			X		X
Directed Energy		X		X		X
Advanced Communications			X			X
Space Offense and Defense				X		X
Unmanned Aerial Systems/ Autonomy	X		X	X		X
Advanced Robotics/AI	X		X	X	X	X

FIGURE 3. The OIP's matrix of PCB needs by end-program.

The USPAE board is made up of Shane Whiteside, CEO of Summit Interconnect, ret. Adm. Kevin Sweeney, a former Pentagon chief of staff, and Mitchell. Turpin is a senior advisor.

While Mitchell says he plays an "active role" in USPAE, both he and Peters acknowledge the balancing act needed to keep the interests of IPC's members from bleeding over into USPAE. "We have firewalls that describe what info can and can't go between IPC and USPAE," Peters said. "Very little goes back to IPC, so we remain trusted and neutral."

"We are trying to help government understand that electronics is horizontal, not vertical," says Mitchell of the effort. "And here are the changes to the infrastructure you need if you want a robust industry."

The US model could be offshored as well. "When we proposed setting up USPAE," Mitchell said, "we brought it up to our board, which is global. We saw it as helping this industry, but we've also talked with the French government to see what we might do there. It's the kind of activity we would do anywhere."

The benefits of membership are hard and soft. Members gain participation in and access to cutting-edge research, funded by the DoD. And in some instances, especially for smaller businesses, they gain visibility and potential access to DoD contracts they might not otherwise be privy to.

IPC Firewall

To join USPAE, a company must be organized in the US, or in a qualifying country as set forth by the Defense Federal Acquisition Regulation Supplement (DFARS),[2] and agree to be certified to IPC-1791 within a year of joining. But, as Peters notes, "each DoD contract is different and might have tighter requirements for participation."

For its part, the DEC is less a company and more a "contract vehicle," says Peters.

"It's unique in that it doesn't follow the usual rules of the federal acquisition. It helps the DoD interact more easily with nontraditional manufacturers and SMEs that might otherwise have challenges meeting all the regulations.

"Most other transaction authority (OTA) agreements focus on research and prototypes," he continues. "Ours allows a project to move from prototype to production without having to go to recompete. So, if a company verifies a product's viability in a prototype, the government can order a production run without it having to go out for recompete. That's a huge advantage."

'Trusted and Assured'

At the top of the pyramid of data control is NIST SP 800-171, "Protecting Controlled Unclassified Information in Nonfederal Systems and Organizations." But for USPAE, the lynchpin is IPC-1791.[3] That's a standard published three years ago to address the electronics supply chain cybersecurity measures, plus physical security, anticounterfeiting, and supply chain management.

The *Industrial Capabilities Report* references the scope of IPC-1791 and notes the "B" revision will be expanded to complement Cybersecurity Maturity Model Certification requirements. Mere mention of CMMC sends shudders through entire SMBs. The Pentagon has imposed a host of cybersecurity standards, and industry, especially smaller companies, have found them painfully expensive to implement. And while the Office of the Under Secretary of Defense Acquisition & Sustainment estimated the costs at $3,000 – $5,000 for CMMC level one certification, SMBs and Peters told PCD&F/CIRCUITS ASSEMBLY the true costs are substantially more. While the DoD plans to issue contracts starting this year with CMMC

as a requirement, manufacturers we spoke to noted continued haggling over how the levels are defined (there are five), what the audit protocols will be, and who will conduct them.

For some, this comes after spending hundreds of thousands of dollars to gain and maintain NIST SP 800-171 compliance. But for those worried USPAE plans to pile on more cyber requirements, Turpin says that's not an issue. IPC-1791 incorporates the NIST SP 800-171 compliance requirements, but "it goes way above CMMC because it goes above cybersecurity, looking at supply chain, physical security, background checks, counterfeit mitigation, and other areas. It also applies to boards and EMS."

Peters agrees. "I've coauthored several papers on cybersecurity for manufacturing and have been focused on how CMMC implementation is placing an undue burden on SMBs," he says. "No one questions it is needed. Everyone knows the information must be protected. But when it begins to cost SMBs hundreds of thousands of dollars to comply, and thousands more to remain in compliance, that's a burden on the industrial base."

Referencing a comprehensive Department of Commerce survey from 2019,[4] Peters notes that of 145 US bare board fabricators that reported sales tied to defense end-use, 53% garner less than 25% of their revenue from military programs. "We already make it hard enough to work with the government. Additional burdens like CMMC increase the likelihood of companies abandoning defense work," he says.

"The information on CMMC has not been consistent, compounding the problem. Government needs to give industry greater clarity on what is CUI (controlled unclassified information), and industry needs greater confidence that if they spend money to comply, those solutions will be acceptable to auditors. Manufacturers have added complexities, like older and different operating systems on their plant floor, and they need greater clarity and better solutions."

Since IPC oversees and generates revenue from validation services for IPC-1791, some observers who requested their names be withheld because they do business with the DoD said the lobbying of Congress to extend "trusted supplier" requirements to PCBs and assemblies could be self-serving. Others noted that with no CMMC certification available, IPC-1791 is the only current option.

The drawback to joining USPAE might be the cost. Membership starts at $7,500 per year for companies under $100 million in annual revenues, climbing to $50,000 annually for the relative handful of $20 billion companies. (Startups less than two years old and nonprofits pay $500.) Given that about 70% of the remaining fabricators in the US already supply the Pentagon, and nearly 500 assembly companies are registered to do business with the government, access to the DoD spigot might not be enough incentive to join. And smaller firms generally don't have the luxury of staffing R&D groups. Instead, the value for them would be access to the research that comes out of DEC and like programs.

Peters is unbowed. "There is no obligation to participate in research. I've already heard from companies interested in joining just to network and explore commercial business opportunities," he told us. He adds that the new consortia allow the Pentagon access to the electronics industry at a level it is not accustomed to. "(T)he electronics industry … is often buried layers down in the supply chain. The DoD typically doesn't have insights into who those companies are or what those companies are doing. USPAE and the DEC helps bring them together." Doing so, he adds, will help the DoD gain knowledge of where the US is reliant on foreign sources.

Turpin, who knows the industry well, having spent 12 years as the head of the EMS firm Zentech, which derived more than half its sales from defense and aerospace, remains bullish on the potential.

"The explicit vision of the DoD and USPAE is that DEC will have many, many projects like the lead-free project running through it." The consortia, he says "give the DoD quick access to lots of companies that could help it on both large and small projects, and help educate the DoD on who is out there." ❑

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2021: Automation, Flexibility and the 'ELECTRONICS SUPERCYCLE'

One year in, Covid-19 has shifted priorities in the industry – or has it? **by CHELSEY DRYSDALE**

One year in, has Covid-19 shifted priorities in the industry? To find out, CIRCUITS ASSEMBLY reached out in January to experts for insights on how the pandemic has impacted everything from inside the factory to the business decisions we make. Then, for good measure, we asked how the semiconductor industry might change in the wake of Intel's proposed sale of some manufacturing assets, a move that could have lasting impacts on the IC. We spoke with a range of leaders covering various segments of the electronics manufacturing supply chain. Their responses, lightly edited for clarity and length, follow. After reading their thoughts, share your own on our LinkedIn page (https://www.linkedin.com/groups/2847418).

CA: In the wake of Covid-19, have factory qualification procedures changed? If so, how?

Ryan Hagemeier *(director quality and product regulatory assurance, Plexus):* Overall, audit/inspection criteria have not changed. However, regulatory authorities, notified bodies and even our customers have had to modify their approach given the current limitations for traditional onsite inspections, including: extending certifications to allow revised audit scheduling, performing remote audits/inspections, and leveraging other regulatory authority inspection/documentation history to focus on performing higher-risk inspections in the short term.

Phil Zarrow *(president and principal consultant, ITM Consulting):* One interesting challenge we undertook during the current pandemic was validating no-clean processes at several CEMs. One particular client is a manufacturer of mission-critical medical equipment that is vital for life-support, especially for people with Covid.

The client had several CMs geographically scattered. While that geo-diversity turned out to be helpful to mitigate Covid risk, it was more challenging when it came time for new process qualification. We found out because a quality risk was identified, and the only way to confirm the elimination of that risk was a wholesale change in soldering technology. But how to qualify and validate the new soldering technology processes expeditiously and comprehensively at five different CEMs in the time of Covid?

The answer took a lot of thought by a broad team of technical experts, not to mention a few plant safety folks. It was decided, in light of cleanliness testing standards directions on IPC standards, dynamic SIR testing would be the most efficient and reliable means of determining acceptability of the assembled PCBAs. It was important all PCBAs assembled with the new soldering process meet IPC J-STD-001G, Amendment 1, Section 8.

A cross-functional team, including the OEM, CMs, yours truly and other outside experts, created a validation program on dynamic SIR testing. The validation process was pretty straightforward.

Initially, test coupons for both SMT and through-hole, based on the IPC-B-24 and IPC-B-52 coupons, were supplied to the CEMs, along with appropriate components. The CEMs assembled the test coupon PCBAs with the same materials, equipment and techniques with which they would be assembling the client's boards. Note: Due to the nature of the client's components, this new soldering process would be without cleaning. With the exception of test coupons designated for touch-up testing, no rework was allowed.

The assembled and no-clean-soldered test coupons were sent to an outside lab for dynamic SIR testing using standard IPC protocols: 90% RH at 40°C with a pulsed bias voltage of 5 VDC for a period from one to 168 hrs. The status of SIR under components is monitored and tracked in real time during this interval, with unacceptable results reported mid-test when encountered. This type of dynamic SIR testing is essentially HALT of the residue with regard to SIR. The goal is to determine whether a stable process from board-to-board has been attained by the assembler and that there is no parasitic leakage when the PCBA is exposed to hot, humid conditions. Acceptable passing-grade values were sustaining a level above Log 8 on each of the test coupons submitted.

Beyond initial validation of the CEMs' new soldering

processes, the plan includes ongoing testing to allow the OEM to monitor incoming PCBAs by in-house testing on a lot basis. This process control program will utilize test coupons incorporated into unused areas of the actual product PCBAs. These test coupons will be populated and tested by the OEM at incoming QA. Going forward, several of the CEMs are considering acquiring in-house testing capability as well.

In this instance, the Covid situation, with extreme travel restrictions and greatly increased demand for a product, was a catalyst for the direction for validating a new soldering process for an existing production PCB assembly. However, in light of IPC compliance requirements, this validation procedure and methodology appears to be a best practice going forward, including "normal" times.

CA: Do you expect M&A activity in the electronics manufacturing sector to increase or decrease year-over-year in 2021? Why?

Tom Kastner *(president, GP Ventures):* I expect M&A activity in the EMS sector to increase in 2021 due to 1) a large number of interested buyers, especially private equity-backed strategic buyers (HIG's take-private transaction with SMTC will free them up to do more acquisitions, for example), 2) low interest rates, 3) a gradual reduction in market uncertainty due to the rollout of Covid-19 vaccines and the US presidential elections being in the rearview mirror, 4) a large number of EMS owners who are of retirement age, 5) more distressed companies coming to market after their PPP loans run out, and 6) a resurgence in manufacturing due to a strong US military budget, an improving economy, and reshoring.

Jack Calderon *(managing director, Lincoln International):* The M&A market for electronics manufacturing has picked up during Covid and should continue for several reasons. First, more investors are becoming aware of the emergence of Supercycle 2.0, which started in 2016. A Supercycle occurs when technology rapidly transforms all facets of life, whether in the home, car, factory, warehouse or office. Supercycle 1.0 occurred with the commercialization of the microprocessor, which lasted from 1979 to 2001. During that two-decades period, every facet of life was transformed into the digital age (Supercycle 1.0). Supercycle 2.0 is being driven with every device being smart, connected, data-producing, and the AI to apply that data in transformative ways. Like the first Supercycle, the EMS industry stands to be a big beneficiary of this new cycle of product innovation. This has brought heightened private equity interest into the sector. Private equity investments in the past 24 months have exceeded the number in the 10 preceding years. And as private equity acquires a platform,

they will look to accelerate the growth of those platforms into larger operating entities, thus driving further consolidations. In addition to the emergence of Supercycle 2.0, the EMS industry proved essential during Covid, and most EMS companies worldwide proved they could operate safely. Their resiliency during the pandemic has made EMS companies even more attractive to investors.

CA: In the wake of Covid-19, companies are reviewing their staffing layout and product flow to reduce human bottlenecks and meet social distancing requirements. How will existing automation and software tools help fabricators and assemblers accomplish these goals?

Peter Bigelow *(president and CEO, IMI Inc.):* While I'm not necessarily an accurate predictor of the future, Covid-19's impact on how manufacturing companies harness technology to better conduct business should be felt in two basic ways: First, for all companies large and small, assembly and fabrication, the rapid adoption of software, secure internet, and virtual communication tools have made it possible for staff to work remotely and/or on split shifts. This should continue, especially for staff such as sales, finance and administration, etc., who are tethered to computers vs. workbenches or machines to perform their work. This includes functions such as CAM and machine programming. Second, for larger companies who typically are dealing with higher-volume lower-mix production, shop-floor automation has been and will continue to be embraced and invested in. Not that Industry 4.0 is here, but it certainly has made a large stride closer to being here thanks to Covid-19. People from top to bottom have seen how the benefits of automation can outweigh the limitations or previously perceived limitations that kept many companies from making the investments. One other non-technical impact of Covid-19 has been the embracing by both employees and managers of staggering, flexing and adding shifts, so fewer employees are in a facility or work area at the same time. This flexibility has enabled some facilities to move toward 24/7 production, even without adding automation.

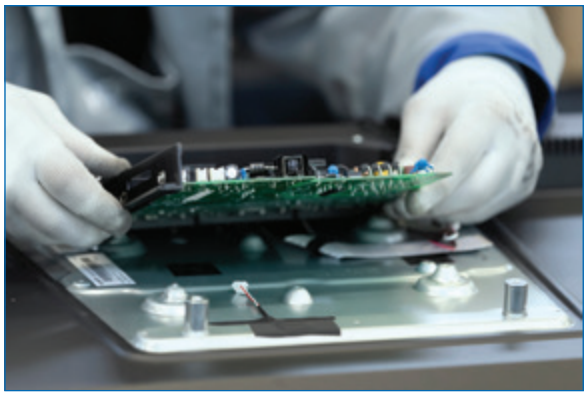

FIGURE 1. Covid changed the way some assemblers validate their soldering processes.

Teresa Huber *(president and CEO, Intervala):* Before Covid-19 hit, we had made, or were in the process of making, investments in a variety of tools and technologies to drive greater efficiencies within our business and better serve our customers. These included new automated insertion equipment for printed circuit board assemblies and an automated conformal coating system, among others. Our timing turned out to be fortuitous, as these tools have helped us streamline certain processes to require fewer operators who are able to perform their work at a safe distance from each other. A new manufacturing execution system (MES), enhanced planning tools and Microsoft Teams are allowing team members to participate in virtual collaborations, trainings and remote process reviews more safely and efficiently. Covid-19 presents a variety of challenges for sure, but the additional flexibility provided by these tools helps tremendously.

Michael Ford *(senior director emerging industry strategy, Aegis Software):* Manufacturing has always had to work within multiple constraints. Material/subassembly availability, hardware configuration, and changing customer demand are key elements, as well as organizational aspects of human operations, especially where needing to work in close proximity, including assembly, logistics and quality. With Covid-19, workstation spacing, walking paths around the manufacturing facility, and even the bathroom break schedule now must be planned with care. We used to be experts at this. The *muda-tori* approach within manufacturing once included defined walking paths, and speeds to and from the bathroom, with some facilities famously having lights that showed where you should walk and how fast. It was all measured and included in the planning operation. Where are our old-school industrial engineers today? Mass-production was so much easier than the high-mix, volatile environment we see today.

Constraints around the number of people working on the shop floor is the result of the pandemic but is also consistent with the introduction of additional assembly automation, so it must be good, right? This direction, however, brings with it the need for significant investment and concerns with deployment. Though there may be spare manufacturing capacity in some cases to allow time for the introduction and learning curves around such automation, companies that are able to justify the investment are likely to be those that don't have the opportunity to deploy right now. Care must also be taken that new automation does not compromise flexibility and agility, something human workers are prized for right now. Hardware automation innovation must therefore be a strong but secondary concern with the industry early in 2021, just a little more compelling than it has been previously.

Taking the holistic business approach for 2021, there are two necessities: first, to look after the health of all people working in manufacturing; second, the ability to be extremely flexible and agile to adapt manufacturing operations in response to any change of constraint or opportunity that presents itself. With shortages of key materials and supply issues on one side, we have on the other side significant change and

volatility of customer demand. Have you seen the price of webcams recently? Not the most difficult product to make, and many people are making serious money selling any stock they can find at highly inflated prices. How hard is it to switch production to meet newly forming demands? In the normal world, it was not so easy, but now with constraints on people, materials, etc., it seems to most like a nightmare.

It doesn't need to be. Having accurate and detailed visibility and control of production operations, materials, quality and logistics has never been so important. The use of MES introduces "soft automation" that is far more effective right now than hardware-based automation. Having operational information enables decisions to be made quickly and effectively that address immediate challenges, as well as allowing the business to take advantage of opportunities. Engineering tools within modern, effective MES solutions include the ability to configure work assignments on demand, including last-minute BoM changes and choices, as well as product customization capabilities, all of which are automatically reflected into work instructions created and deployed electronically in almost real time, carrying key information that allows flexibility without risk of productivity or quality loss.

FIGURE 2. Are the days of workers crowded together at adjacent stations a thing of the past?

Although hardware automation over time relieves the pressures on threats to health, there is right now the renewed need for precise visibility and control over manufacturing that only a holistic IIoT-based MES solution can provide. This is not a new concept. Mature tools are available right now, the demand for which we will see growing strongly throughout 2021 and beyond. It is the importance of selecting the right tools and having them installed and working effectively that is the key differentiator, greatly benefiting even the most modest of manufacturing operations.

CA: What is happening specific to the semiconductor industry in support of chiplet implementation?

Jan Vardaman *(president, TechSearch International):* New packaging solutions are being adopted to achieve the economic advantages that were previously met with silicon scaling. The role of heterogeneous integration, especially chiplets, is pivotal in this new era. TSMC indicates the use of chiplets will be one of the most important developments for the next 10 to 20 years. A chiplet is a functional circuit block and includes reusable IP blocks. A chiplet is an integrated circuit block specifically designed to work with other circuit blocks, including reusable IP blocks to form a larger, more complex system. A chiplet can be created by partitioning a die into functions and is typically attached to a silicon interposer or organic substrate today, but new options are emerging as advanced fan-out, RDL interposer, embedded bridges, and 3-D packaging. The chiplet is not a new idea, but EDA tool improvements are making new architectures possible. Foundries are also providing chiplet solutions for customers. The close cooperation between all segments of the industry, EDA tool vendors, IC designers, third-party IP providers, foundries, and OSATs will help drive the growth of chiplets into a wide range of applications. Adoption is not possible without these working relationships.

Phil Marcoux *(managing director, PPM Associates, with input from 22 colleagues, including* Mike Crawly *and other past executives from Signetics Semiconductor, which eventually became NXP):* Regarding chiplet implementation, the consensus of the group is despite much hype and promise about chiplets, large-volume implementations are still far and few. The same obstacles have hindered it, and many predecessors remain (think hybrids, MCMs, 2.5-D/3-D market attempts). Common obstacles are the difficulty of interconnectability between chips, lack of standards between chiplet suppliers of like chips, and high costs.

Chiplet implementations that rely on silicon substrates continue to struggle with the cost of silicon as a simple substrate.

Among the factors touted for chiplets are that system-on-chip development and manufacturing costs are much higher and longer than a chiplet. Experience in many cases has found chiplet implementation is a suitable entry product (MVP in today's terminology) until a suitable process technology is online to process the single chip version cheaper and with better performance.

Some of the large foundries, and in particular TSMC, employ this approach to not only hold onto customers but give both the customer and TSMC a chance to see if a product in chiplet form generates enough market volume demand to implement it in a single chip SoC or to sustain the market until the SoC is ready.

CA: IPC believes the US defense industry has been reluctant to migrate to lead-free electronics and is pushing Congress to fund research and development to help contractors make the transition. What needs to change in order for aerospace or military to use lead-free electronics in the preponderance of new designs?

Larry Romero *(ESF execution operations manager, Ball Aerospace):* In Ball Aerospace's current environment, the biggest issue we have is more on the space arena. The main issue we have is that of the unknown relative to the various different

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environments our hardware is subjected to during space orbits. As there are unknowns, we tend to err on the side of caution that have good legacy. We have migrated to ENIG board surface finishes for more manufacturability, as we have more high-pin-count dense-lead spacings that require flatness.

We typically don't have funding or time available to go down the path on our own to determine risk, test for identified risks and then implement the findings that will ensure we have a complete understanding of migrating from our current structures to a different one that will provide robust designs, as failure is not an option.

Dave Hillman *(fellow, materials and processes, Collins Aerospace):* The introduction of new materials such as lead-free solder alloys requires additional testing beyond the typical protocols established for commercial electronic products. Lead-free materials and soldering processes are currently being used successfully by a number of OEMs in a wide number of harsh environment products where the application risks are not life/mission/safety-critical. However, there is a serious need for funded joint industry/government R&D activity to establish baseline lead-free material and process datasets. The baseline dataset allows more efficient and effective design/manufacturing information dissemination for the harsh environment applications. Uniform lead-free electronics protocols and practices result in low-cost and high-reliability electronic products. Government-funded partnership with industry OEMs such as Collins Aerospace and industry organizations such as IPC is one methodology for widespread lead-free electronics acceptance.

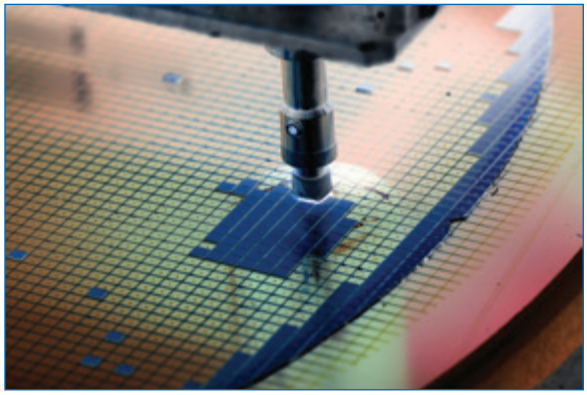

FIGURE 3. Can Intel continue to fabricate its own semiconductors?

Tim O'Neill *(director of product management, AIM Solder):* There is no easy solution to this conundrum. The available alternatives represent an increased risk over the SnPb in use and may require downstream material changes, further complicating the matter.

As the performance characteristics and manufacturing requirements of SnPb alloys are well understood, there is little incentive for military applications to implement lead-free solders. Military and aerospace have been largely exempted from the lead restrictions. Therefore, military designs continue to use SnPb processes and materials.

The ideal alloy replacement would have lower processing temperatures, improved thermal cycling and mechanical performance, and lower tin whisker risk than the current SAC-based alloys. Unfortunately, there simply is no combination of elements that can replicate lead in solder alloy.

Fortunately, alloys have been developed to meet military application requirements, but introduce additional challenges due to the widespread use of lead in these applications. Many of the new high-reliability alloys contain bismuth, which is incompatible with Pb-bearing solder. This is a significant complication, as it is impossible to know what was used during assembly and could adversely impact subsequent rework applications.

If there were congressional support that could aid the military electronics requirements, it would be in research and development funding to study the characteristics and implementation of this new class of SAC-based, high-reliability alloys.

CA: Is Intel's sale of its NAND memory business and the talk that it might use external foundries significant or just symbolic?

Marcoux and colleagues: IC manufacturing has always been expensive, but for the past decade or so, it has become almost impossible. Only a couple of companies can generate enough money to pay for both the product development and the process development/implementation of mass-volume semiconductor manufacturing.

Intel has been hurt by the successes of rivals such as AMD, which years ago moved to a fabless business model. It was only a matter of time before Intel had to do the same.

Our common worry is the US will lack the necessary manufacturing knowledge and acumen to maintain industry leadership, but we acknowledged the US gave up its desire to lead in IC manufacturing decades ago. Companies such as Apple have demonstrated the product profits are to be made not from owning the manufacturing but from the creation and marketing of products utilizing the manufacturing resources of others.

Name withheld *(retired senior executive, Intel):* Intel still fabs its own processors and intends to continue. So, it is still manufacturing in the US. The company made a number of incorrect management decisions and directions that caused it to lose market dominance. This sale, plus new management and the addition of new private equity investment, will give the company the financial clout to regain some dominance in the market. Intel is not planning to leave the fab business. ▫

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Materials Environment Drives New Challenges

Needed: Methods to best predict and adjust to demand spikes.

ANY SUPPLY-CHAIN management executive will likely tell you that 2021 is 2020 on steroids. Reason: While 2020 had supply-chain disruption, the worst part of that disruption was followed by drops in customer demand due to Covid-19-related lockdowns, so the situation never worsened beyond spot shortages or transportation delays. This year, pent-up consumer demand combined with historic low interest rates supporting consumer spending is spiking product demand in multiple industries as consumers make purchases they delayed in 2020. 5G infrastructure is rolling out, demand has increased for electric vehicles, which have substantially more electronic components per car, and Covid-19 continues to drive higher medical equipment production. As a result, demand variations are changing schedules weekly. At the same time, constraints developing in the materials market are driving higher prices and longer lead-times. Transportation and freight resources are stretched, and pricing and lead-times are increasing. Covid-19 continues to cause some level of disruption as hot zones develop around the world. In short, 2021 will be a year where multiple variables are constantly in flux.

Several constraints are likely in 2021:

- Unforecasted spikes in demand across multiple industries
- Component manufacturer and/or distributor decommits on material currently in forecast
- Increasing component lead-times
- Increasing transportation lead-times
- Unplanned disruption due to development of Covid-19 hotspots.

These constraints may drive additional constraints in production. For example, in a perfect Lean manufacturing world, production teams build to demand throughout the factory, even when the capacity to build more is available, because overproducing creates the waste of unnecessary inventory. However, in a world where demand is increasing dramatically week over week, building strictly to demand this week can lead to capacity constraints next week. Comparatively, adjusting production to build a buffer on projects with trends that suggest unanticipated order increases are likely helps break that constraint. In an environment of continual spikes in demand, reviewing and resizing material bonds and reviewing and resizing finished goods kanbans may need to be done monthly rather than quarterly or semiannually.

Managing the challenges of 2021 is more than simply focusing on breaking constraints to achieve the necessary throughput, however. This is the year systems strategy and management versatility will come to bear. The goal isn't filling warehouses with products in anticipation of increased demand or supply-chain disruption. One need only to look back to the telecom crisis at the turn of the century to see the pitfalls of that approach. Instead, the goal becomes developing the correct systems queries to best determine the products likely to have steep spikes in demand, appropriately assessing supply-chain risks, and modifying internal response as conditions change. It requires a 360-degree approach that encompasses program teams, purchasing, senior management and customer teams.

This strategy continues to be grounded in Lean manufacturing philosophy, but it needs to exploit systems visibility and personnel expertise in new ways to address the speed at which constraints may be changing.

For example, at SigmaTron International, customers are being encouraged to give longer forecasts. A 12-month forecast has been standard, but now at least 18 months is encouraged. Program teams are running horizontal MRP to view the total demand from each account and monitor the way consumption and demand is changing for the following three weeks to look for early indicators of changes in demand. IT tools that help assist with this modified reporting are being put in place.

SigmaTron uses a combination of proprietary and internally developed systems for enterprise and shop floor management. All facilities utilize a common ERP system plus third-party PLM tools. That combination enables all stakeholders to track demand, material on order, inventory, work-in-process, finished goods and shipments. An MRP Share program provides suppliers with complete customer forecast visibility, plus current inventory and material on order.

On the supply-chain side, this system enables the purchasing team to view consumption across the company on a given part or part manufacturer. When constraints develop, purchasing provides early trend warnings to program teams, which, in turn, warn customers. The system's auto-replenishment feature is monitored for late decommits. Core Lean practices such as identifying alternate sources for as much of the bills of material (BoMs) as possible are ongoing. Some of SigmaTron's international purchasing office

continued on pg. 44

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State-of-the-Art Technology Flashes

Updates in silicon and electronics technology.

Ed.: This is a special feature courtesy of Binghamton University.

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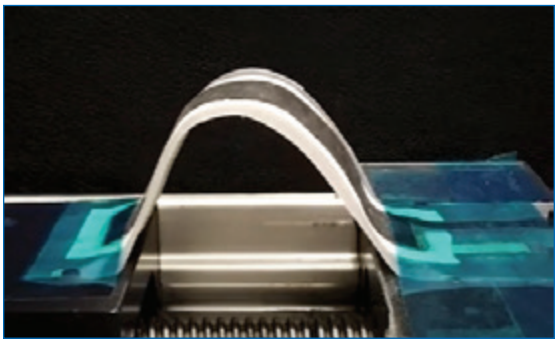
The **INTEGRATED ELECTRONICS ENGINEERING CENTER (IEEC)** at Binghamton University is a New York Center of Advanced Technology (CAT) responsible for the advancement of electronics packaging. Its mission is to provide research into electronics packaging to enhance our partners' products, improve reliability and understand why parts fail. Research thrusts are in 2.5/3-D packaging, automotive and harsh environments, bioelectronics, flexible and additive electronics, materials for packaging and energy storage, MEMS, photonics, power electronics, sensors, embedded electronics, and thermal challenges in electronic packaging. More information is available at binghamton.edu/ieec.

Breakthrough quantum-dot transistors create a flexible alternative to conventional electronics. Researchers at Los Alamos National Laboratory have created fundamental electronic building blocks out of tiny structures known as quantum dots and used them to assemble functional logic circuits. This development provides a low-cost and manufacturing-friendly approach to complex electronic devices. The building blocks can be fabricated in a laboratory with simple, solution-based techniques, and provide these components for a host of innovative devices. Potential applications of the new approach to electronic devices based on non-toxic quantum dots include printable circuits, flexible displays, lab-on-a-chip, wearable devices, medical testing, smart implants, and biometrics. *(IEEC file #11971, Science Daily, 10/29/20)*

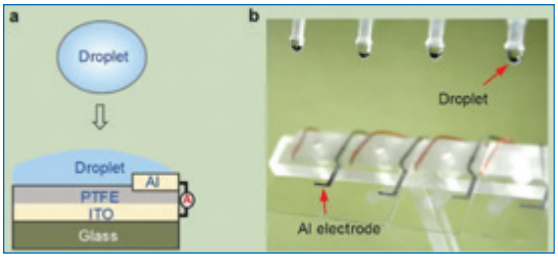
This flexible and rechargeable battery is 10 times more powerful than state-of-the-art. University of California researchers working with ZPower have developed a flexible, rechargeable silver oxide-zinc battery that provides five to 10 times greater energy density than current state-of-the-art. The battery also is easier to manufacture, as it can be screen-printed in normal lab conditions. The areal capacity for this innovative battery is 50ma/cm^2 at room temperature, which is 10 to 20 times greater than the areal capacity of a typical lithium-ion battery. The device can be used in flexible, stretchable electronics for wearables as well as soft robotics. *(IEEC file #12027, Science Daily, 12/7/20)*



Laser-on-silicon photonics process. Tower Semiconductor is participating in DARPA's Lasers for Universal Microscale Optical Systems (LUMOS) program, which aims to bring high-performance lasers to advanced photonics platforms, addressing commercial and defense applications, and to create a semiconductor foundry integrated-laser-on-silicon photonics process. This process will combine high-performance III-V laser diodes with Tower's production silicon photonics platform. The benefits of laser integration on silicon include an increase in the density of lasers, a reduction of coupling losses between the laser and the photonics, a reduction in components required and a much-simplified packaging scheme. *(IEEC file #12070, Electronics Weekly, 1/6/21)*

Engineers create hybrid chips with processors and memory to run AI on battery-powered devices. Processors and memory can consume 95% of the energy needed to do machine learning and AI, which severely limits battery life. Stanford University researchers have designed a system that can run AI tasks faster, and with less energy, by harnessing eight hybrid chips, each with its own data processor built right next to its own memory storage. Their development of RRAM, a new memory technology, stores data even when power is switched off, faster and more efficiently then flash memory. This design incorporates a critical new element: algorithms that meld the eight separate hybrid chips into one energy-efficient AI-processing engine called the Illusion System. The researchers developed this system as part of DARPA's Electronics Resurgence Initiative (ERI). *(IEEC file #12072, Science Daily, 1/11/21)*

Droplet-based energy generator lights up 100 LEDs. City University of Hong Kong researchers have made an energy breakthrough in a single drop of water. Their droplet-based electricity generator (DEG) provides renewable energy possibilities by creating electricity from falling rain. The DEG employs a structure based on the FET. The power generated can light up 100 small LED lights. This system's power density reaches up to 50.1W/m^2, which is thousands of times higher than similar devices, and offers short bursts of instantaneous power. *(IEEC file #12028, Tech Brief Insider, 12/8/20)*

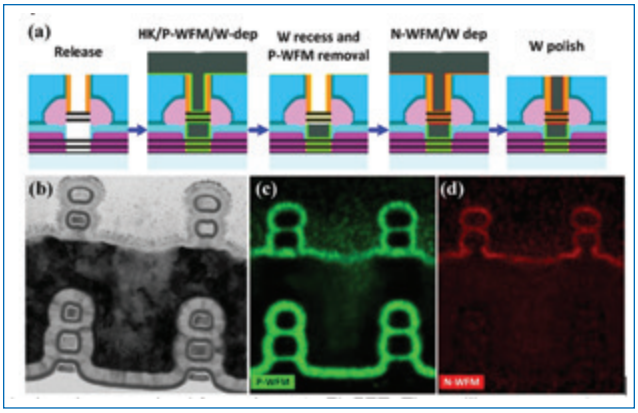


Platform for all-optical computing. Harvard University researchers have developed a new platform for all-optical computing where computations are done solely with beams of light. All-optical computing removes the rigid components and controls light with light. These platforms rely on nonlinear materials that change their refractive index in response to the intensity of light. When light is shone through these materials, the refractive index in the path of the beam increases, hence generating its own light-made waveguide. They developed a material that uses reversible swelling and contracting in a hydrogel under low laser power to change the refractive index. The hydrogel is composed of a polymer network that is swollen with water and a small number of light-responsive molecules known as spiropy-ran. When light is shone through the gel, the area under the light contracts a small amount, concentrating the polymer and changing the refractive index. When the light is turned off, the gel returns to its original state. *(IEEC file #12073, NASA Tech Briefs, 1/1/21)*

Light-carrying chips advance machine learning. In the digital age, data traffic is growing at an exponential rate. The demands on computing power for applications in artificial intelligence (AI) such as pattern and speech recognition or for self-driving vehicles often exceed the capacities of computer processors. University of Münster researchers are developing new approaches and process architectures that can cope with these tasks extremely efficiently. They have shown photonic processors can process information much more rapidly and in parallel. In the field of AI, more data can be processed simultaneously, while saving energy and providing more precise data analysis. Further applications include self-driving vehicles and IT infrastructures such as cloud computing. *(IEEC file #12069, Science Daily, 1/8/21)*

3-D-printed lens design improves data transfer possibilities. University of Illinois researchers have developed a spherical lens capable of allowing incoming light to be focused on the lens' surface opposite the input direction into a very small spot. The lens is one of multiple microlens designs introduced, each of which are 3-D-printed and feature adjustable refractive indices. The design of the lenses has the potential to improve existing imaging and communications methods. In computing, the lens technology is poised to enhance the ability of computer chips and other optical systems to perform data-routing tasks. The researchers used direct-laser writing, or multiphoton lithography, in the manufacture process that involves focusing a femtosecond-pulsed laser into a photopolymer. *(IEEC file #12052, Photonics Media, 12/15/20)*

Intel's stacked nanosheet transistors could be the next step in Moore's law. The logic circuits behind just about every digital device rely on the pairing of two types of transistors: NMOS and PMOS. The same voltage signal that turns one of them on turns the other off. Putting them together means electricity should flow only when a bit changes, greatly cutting power consumption. These pairs have sat beside each other for decades, but if circuits are to continue shrinking, they're going to have to get closer still. Intel researchers have showed a different way by stacking the pairs so one is atop the other. The scheme effectively cuts the footprint of a simple CMOS circuit in half, meaning a potential doubling of transistor density for future ICs. *(IEEC file #12057, Science Daily, 1/5/21)*

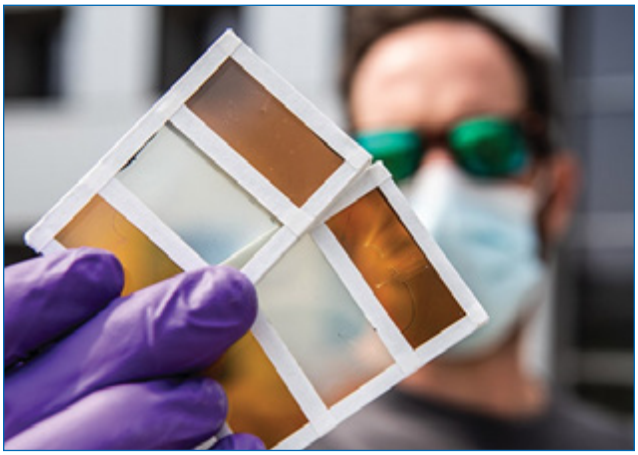


Cooling electronics efficiently with graphene-enhanced heat pipes. Researchers at Chalmers University have developed graphene-based heat pipes that can help solve the problems of cooling electronics and power systems used in avionics, data centers and power electronics. Current heat pipes are made of copper, aluminum or their alloys. The graphene-enhanced heat pipe exhibits a specific thermal transfer coefficient, which is 3.5 times better than that of a copper heat pipe. The new findings pave the way for using graphene-enhanced heat pipes in lightweight and large-capacity cooling applications. The graphene-enhanced heat pipes are made of high thermal conductivity graphene-assembled films assisted with carbon fiber wicker-enhanced inner surfaces. *(IEEC file #12050, Nano Magazine, 12/15/20)*

Two-sided solar cells to collect scattered light. To increase the performance of solar panels, University of Toronto and KAUST researchers have created a bifacial, or two-sided, tandem solar cell, built by bringing together the best of the perovskite and silicon technologies. Light reflected and scattered from the ground – known as "albedo" – can also be collected to significantly increase the current of a tandem solar cell. Bifacial silicon-only solar cells have rapidly taken an increasing share in the photovoltaics market, as they can lead to a performance gain of 20%. Exploiting this concept in perovskite/silicon tandems now opens opportunities for ultra-high-power generation at affordable cost. *(IEEC file #12074, Science Daily, 1/11/21)*

Thermoelectric window reduces need for air con, generates electricity. DoD's NREL researchers reported a breakthrough in a next-generation thermochromic window that not only reduces the need for air conditioning but simultaneously generates electricity. Heat generated by sunlight shining through windows is the single largest contributor to the need for air conditioning in buildings. Because residential and

commercial buildings use 74% of all electricity and 39% of all energy in the United States, the shading effect from tinting windows helps buildings use less energy. The technology, termed "thermochromic photovoltaic," allows the window to change color to block glare and reduce unwanted solar heating on a hot, sunny day. This color change also leads to the formation of a functioning solar cell that generates on-board power. *(IEEC file #11979, Printed Electronics World, 10/19/20)*



Motors officials described an ambitious vision for electric and autonomous vehicles at CES 2021, showing off a futuristic flying car drone concept and three new EV models based on a more efficient modular battery system called Ultium. The one-seater flying vehicle dubbed eVTOL (electric vertical take-off and landing) has four rotors and the ability to take off and land vertically. The drone uses a 90KwH EV motor to power the rotors and has air-to-air and air-to-ground communications. GM expects to invest $27 billion in EV and autonomous vehicle products through 2025. *(IEEC file #12085, Fierce Electronics, 1/13/21)*

Market Trends

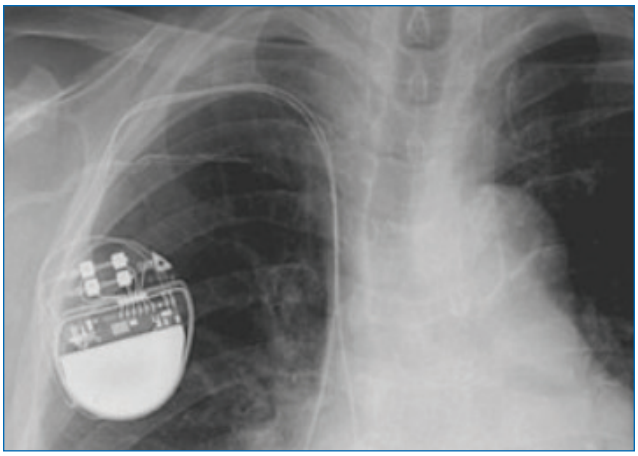
Air Force lab uses lasers to fabricate electronics using a new "transformative manufacturing" process. Electronic circuits require precise integration of materials in space to control the flow of electric current. On the horizon is a new technique using lasers to customize, design, repair and build electronics. Developed at the Air Force Research Lab, this laser "writing" technique allows the user to design and precisely place conducting, insulating, and semiconducting materials with ease utilizing a substrate coated with a thin film. This new manufacturing strategy is known as transformative manufacturing. Unlike additive or subtractive manufacturing, transformative manufacturing requires a film and a laser beam to pattern electronic devices. The laser beam acts as a means to change the thin-film through localized heating and causes reactions with the environment at extremely high temperatures. *(IEEC file #12034, Design Fax, 12/15/20)*

Smart building opportunities for printed sensors. Smart buildings promise automated control of the buildings' operations, along with integrated technology for human-machine interactions. Such functionality requires multiple sensors, to which printed/flexible electronics are very well suited due to their low weight and thin-film form factor. Indeed, the building of the future may have printed sensors built into the walls, floor and ceiling to detect water leaks, air quality, usage patterns, and more. These sensor applications include touch-sensitive walls, pressure-sensitive floors, leak detection, and gas sensing for air quality. *(IEEC file #12086, Printed Electronics World, 1/13/21)*

GM wows CES 2021 with flying car concept. General

Engineers race to develop wireless charging technology. An obstacle to widespread acceptance of electric vehicles is a recharging infrastructure that is fast and readily accessible. Stanford University researchers are developing wireless technology that addresses many of those constraints and challenges. They envision electric cars that recharge themselves as they speed along futuristic highways built to "refuel" vehicles wirelessly. Traditional wireless chargers transmit electricity by creating a magnetic field that oscillates at a frequency that creates a resonating vibration in magnetic coils on the receiving device. They developed a wireless charger that could transmit electricity even as the distance to the receiver changes. They did this by incorporating an amplifier and feedback resistor that allowed the system to automatically adjust its operating frequency as distance between the charger and the moving object changed. *(IEEC file #12083, Assembly Magazine, 1/11/21)*

Nano-thin piezoelectrics advance self-powered electronics. RMIT University researchers have developed a new type of ultra-efficient, nano-thin material that could advance self-powered electronics, wearable technologies and even deliver pacemakers powered by heartbeats. Flexible and printable, the piezoelectric material can convert mechanical pressure into electrical energy. It can be easily fabricated through a cost-effective and commercially scalable method using liquid metals. The new material is based on non-toxic zinc oxide, making it easy to integrate into current electronics. The technique can rapidly produce large-scale sheets of the material and is compatible with roll-to-roll processing. *(IEEC file #12092, New Electronics, 1/11/21)*



Recent Patents

Semiconductor packages with EMI supported stacked die (assignee: Intel Corp.; patent no. 10,796,975). The semiconductor packages may house a stack of die in a system-in-package (SiP) implementation, where one or more of the die may be wire bonded to a semiconductor package substrate. The die may be stacked in a partially overlapping and staggered manner, such that portions of some dies may protrude out over an edge of a die that is below it. This die-stacking may define a cavity, and, in some cases, wire bonds may be made to the protruding portions of the die.

Flexible printed circuit to mitigate cracking at through-holes (assignee: CommScope; patent no. 10,798,819). Flexible fingers for flexible printed circuits improve the crack resistance of prior art designs. The crack resistance can be improved by encapsulating the trace inside additional layers such that the outer two layers include only the lands of the through-hole, and all other copper is etched away. The crack resistance can also be improved by strategically adding copper on layers other than the trace layer, including attaching it to the land of the through-hole as a stub. These two designs can be combined to include a stub trace into a four-layered design.

Liquid cooling through conductive interconnect (assignee: Intel Corp.; patent no. 16/379619). Embodiments include semiconductor packages and cooling semiconductor packaging systems. A semiconductor package includes a second die on a package substrate, first dies on the second die, conductive bumps between the first dies and the second die, a cold plate, and a manifold over the first dies, second die, and package substrate, and first openings in the manifold. The first openings are fluidly coupled through the conductive bumps. The semiconductor package may include a first fluid path through the first openings of the manifold, where a first fluid flows through the first fluid path.

Semiconductor integrated optical device (assignee: Sumitomo Electric Industries; patent no. 16/831895). A semiconductor integrated optical device includes a waveguide mesa having a first multilayer including a first core layer, a second multilayer including a second core layer, and a butt joint interface between the first core layer and the second core layer; a support having first to third regions; and a buried semiconductor region provided on the support. The first multilayer has a first mesa width on the first region. The second multilayer has a second mesa width on the second region. On the third region, the second multilayer has a waveguide portion having a third mesa width smaller than the first and the second mesa widths.

Microelectronics package with vertically stacked flip-chip dies (assignee: Qorvo US, Inc.; pub. no. US10804246). The present disclosure relates to a microelectronics package with vertically stacked flip-chip dies and a process for making the same. The disclosed microelectronics package includes a module board, a first thinned flip-chip die with a through-die via, a second flip-chip die with a package contact at the bottom, and a mold compound. Herein, a top portion of the through-die via is exposed at top of the first thinned flip-chip die. The first thinned flip-chip die and the mold compound reside over the module substrate. The mold compound surrounds the first thinned flip-chip die and extends above the first thinned flip-chip die to define an opening. The second flip-chip die, which has a smaller plane size than the first thinned flip-chip die, resides within the opening and is stacked with the first thinned flip-chip die.

Substrates with ultra-fine-pitch flip-chip bumps (assignee: Zhuhai ACCESS Semiconductor; patent no. 10,779,417). A method of attaching a chip to the substrate with an outer layer comprising via pillars embedded in a dielectric such as solder mask, with ends of the via pillars flush with said dielectric, the method comprising the steps of (o) optionally removing organic varnish, (p) positioning a chip having legs terminated with solder bumps in contact with exposed ends of the via pillars, and (q) applying heat to melt the solder bumps and to wet the ends of the vias with solder. ▫

Hell Hath No Fury Like A Test Engineer Scorned

Or even mildly irritated. So watch those catchphrases.

AS WE MOVE into 2021, I resolve to renew my approach to doing business, call things as they really are, and exile all my peeves into permanent residence, where they belong, in their appropriate circle of Hell, apropos Dante Alighieri.

That's right: we're talking *Inferno*.

Flames have consequences.

Nine circles. Nine gripes. All therapy.

In ascending order of severity.

Here goes.

First Circle: Those who begin an email with the salutation "Hey."

As in, "Hey Robert, our driver just dropped off 1,594 boards for flying probe testing." No prior warning. "Can we come back in two hours to start picking them up?"

Or, "Hey Robert, can we call you up on Friday at 4 pm to ask you to open up and process our job this weekend?"

I don't know you from Adam (or Eve, although I see this approach from more Adams than Eves). So why the insincere familiarity? Don't count on better service. Do count on biased malevolent thoughts against a certain age group.

Hence the retort: "Hey customer, can you read? Did you overlook the lead time published in our quote? Insofar as the status of your spontaneous expedite is concerned, don't call us. We'll call you."

Hey? Who invented this? Where did this come from? When is it going away?

Second Circle: Those who fail to change the subject line after message 35 of an email thread.

As in, "AS9100 renewal certificate attached" heading an email detailing customer field failures owing to endemic solder joint cracking.

The subject and predicate don't match. The writer falsely assumes one knows the context and the content. Instead, we get cognitive dissonance. Dangerous in a time of diminished attention spans.

Blessed are those whose subject lines provide clear reference points, for they will obtain faster service and better answers. And we will all know what the hell is going on.

Third Circle: Those who substitute euphemisms, buzzwords and marketing-speak for factual language and direct confrontation.

A curmudgeon's Whitman sampler includes:

- Granularity (Details. Like rocks. Very small rocks. Or fine print for geologists.)
- Value proposition (Space filler. Multisyllabic term for "benefits," as in "what I really get for my money.")
- Issues (Euphemism for "problems," only nicer in an antiseptic, passive-aggressive sort of way, like "our x-ray images reveal your BGA has issues," rather than "your board is an abomination from the BGA outward. Whoever soldered this was under the influence and should consider rehab, or retraining, or both, immediately; meanwhile, they should not be permitted within a 12-mile radius of a pick-and-place line." Or, "Our accounting system has issues, which is why you haven't received payment for 180 days." And, "Your ITAR application has issues. It is missing your company's articles of incorporation." Why not simply say your ITAR application isn't close enough for government work?)
- Synergies (Valuable stuff the acquirer covets in the acquired.)
- Empowerment (Feel-good validation of one's silly choices, conferring a false sense of security.)
- Win-win (That which confers advantage, monetary or otherwise, to the originator under the guise of equality.)
- Partnership ("If you do what I want, we can be great partners!" Serendipity on the part of the one calling the shots. For reference, see Japanese '80s/'90s term *Kanban*, which loosely translated means "You be the bank.")
- Ecosystem (Partnership with a green veneer. Makes otherwise odious behavior politically correct.)
- Onboarding (Hiring, with an implied plank to be walked, when matters inevitably and invariably go south.)
- Anything ending in "curve" (Power curve, learning curve, etc. Mathematized language lending sophistication – "curve fitting" – to otherwise unremarkable human behavior and acquired experience.)
- Pivot (Change, welcome or not. Coercively employed to continue securing the blessings of receiving one's dinner; i.e., adapt or die.)
- New normal (The Way Things Are Going to Be. Presupposes an Old Normal. Presupposes someone or something qualified to know the difference and proclaim the change. Presupposes those hearing and comprehending the difference accept it. Prone to differences of opinion.)
- Data (numbers feeding an archive to be weaponized and manipulated accordingly should the opposing party grow obstreperous, usually, and safely, long after the originating project engineer has retired.)
- Evidence-based (the antithesis of rumor and innuendo-based; meant to confer status and respectability while stating the obvious.)

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Fourth Circle: Throwaway lines.

Like emails prefaced by "In these unprecedented times." Or, "We're all in this together." Or, "Testing doesn't add value."

Really?

Empathy never came so cheap. And testing really *does* add value. Even at Six Sigma.

Consider the undisputed heavyweight world champion of throwaway lines for test engineers: "I'll keep you in mind." As in, "Your quote for in-circuit testing was outrageously expensive compared with what we've been paying our source in Uttar Pradesh, and in the probabilistically doubtful event that source is struck by a meteor, we will keep your services in mind as a fallback option."

Of course, this isn't what the customer says. This is what the customer *thinks*.

As suppliers, when we hear, "We'll keep you in mind," we think, "We won Miss Congeniality again." Not to mention, "Have a nice life." We won't be waiting by the phone.

When you see throwaway lines like these, throw them away.

Fifth Circle: Ethics statements.

Definition: Virtue signaling: To take a conspicuous but essentially useless action ostensibly to support a good cause but actually to show off how much more moral you are than everybody else (Source: *Urban Dictionary)*.

Exhibit A: A new customer wishes to use our flying probe test services. But first, as part of their supplier onboarding process (see above), we must sign an ethics statement, solemnly pledging not to attempt any of the following:

- Use forced or involuntary labor
- Use child labor
- Discriminate on the basis of race, religion, age, nationality, ethnicity, sex, sexual orientation, gender identity or expression, marital status, pregnancy, political affiliation, or disability
- Procure gold, tantalum, tungsten, or tin from sources in the Democratic Republic of Congo (so-called "conflict minerals")
- Bribe the customer's employees or otherwise engage in corrupt practices.

Agreed. We have no problem with any of these clauses and support their intent firmly. Who of right mind and common sense wouldn't?

However, unbeknownst amid the self-righteousness, the customer may also, without penalty, insist contractually on 120-day payment terms; procure services at or below cost; and abscond with engineering information gleaned from this supplier relationship to obtain cheaper pricing for identical services overseas. All in the interest of partnership. There is no irony clause in their ethics statement.

Rightness is as rightness does. For appropriate action see Fourth Circle above.

Sixth Circle: Junk marketing email.

Yes, I'm talking to you, Chinese circuit board companies and procurers of attendee lists of yet-to-be held trade shows. Are 10 emails daily really the way to capture attention, my dear long-lost but extremely close possible friend from Shenzhen? No need for elaboration here, as I've written previously and extensively about this scourge. It was a pandemic long predating the pandemic.

Just hit delete.

Seventh Circle: Covid as a universal excuse.

Press release: "In these unprecedented times, we are empowered to search for evidence-based data illuminating new synergies and a renewed ecosystem partnership that will give us a granular value proposition as we scrutinize evidence-based data to pivot down the power curve for the duration of the New Normal in the roaring 2020s."

Translation: Our company was a basket case before Covid-19 hit. The pandemic gives us cover to clean house and right serious, nearly fatal self-inflicted sins, while earning approbation for adapting to the times. Truly a win-win! At least a moral two-fer. Maybe in six months we can obtain a list of Chinese circuit board companies attending trade shows that approve of our decision. Ain't technology grand?

The writer of such pathetic prose should be condemned to create granularity (break rocks) for all eternity.

Eighth Circle: Attempts to secure free engineering.

A capital offense. Especially when remarketed as original engineering.

Attempts at free engineering sometimes stem from technical ignorance. Other times from diabolical intent. Somehow gratuitous engineering escapes mention in ethics statements such as the example above. Imagine!

Either way, test engineers worth their salt have well-developed radar for identifying opening gambits for free or below-cost services.

Engineering is not free. Somebody always pays, in product or time. If you turn away from offered services, you still have a problem. The other nagging truth is we still have a solution.

And stealing remains stealing in any language.

Ninth Circle: Needless complexity, brought about either by failing to tell, or hear, the truth.

Tell us what you want, when you want it, and how you want it. Straight up: do not mince words.

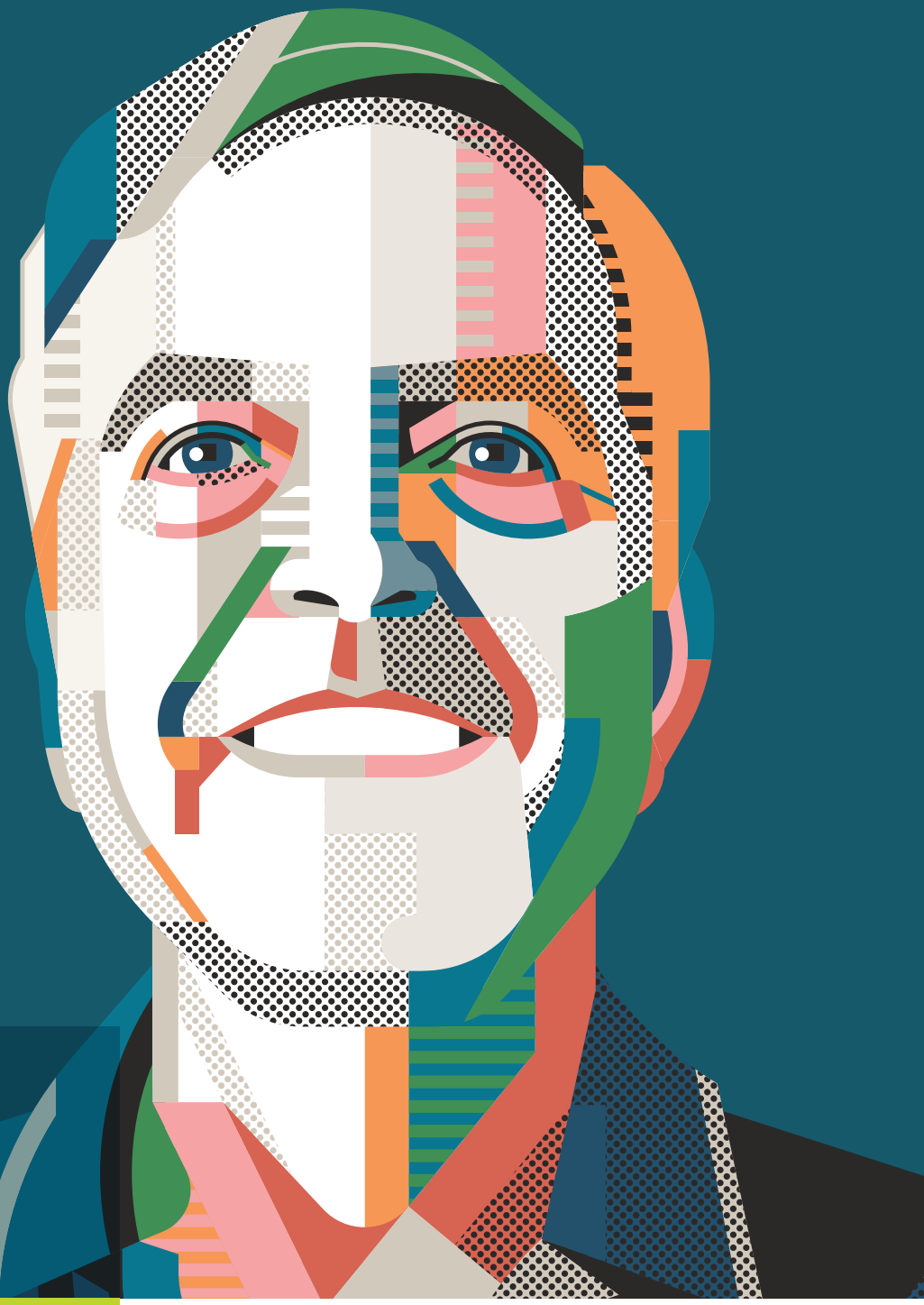
There is no fake news in test engineering. Bluffing your way through a test specification, lacking a detailed statement of work, works once. You either know the subject matter or you don't. If you don't, and you conceal that you don't, you will be found out and frozen out, just like the Devil in Dante's Ninth Circle. A very solitary place indeed.

Truth, n. *An ingenious compound of desirability and appearance. Discovery of truth is the sole purpose of philosophy, which is the most ancient occupation of the human mind and has a fair prospect of existing with increasing activity to the end of time.* (Source: Ambrose Bierce, *The Devil's Dictionary)*

Or so we hope.

Thus warned, make it a good year. □

Dennis Ralston
Sr. Director –
Government Relations and Cooperative R&D
KLA



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PCB and Component Coating Dewetting

As-supplied component residues are often the culprit.

THIS MONTH WE look at dewetting on the surface of solder mask or components in manufacture.

FIGURES 1 and **2** show the impact of dewetting on the surface of plastic components in conformal coating. Figure 2 illustrates dewetting on solder mask. In both cases if the coating does not cover all the critical areas of the assembly, it must be reworked. It is up to the quality and design departments to agree what level, if any, of dewetting is acceptable to the product and the customer, rather than just quoting a standard. In some cases, the position or level of the problem may not affect the product operation or reliability.

Dewetting on components is most commonly associated with residues on components as-supplied. In addition, it can be caused by material from other assembly processes. This is also the case with solder mask, as the surface is soldered and the board is cleaned, which can affect coating adhesion. This Defect of the Month video explains some of the dos and don'ts (https://youtu.be/nuV6FYexzCM).

We have presented live process defect clinics at exhibitions all over the world. Many of our Defect of the Month videos are available online at youtube.com/user/mrbobwillis. □

BOB WILLIS
is a process engineering consultant; bob@bobwillis.co.uk. His column appears monthly.

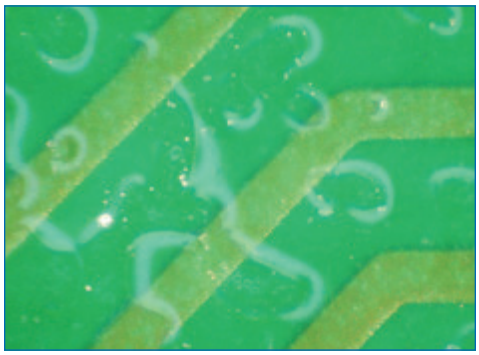


FIGURE 1. Conformal coating dewetting on a plastic component.

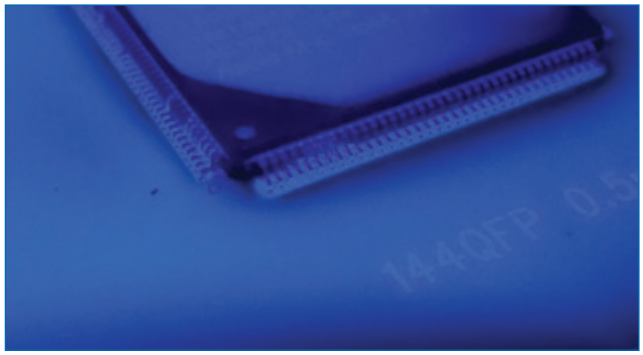


FIGURE 2. Dewetting on solder mask.

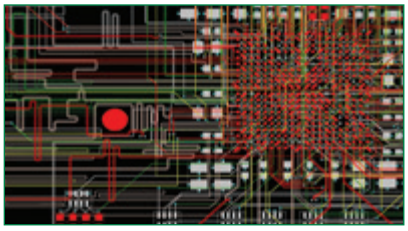
Getting Lean, continued from pg. 41

(IPO) has been reallocated to assist North American teams in this effort.

Senior management has a stronger focus on communicating with component manufacturers and distributors to highlight the criticality of projects and push back on policies that drive unacceptable risk. For example, in the current materials market, orders are locked for six months as a result of current demand. The nonreturnable, noncancellable (NCNR) period has stretched out accordingly. However, assigning NCNR to forecasted demand 12 months out is unacceptable because at that point component manufacturers have not committed resources to building those parts. Consequently, management needs to be vigilant in monitoring changing terms that don't reflect business realities as the irrational exuberance of a seller's market hits the components market.

Finally, expectations need to change. There will be price inflation in the coming year. In some cases, allocation may require use of non-franchised distributors. Planning horizons need to factor in longer shipping times. Discussing these issues with customers before they cause a problem helps for better decision-making should these issues arise.

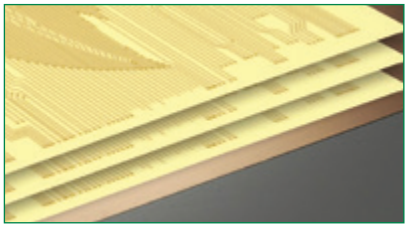
The coming year holds many challenges. That said, those challenges should not be reason to abandon the benefits of Lean philosophy. Teams just need to be prepared to analyze trends and adjust buffers more frequently. A system that supports real-time analysis as a visual factory tool and a proactive approach to identifying constraints and options for breaking those constraints are critical to maintaining a cost-efficient level of effective responsiveness. Much of this steep demand is an anomaly driven in part by 2020 lockdowns. Markets may slow abruptly as pent-up demand is satisfied. There can be no inertia in adapting buffers as those trends become evident. □



PULSONIX V. 11.0

Pulsonix version 11.0 offers significant speed improvements and new functionality for high-speed designs. Dramatically reduces time to perform many PCB design operations, such as DRC, copper pouring and Gerber generation. Complete rewrite of underlying graphics engine displays some large designs up to 2.5 times faster. Extends multi-threading capabilities.

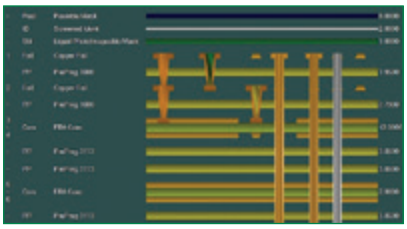
Pulsonix
pulsonix.com



HITACHI CHEMICAL MCL-HS200

MCL-HS200 advanced functional laminate features low polarity resin materials and low dielectric glass cloth for low transmission loss and warpage. CTE is 10 ppm/°C and dielectric constant (Dk) is 3.4 @10GHz. For 5G, ADAS, and AI.

Hitachi Chemical
hitachi-chemical.com



POLAR INSTRUMENTS SPEEDSTACK 21_02

Speedstack 21_02 stackup tool supports a new shield material type, allowing addition of shielding materials for rigid and flex PCB constructions. Exports/imports shield library data via third-party tools like Excel. Includes stackup editor enhancements: shield material options to add, delete, swap, move up, move down, symmetry and set properties. Impedance and insertion calculations support new shield material type.

Polar Instruments
polarinstruments.com

OTHERS OF NOTE

VISHAY MKP1848H

MKP1848H series DC-Link metallized polypropylene film capacitors are optimized for high humidity environments. AEC-Q200-qualified; withstand temp. humidity bias testing of 85°C, 85% RH for 1,000 hr. at rated voltage without alteration of electrical characteristics. Radial leaded.

Vishay
vishay.com

PASTERNAK PCB ANTENNAS

PCB antennas are for Wi-Fi, GSM, CDMA, 3G, 4G, LTE, GPS, Bluetooth, ZigBee, ISM and NB-IoT applications. Come in 23 embedded types and feature small form factor PCB design with frequencies ranging from 700MHz to 5.8GHz, gain ranging from 0dBi to 5dBi, and UMCX connectors. Support end-use applications such as use in wireless networking devices.

Pasternak
pasternak.com

TE ICCON BLOCK

ICCON Block and ICCON Insert connectors for high-speed board-to-board and board-to-busbar data communication offer easy installation for applications up to 350A. Optional floating feature for +/-1mm radial misalignment when mating two PCBs or busbars.

TE Connectivity
te.com/usa-en/home.html

TT ELECTRONICS METAL FOIL CHIP RESISTORS

Metal foil chip resistors combine heat-spreading properties of ceramic substrate with surge tolerance of bulk metal alloy resistance element. Lower self-heating levels than thick-film or metal strip resistors and better surge tolerance than thick-film options. Minimize use of PCB area. Sizes from 0402 to 2512.

TT Electronics
ttelectronics.com

OPTOMEC AEROSOL JET HD2

Aerosol Jet HD2 3-D additive manufacturing printer produces high-resolution circuitry, including ability to dispense conformal 3-D interconnects between die, chips, components and substrates. Is suited for 5G and mmWave applications. Prints features as narrow as 10µm with placement accuracy under 5µm on polymers, IC materials, FR-4, and more.

Optomec
optomec.com

SUNSTONE PCB123

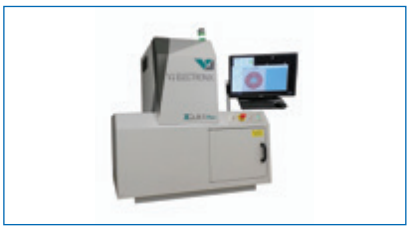
PCB123 printed circuit design and ordering software now includes option for ordering and sending Gerber files without any further steps on the users' part. Is for designers who want to keep a library of completed and tooled Gerber files.

Sunstone Circuits
sunstone.com

EVS 18KLF

18KLF solder recovery system has a 40lb pot. Recovers up to 80% of pure solder. Has touchscreen display and is automatic. Provides clean ingot bar as it filters solder through gauze. Includes sealed cabinet, enclosing dross bucket and fume extraction. Has tilting pot mechanism. Inverting and rotating dross/solder pot and hot-air-activated auto drain tap create solder ingots. ISO14001 compatible.

EVS International
solderrecovery.com



VJE XQUIK II PLUS

XQuik II Plus component counter has less than 20 sec. cycle time for single reel and quad counts. AI detection algorithms automatically recognize components. Automatically determines whether up to four small reels are loaded and keeps track of reel location. Built-in barcode reader eliminates extra manual scanning steps.

VJ Electronix
vjelectronix.com

SAWA SC-BP3

SC-BP3 multi-purpose bubbling cleaning system reportedly cleans flux five times faster than immersion cleaning. Uses air valve in place of electricity. Bubble washer features tank large enough to clean 10 pallets simultaneously. Removes flux by soaking parts. Bubble washing system includes rinse and drying units for cleansing/rinse/drying in 20 to 30 min. Pica solvent is safe and odor-free with no flame point, sustainable and eco-friendly. Can be used with other low-VOC and water-based cleaning solutions.

Sawa	Seika Machinery
sawa-corp.co.jp/en	seikausa.com

OTHERS OF NOTE

AIM W20 SOLDER PASTE

W20 water-soluble solder paste is a zero-halide/halogen flux formula engineered for enhanced wetting performance on all solderable electronic surfaces. Exhibits excellent print characteristics and 8+ hr. of stencil life. Residues are reportedly easily removed in plain water, even under low-standoff components.

AIM Solder
aimsolder.com

KEYSIGHT 800G

800G test systems validate electrical and optical interfaces to speed development of data center technologies. Electrical and optical analysis products enable 800G ecosystem, consisting of optical components, chipset, switch and semiconductor IC vendors, as well as system integrators, to speed design, development, test and validation across design cycle. Include 100Gb/s electrical conformance test.

Keysight Technologies
keysight.com

1 CLICK SMT ANT-I2

Ant-i2 offline selective soldering machine includes two drop-jet fluxers, bottom preheat zone, optional top preheat zone, and one solder pot with two individual selective wave tunnels. Handles two max. 350 x 215mm boards simultaneously. Optional nitrogen purity monitoring.

1 Click SMT Technology Co.
1clicksmt.com

IPC CFX

IPC-CFX Self-Validation and Equipment Qualification System is a cloud-based test bed for equipment vendors and manufacturing facilities to self-validate CFX messaging. Establishes CFX equipment portal with independent third-party validation of equipment. Ensures CFX connections, broadcasting, and consumption of CFX messaging.

IPC
ipc.org

MACDERMID ALPHA OM-372

OM-372 Pb-free, no-clean solder paste is for fine-pitch, low-standoff components. Low post-reflow residue on fine feature pads as low as 008004. Minimizes HiP/NOW. Advanced SIR performance. Comes in Type 5 and Type 6. Requires nitrogen reflow (≤1000ppm O_2).

MacDermid Alpha
macdermidalpha.com

TRI TR77000QM SII

TR77000QM SII 3-D AOI has 5.5µm 12MP imaging technology for semiconductor, packaging, and other applications. Metrology capabilities enable high accuracy and reliability inspection.

Test Research Inc.
tri.com.tw/en/index.html

In Case You Missed It

This column provides abstracts from recent industry conferences and company white papers. Our goal is to provide an added opportunity for readers to keep abreast of technology and business trends.

Carbon-Based Conductors

"Fast Response Organic Supramolecular Transistors Utilizing In-Situ π-Ion Gels"

Authors: Soh Kushida, *et al.*

Abstract: Organic electrochemical transistors (OECTs) are transistors that involve electrochemical doping. Although the device configuration of OECTs is identical to that of electrolyte-gate OFETs, the principal mechanism differs fundamentally. Once a gate bias is applied, ions pass through the boundary and penetrate the active layer. As a result, the whole layer is electrochemically doped, gaining a volumetric current through the full 3-D channel. In this paper, the authors present a new class of supramolecular transistors, named π-ion gel transistors (PIGTs), that employ an *in situ* π-ion gel as an active layer, as well as an internal gate capacitor. PIGTs exhibit a large transconductance of 133μS, retaining a hole carrier mobility (4.2×10^{-2}cm^2 V^{-1} s–1) and an on/off ratio ($\approx 3.7 \times 10^4$) comparable to those of supramolecular devices. Due to the unique device structure, PIGT shows a response time of <20μs, the fastest time among accumulation-mode electrochemica-based transistors ever reported. (*Advanced Materials,* December 2020; https://onlinelibrary.wiley.com/doi/10.1002/adma.202006061)

Final Finishes

"ENIG – Corrosion: When It Gets Critical and How Is the Status in the PCB Industry?"

Author: Britta Schafsteller, Ph.D.

Abstract: ENIG is one of the basic final finishes that has been accepted in the market for decades. As the nature of the gold deposition is an immersion reaction, dissolution of nickel and the risk of extensive nickel corrosion is imminent. The so-called "black pad" defect, which refers to excessive nickel corrosion with a two-dimensional surface attack, has been described extensively in literature. But although ENIG corrosion is a highly discussed topic, ENIG still counts as one of the most successful and most reliable surface finishes in the market. ENIG corrosion does not cause issues in the solderability or reliability of the coating. The specification establishing the acceptable corrosion amount and type, layer performance and solder connection is discussed and defined in the latest revision of IPC-4552. (SMTA International, September 2020, https://smta.org)

Solder Joint Reliability

"Influence of Joint Arrangement on the Fracture Behavior of Lead-Free Solder Joints"

Authors: Sadegh Mirmehdi, *et al.*

Abstract: This research investigates the influences of joint arrangement (loading arm and load sharing) on the level of constraint imposed on joint deformation, fracture energy, and generally, fracture behavior of solder joints. Fracture behavior of solder joints using double-cantilever-beam (DCB) specimens as a function of loading arm and load sharing (i.e., the distance between two solder joints) was studied under mode I loading conditions at a strain rate of 0.03 s^{-1}. By increasing the loading arm, the fracture force, F_{ci}, decreased linearly, while the critical strain energy release rate for crack initiation, J_{ci}, increased from a loading arm of 12.7mm to 38.1mm and then remained almost unchanged for loading arms of 38.1mm to 71.1mm. Plastic deformation in the solder layer and criteria such as opening stress (i.e., the predominant stress component in DCB specimen) and stress triaxiality factor were calculated. It was shown that for the larger loading arms (from 38.1mm to 71.1mm), the fracture behavior was as a normal DCB specimen (i.e., the normal stress caused by bending was predominant and normal stress caused by tensile loading could be ignored). For the loading arm of less than 38.1mm, the fracture behavior was similar to that of tensile-type specimens (i.e., the normal stress caused by bending decreased significantly by decreasing the loading arm and normal stress caused by tensile loading became considerable). Variations in the distance between two solder joints did not affect the J_{ci} value, while F_{ci} was influenced by the joint arrangement. This behavior was attributed to stress distribution in the solder layer. (*Journal of Electronic Materials,* January 2021; https://link.springer.com/article/10.1007/s11664-021-08748-4)

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EM Solutions Inc.
EMA Design Automation
Firan Technology Group - FTG
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